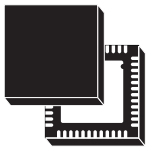
STLC2150

BLUETOOTH® RADIO TRANSCEIVER

- Bluetooth® v.1.2 specification compliant
- Fully integrated single chip:
  - transceiver with minimum of external RF components
  - PLL completely integrated
  - Integrated antenna switch
- Supports Power Class 2 and 3 operation with power control
- Supports Power Class 1 operation with an external Power Amplifie
- Outstanding maximum usable input signal
- Interface with base-band:
  - BlueRF compatible
  - unidirectional
  - received data: RxMode2 and RxMode2+ are supported
  - serial interface: JTAG
- CMOS technology
- Standard VFQFPN-48 package
- Low standby power consumption
- Extended temperature range
- Compliant to automotive specification AEC-Q100



VFQFPN-48 (7x7x1.0mm)

ORDERING NUMBER: STLC2150
Temperature range: -40 to 85 °C

APPLICATIONS

- Wireless data transmission applications to 432 Kbps symmetrical or 721 Kbps asymmetrical.
- Typical applications in which the STLC2150 is used are:
- Computer peripherals
- Modems
- Cameras
- Portable computers, PDA
- Handheld data transfer devices
- Mobile phone
- Other types of devices that require the wireless communication provided by Bluetooth®.

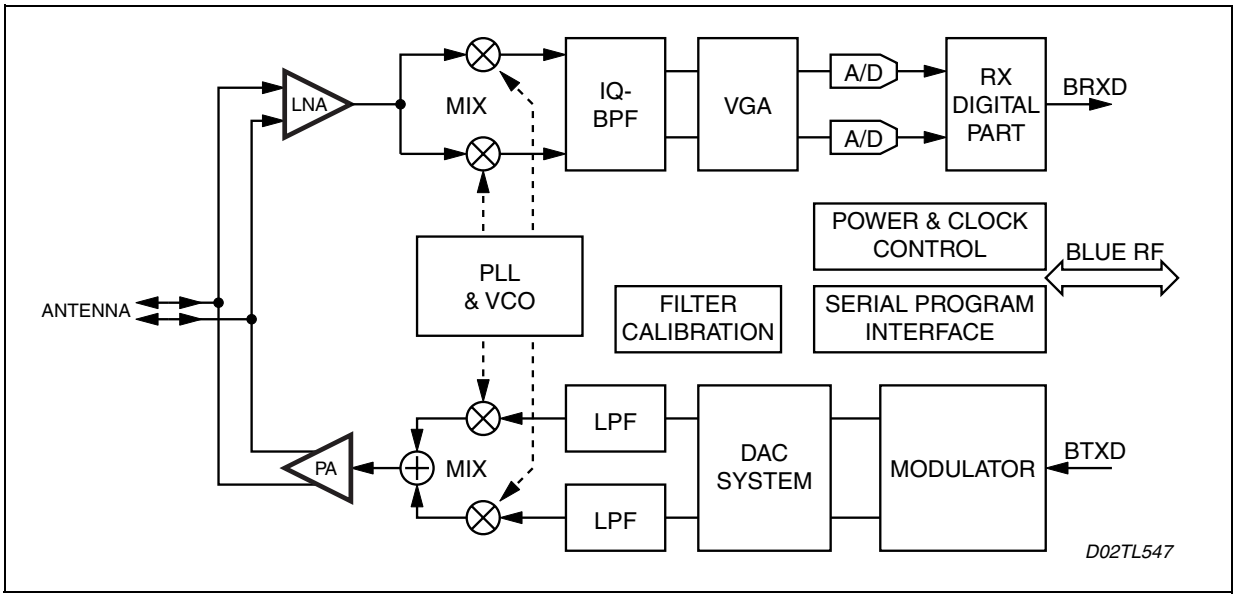
DESCRIPTION

The STLC2150 is a fully integrated Bluetooth® single chip radio transceiver. Together with a BB processor, like STLC2410, it offers a compact and complete solution for short-range wireless connectivity for a variety of applications.

The STLC2150 implements a low-IF receiver for Bluetooth® modulated input signals and no external IF filtering is required. The GFSK demodulator is fully integrated and supplies digital output data and RSSI. The transmit section features a fully integrated GFSK modulator, followed by a direct up-conversion stage, giving an output signal of 0 dBm. Optional power control is available.

On-chip VCO covers full Bluetooth® band and contains all of the tank resonator circuitry. Unidirectional BlueRF compatible interface and 4 wires serial JTAG interface are used to control all functions of radio transceiver, enabling operation with wide range of BB processors.

BLOCK DIAGRAM



QUICK REFERENCE DATA

Table 1. Absolute Maximum Ratings

Operation of the device beyond these conditions is not guaranteed.

Sustained exposure to these limits will adversely effect device reliability.

Symbol	Conditions	Min	Max	Unit
V_{DD}	Power supply Analogue and Digital Core	V_{SS} - 0.3	3.5	V
V_{IN}	Input voltage on any pin	V_{SS} - 0.3	V_{DD} + 0.3 AND < 3.5(*) V_{DDIO} + 0.3 AND < 4.6	V
V_{SSDIF}	Maximum voltage difference between different VSS* pins	-0.3	0.3	V
V_{DDIO}	Power supply for digital I/O	V_{SS} - 0.3	4.6	V

(*) Analogue test and RF pins only.

Table 2. Operating Ranges

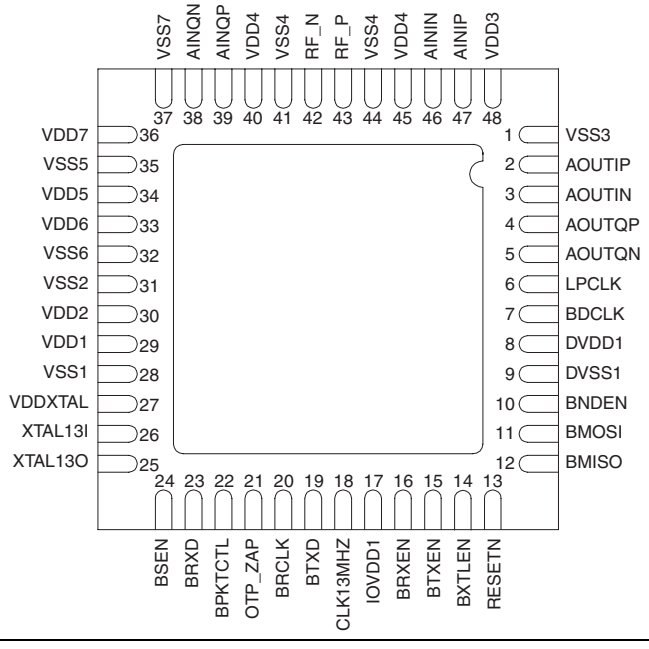
Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied.

Symbol	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply Analogue and Digital Core	2.62	2.70	2.78	V
V_{DDIO}	Power supply for I/O	2.50		3.60	V
T_{amb}	Ambient temperature	-40		85	°C

Pin Description and Assignment

Pin#	Pin Name	Description	Pin#	Pin Name	Description
1	VSS3	Analogue Ground	25	XTAL130	13 MHz Crystal oscillator output pin
2	AOUTIP	Analogue test output	26	XTAL13I	13 MHz Crystal oscillator input pin
3	AOUTIN	Analogue test output	27	VDDXTAL	13 MHz oscillator supply
4	AOUTQP	Analogue test output	28	VSS1	Analogue Ground
5	AOUTQN	Analogue test output	29	VDD1	Analogue Supply
6	LPCLK	3.2 or 32 KHz clock output	30	VDD2	Analogue Supply
7	BDCLK	JTAG TCK	31	VSS2	Analogue Ground
8	DVDD1	Digital Core Supply pin	32	VSS6	Analogue Ground
9	DVSS1	Digital Core Ground pin	33	VDD6	Analogue Supply
10	BNDEN	JTAG TMS	34	VDD5	Analogue Supply
11	BMOSI	JTAG TDI	35	VSS5	Analogue Ground
12	BMISO	JTAG TDO	36	VDD7	Analogue Supply
13	RESETN	Reset	37	VSS7	Analogue Ground
14	BXTLEN	Oscillator enable	38	AINQN	Analogue test input
15	BTXEN	Tx path enable	39	AINQP	Analogue test input
16	BRXEN	Rx path enable	40	VDD4	Analogue Supply
17	IOVDD1	Digital IO Supply pin	41	VSS4	Analogue Ground
18	CLK13MHZ	13 MHz output	42	RF_N	RF antenna connection
19	BTXD	Tx data	43	RF_P	RF antenna connection
20	BRCLK	1 MHz-clock associated with data	44	VSS4	Analogue Ground
21	OTP_ZAP	OTP ZAP	45	VDD4	Analogue Supply
22	BPKTCTL	Access code successfully decoded	46	AININ	Analogue test input
23	BRXD	Rx data	47	AINIP	Analogue test input
24	BSEN	Synthesizer enable	48	VDD3	Analogue Supply

PIN CONNECTION (bottom view)



CURRENT CONSUMPTION

Table 3. Typical Current Consumption

Symbol	Parameter	Typ	Max	Unit
Istby	Current consumption in standby mode (@27 °C)	5		µA
Irx	Current consumption in Receive mode	40	52	mA
Itx	Current consumption in Transmit mode	66	80	mA
Ivco	Current consumption when only PLL is enabled	22	TBD	mA
I32K	Current consumption when only the 32-kHz clock oscillator is operating	TBD	TBD	µA

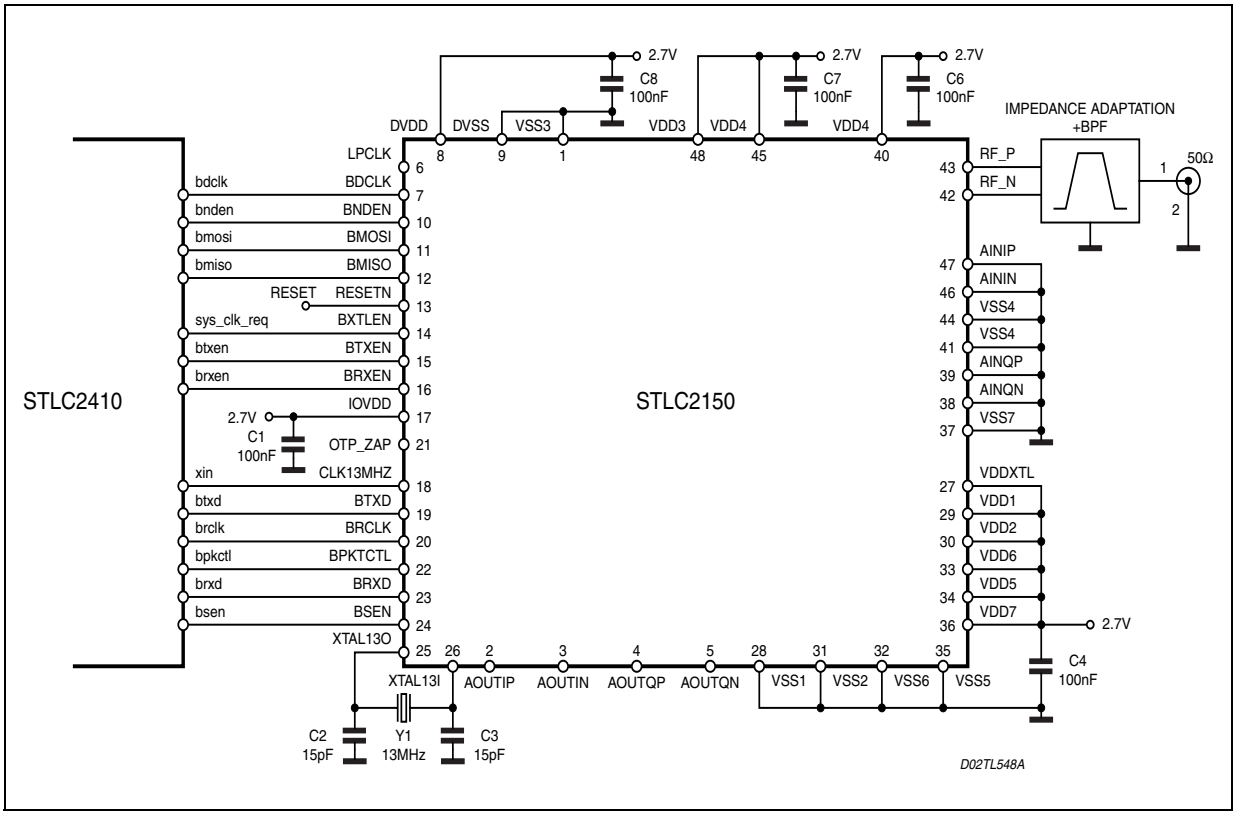
I/O CELL CHARACTERISTICS

Table 4: CMOS DC Electrical characteristics, rated for the operating range

Symbol	Parameter	Min	Max	Unit
V_{IH}	High Level Input Voltage	80% of V_{DDIO}		V
V_{IL}	Low Level Input Voltage		20% of V_{DDIO}	V
V_{OH}	High Level Output Voltage	85% of V_{DDIO}		V
V_{OL}	Low Level Output Voltage		0.4	V
V_{t+}	Schmitt trigger rising threshold	1.4	2.0	V
V_{t-}	Schmitt trigger falling threshold	0.5	1.2	V
	Schmitt trigger minimum hysteresis	248		mV

APPLICATION REFERENCE DESIGN

Figure 1. reference design schematic diagram



FUNCTIONAL DESCRIPTION

Receiver

The STLC2150 implements a low-IF receiver for Bluetooth® modulated input signals. The radio signal is taken from 75Ω balanced RF input and amplified by an LNA.

The mixers are driven by two quadrature signals which are locally generated from a VCO signal running at twice the frequency. The output signals in the I signal path and Q signal path are bandpass filtered by a polyphase bandpass filter for channel filtering and image rejection. The output of the lowpass filters is amplified by a VGA to the optimal input range for the A/D converters.

Further filtering is done in digital filters. The digital part demodulates the GFSK coded bit stream by evaluating the phase information in the I and Q signals.

The digital part recovers the receive bit clock. It extracts RSSI data by calculating the signal strength. Overall automatic gain amplification in the receive path is controlled by the digital part.

Transmitter

The transmitter takes the serial input transmit data from the base-band. This data is GFSK modulated to I and Q signals. The Tx bit clock is provided to the base-band for synchronization.

The output of the digital part is converted to analogue signals which are lowpass filtered before being sent to direct up-conversion mixers.

The quadrature up-conversion mixers use the same LO as the receiver. 0dBm output power at the antenna port is achieved with an internal PA, which has 75Ω balanced RF output. Optional power control is available.

PLL

The on-chip VCO is part of a PLL, the frequency is programmed for the RF channels by the digital part. The tank resonator circuitry for the VCO is completely integrated.

Process variations on the VCO center frequency are calibrated out automatically. Also the RC time constants for the analogue lowpass filters are automatically calibrated on chip.

Base-band interface

Unidirectional BlueRF compatible interface is used to control all functions of radio transceiver.

The unidirectional RXMODE2 is supported. STLC2150 has also the capability to provide the recovered clock and the aligned data to the base-band (Rxmode2+). 4 wires serial JTAG interface is used to access the internal registers. Also JTAG is used to set channel number and read RSSI.

Crystal oscillator

The STLC2150 has a crystal oscillator to generate 13 MHz reference clock for internal use and for the base-band chip.

Also a 3.2 or 32 kHz clock for low power modes operation can be provided.

GENERAL SPECIFICATION

All the provided values are specified over the operational conditions (VDD and temperature) according to the Bluetooth® v.1.2 specification.

Receiver

To comply with the Bluetooth® norm, an external RF filter is required to provide minimum 17dB of attenuation in the bands: 30MHz - 2000MHz and 3000MHz - 12.75GHz. All specification below are measured at the antenna port. The loss between IC inputs and the port is approximately 2dB

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
RFin	Input frequency range		2402		2480	MHz
RXsens	Receiver sensitivity (including dirty signal test)	@BER 0.1%		-77.5 [1]	-73.7 [2]	dBm
RXmax	Max input signal level	@BER 0.1%		>16		dBm
Receiver interference Performance @BER 0.1% [3]						
$C/I_{co\text{-}channel}$	Co-channel interference	@ Input signal strength = -60 dBm		10	11	dB
C/I_{1MHz}	Adjacent (1MHz) interference	@ Input signal strength = -60 dBm		-1	0	dB
C/I_{2MHz}	Adjacent (2MHz) interference	@ Input signal strength = -60 dBm		-36	-30	dB
$C/I_{\geq 3MHz}$	Adjacent (≥3MHz) interference	@ Input signal strength = -67 dBm		-50	-42	dB
C/I_{image}	Image interference	@ Input signal strength = -67 dBm		-25	-11	dB
$C/I_{image\pm 1MHz}$	Adjacent (1MHz) to image interference	@ Input signal strength = -67 dBm		-40	-28	dB
Receiver blocking @BER 0.1%						
RXB_1	30 MHz – 2000 MHz 3000 MHz – 12.75 GHz	@ input signal strength = -67 dBm			-10	dBm
RXB_2	2000 MHz – 2400 MHz 2500 MHz – 3000 MHz	@ input signal strength = -67dBm			-27	dBm
Receiver intermodulation						
RXIIP3	Input referred IP3	Interferers at –39 dBm, intended channel at –64 dBm, BER < 0.1%		-7.5	-11.5	dBm

1) Sensitivity at chip pins is -79.5 dBm.
2) Guarantied over process variation and full temperature range -40 to +85°C.
3) Without any exception.

RSSI Extraction

The RSSI extraction block allows to determine the Received Signal Strength. The indicator output is an 8-bit word, indicating the signal strength in dBm

Symbol	Parameter	Test condition / notes	Min	Typ	Max	Unit
RSSI_AC	RSSI accuracy	Signal power = -70 dBm		± 4		dB
RSSI_R	RSSI range	Range upwards from –70 dBm	20	40		dB
RSSI_RES	RSSI Resolution			0.37		dB/bit
RSSI_REF	RSSI reference point	signal power = -64 dBm		107		

The RSSI value is stored in the RSSI register. The value is latched when the base-band sends the access code recognition signal (BPKTCTL) and is kept unchanged until the next RX active slot. The register can be read by the base-band at any time

Transmitter

All output power specifications are given at the antenna port, with a bandpass filter and matching network in between the port and the IC. The loss between antenna port and IC output is approximately 2 dB

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
RFout	Output frequency range	Bluetooth® frequency band	2402		2480	MHz
TXPout	Nominal output power	@ 2402 – 2480 MHz	-6	0	+4	dBm
In-band spurious emission						
TX_SE1	Frequency offset = ±550kHz	Measured in a 100 kHz bandwidth		-26	-20	dBc
TX_SE2	Channel offset = 2			-51		dBm
TX_SE3	Channel offset ≥ 3			-62		dBm
Out-of-band spurious emission						
TX_SE4	Emission in the 30 MHz – 1 GHz band	Operation mode		-65		dBm
		Idle mode		-65		
TX_SE5	Emission in the 1 GHz – 12.75 GHz band	Operation mode		-58		dBm
		Idle mode		-65		
TX_SE6	Emission in the 1.8 GHz – 1.9 GHz band	Operation mode		-65		dBm
		Idle mode		-65		
TX_SE7	Emission in the 5.15 GHz – 5.3 GHz band	Operation mode		-65		dBm
		Idle mode		-65		

PLL

The centre frequency of the radio transmit or receive channel is controlled by a PLL. The selected radio channel centre frequency is given by:

$$Fc = 2.400GHz + n*1\ MHz,$$

where "n" is a 7-bit channel control word, ranging from 2 to 97

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Fref	External reference clock		-20ppm	13.000	+20ppm	MHz
VCOset	VCO settling time after power up	From Channel selection to LOCK = H		40	100	µs
Fd	Transmitter frequency drift			±100		Hz/µs

Crystal oscillator

An on-chip crystal oscillator provides a 13MHz master clock. The external crystal must be connected to the pads XTAL13I and XTAL13O.

The frequency specification of ±20 ppm can be achieved by 2 different ways:

1. by external components choice (default);
2. by internal tuning (with internal capacitors as defined by the control word stored in the registers.

The control word allows modifying the value of the capacitor connected to the oscillator pads. The total capacitance (including the parasitic capacitors) must be about 16 pF.

The variable capacitor is implemented as a capacitor array of about 255 x 90 fF.

External crystal example

Parameter	Value	Unit	tolerance	Comment
Frequency	13.000000	MHz	± 10 ppm	At 25 °C ± 3 °C
Mode	Fundamental			
Drive level	100	μW	± 20	
Temp drift	±10	ppm		Referred to value at 25°C over temperature range [1]
Aging	±1	Ppm/year	max	
Cload	16.0	pF	± 1 %	
Rseries	40	Ω	max	
C0	1.7	pF	± 20 %	Shunt capacitance
C1	6.5	pF	± 24 %	Motional capacitance
Rins	500	MΩ	min	Insulation resistance
Pull_sens	10	Ppm	± 20 %	(16 pF)
Activity Dips	± 0.5	Ppm / °C	max	Temperature range [1]

[1] Temperaure range is defined by application needs.

Low power clock

The STLC2150 can provide 3.2 or 32 KHz, low power clock for baseband chip operation in Hold, Snif and Park modes.

External reference frequency

The STLC2150 can take a digital clock from external source 13 MHz on the CLK13MHZ pin.

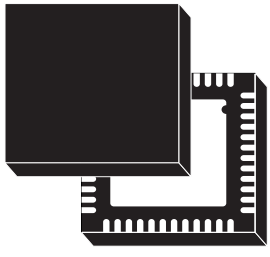
The IC also can use an analogue (sine wave, from 0.2 up to 1 Vpp) clock from external 13 MHz source on the XTAL13I pin.

Registers description

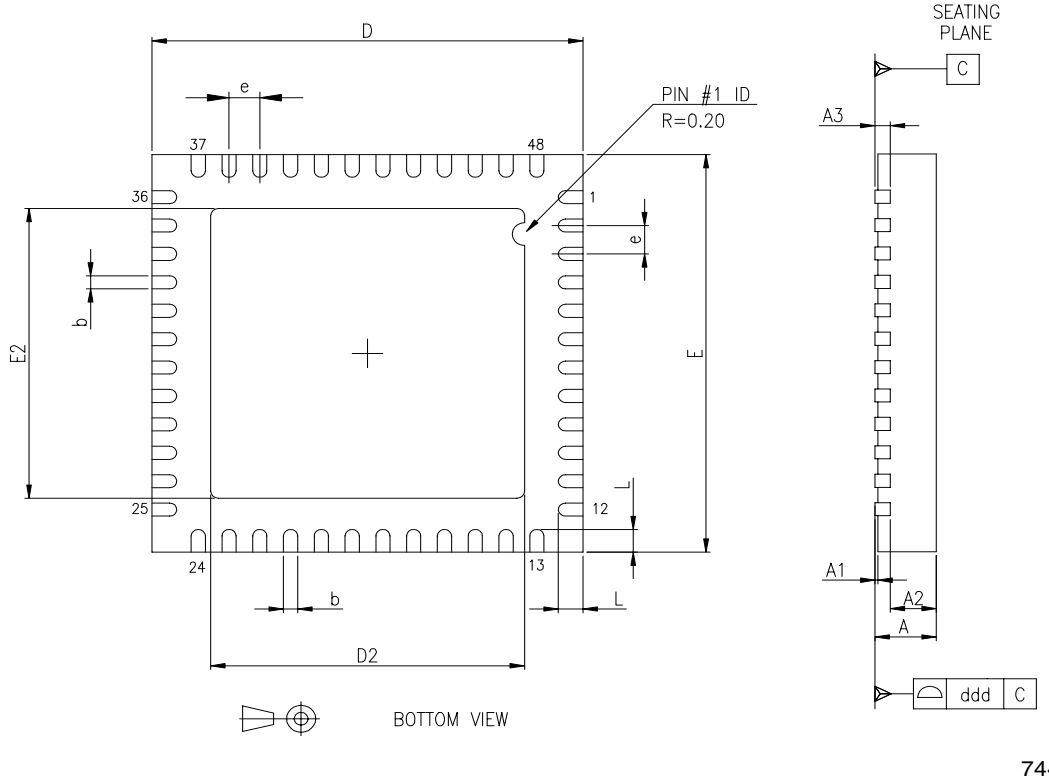
To provide operational control, configuration flexibility (e.g. clock configuration, XTAL trimming) and to set maximum performance the STLC2150 has a bank of registers. Detailed description is available in “STLC2150: Interface and Programming Guide”.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.800	0.900	1.000	0.031	0.035	0.039
A1		0.020	0.050		0.0008	0.0019
A2		0.650	1.000		0.025	0.039
A3		0.250			0.01	
b	0.180	0.230	0.300	0.007	0.009	0.012
D	6.850	7.000	7.150	0.269	0.275	0.281
D2	2.250	4.700	5.250	0.088	0.185	0.207
E	6.850	7.000	7.150	0.269	0.275	0.281
E2	2.250	4.700	5.250	0.088	0.185	0.207
e	0.450	0.500	0.550	0.018	0.020	0.022
L	0.300	0.400	0.500	0.012	0.016	0.020
ddd			0.080			0.003

OUTLINE AND MECHANICAL DATA



VFQFPN-48 (7x7x1.0mm)
Very **F**ine **Q**uad **F**lat **P**ackage **N**o lead



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