Application Note AN4141

Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

Introduction

This application note describes troubleshooting for problems that power supply engineers may encounter when operating FPS application circuits. This note helps engineers figure out causes and solutions to their problems starting with the symptoms. Some useful application tips are also provided. The following items are covered in this application note.

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Figure 1 shows the schematic of the basic off-line flyback converter using FPS, which also serves as the reference circuit for the troubleshooting described in this application note. It is also assumed that all the protection circuits within the FPS are in auto restart mode.

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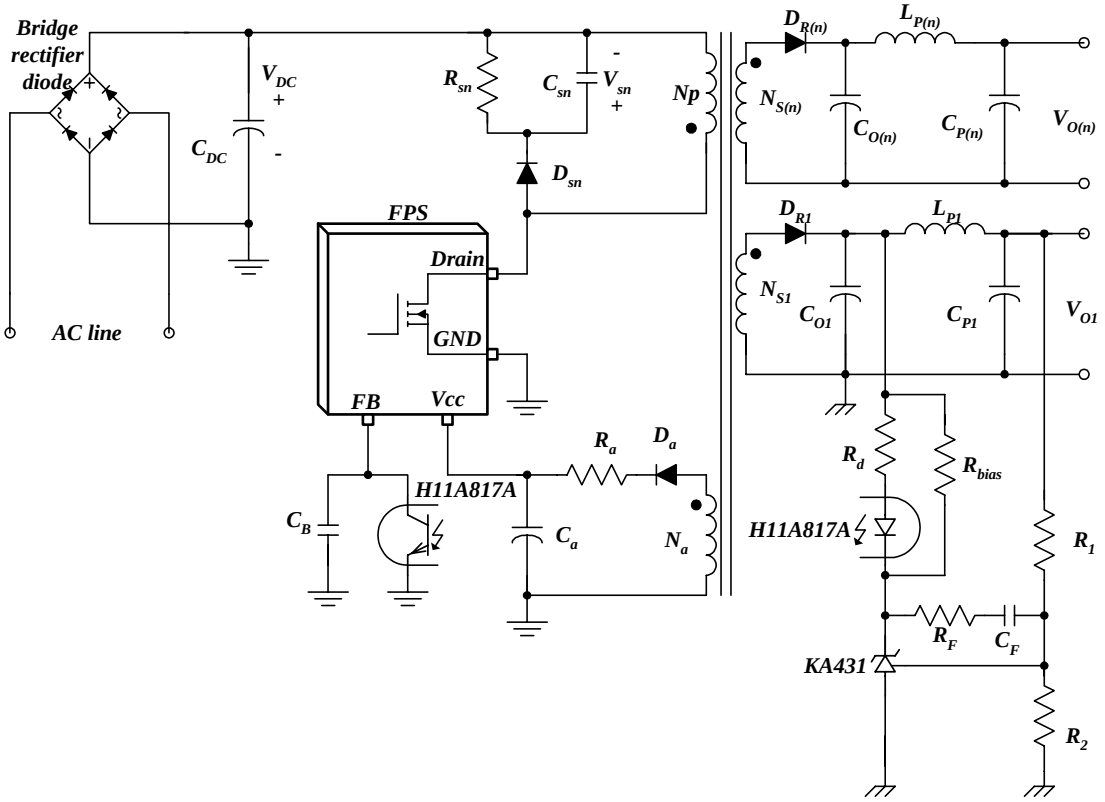


Figure 1. Basic Off-line Flyback Converter Using FPS

1. When the power supply does not start.

When, the converter does not startup, the first point to check is the Vcc voltage. The FPS is designed to begin switching operation when Vcc reaches its start voltage.

(a) Symptom : Vcc does not reach the Vcc start voltage.

- Check the startup circuit. In the case of the FPS requiring external startup circuit, too large a startup resistor may cause this situation.

- Check Vcc capacitor. Failure of the Vcc capacitor also can cause this phenomenon.

(b) Symptom : Vcc reaches Vcc stop voltage, consequently triggering a protection as shown in Figure 2.

- Check that the Vcc winding is connected to Vcc pin of the FPS through the rectifier diode.

- Too small a Vcc capacitor (C_a) may cause an Under voltage lockout during startup. Typical value for C_a is 10-50uF.

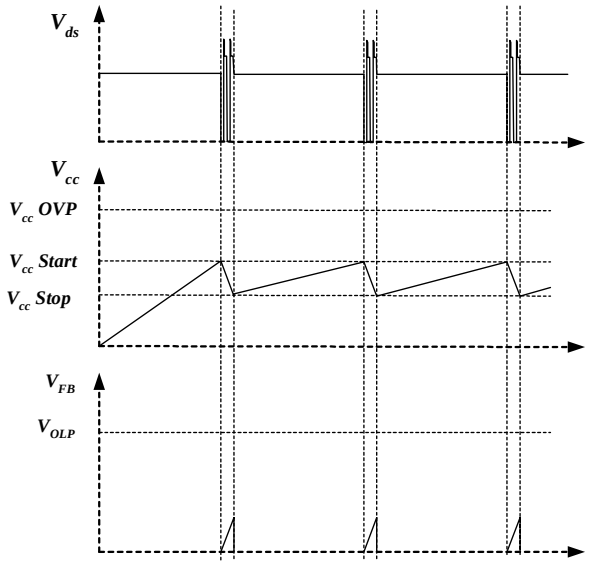


Figure 2. Under voltage Lock out protection

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(c) Symptom : Vcc reaches the Vcc OVP (over voltage protection) voltage, consequently triggering a protection as shown in Figure 3.

- Check that the number of turns for the Vcc winding is correct. It is typical to design Vcc to be around Vcc start voltage (Refer to the data sheet).

- Usually Vcc increases as the load currents of other outputs increase due to the imperfect coupling of the transformer. When the Vcc winding is poorly coupled with output windings, Vcc may reach OVP level. In this case, increase the damping resistor (Ra) that is in series with the Vcc diode. The typical value for R_a is 5-20Ω.

- Check the polarity of Vcc winding. If the polarity of the Vcc winding is reversed, the Vcc voltage might be larger than the designed value.

- When the opto-coupler, output capacitor or rectifier diode fails, OVP can be triggered.

- In the case of multiple outputs, OVP can be triggered when one of the outputs is very lightly loaded or unloaded while other outputs are heavily loaded.

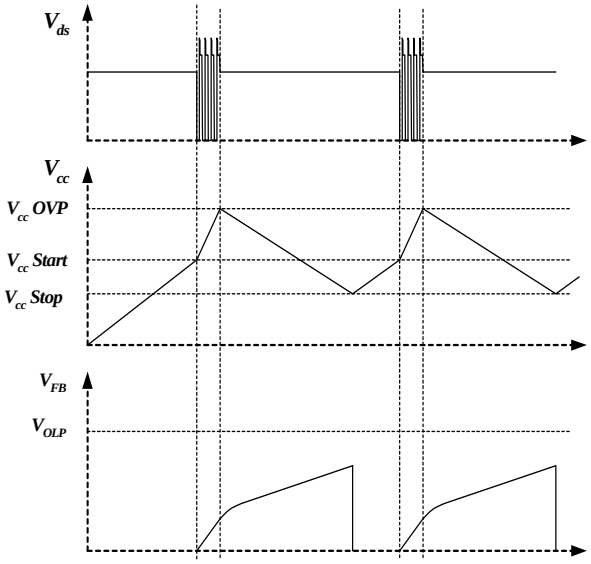


Figure 3. Vcc OVP protection

(c) Symptom : V_{FB} reaches the OLP (over load protection) level, consequently triggering a protection as shown in Figure 4.

- Too small a feedback capacitor (C_B) may cause a OLP during startup. Typical value for C_B is 10-50nF.

- The failure of output capacitor can cause OLP.

- Too large an opto LED series resistor (Rd) may cause OLP. Rd should be designed to guarantee the full swing of the feedback voltage for the FPS device. For detailed design equations, refer to AN4137.

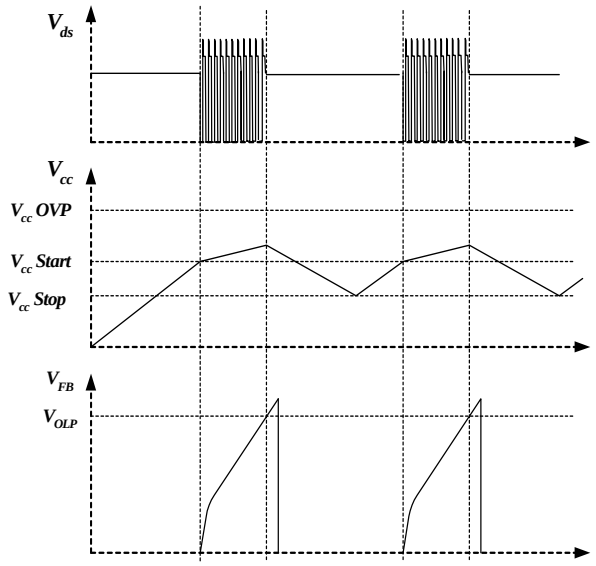


Figure 4. The Over load protection

2. When the power supply is unstable.

First of all, check if the converter is really stable or not. In many cases, an auto restart operation triggered by a protection circuit, as shown in Figure 2, 3 and 4, is misunderstood as unstable operation. Sometimes, 120Hz ripple of the feedback voltage due to the line frequency, as shown in Figure 5, is also misunderstood as unstable operation.

The best way to check the instability is to monitor the feedback capacitor. When the feedback voltage oscillates with other than 120Hz and its waveforms are different from those in Figure 2, 3 and 4, it can be considered legitimately unstable. The real waveforms of an unstable converter are shown in Figure 6 where the feedback voltage oscillates with a frequency different from 120Hz.

The instability is usually caused by insufficient gain/phase margin of the feedback loop. For a detailed design process of the feedback loop, refer to AN4137. Usually the following actions reduce the feedback gain, consequently making the system stable.

- Increase the opto LED series resistor (Rd).

- Increase the resistors (R_1 and R_2) in the voltage divider network of the feedback circuit while keeping R1/R2 constant.

- Sometimes, the post LC filter in the output makes the system unstable by introducing a low frequency pole to the system transfer function. Check if the resonant frequency of the post LC filter is below 1kHz. If so then, reduce the capacitor of the post LC filter.

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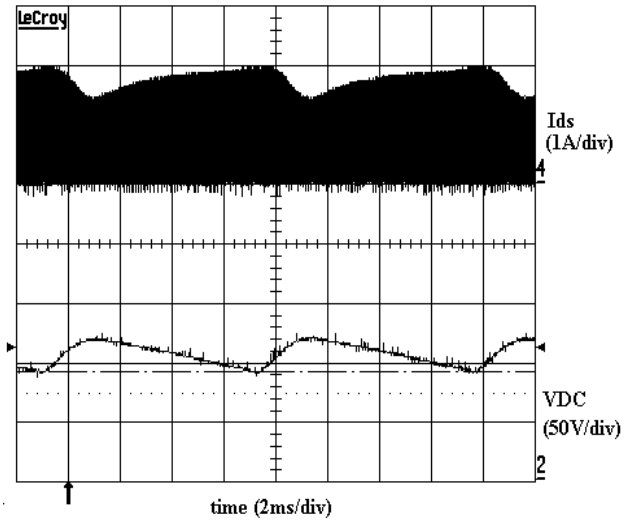


Figure 5. Effect of 120Hz ripple

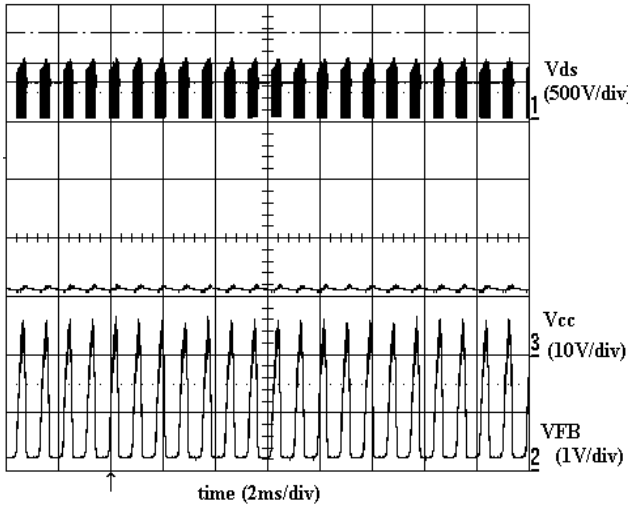


Figure 6. Unstable system

3. When there is a transient overshoot in the output voltage.

- Check if the feedback loop has sufficient phase margin.

- If overshoot occurs only during startup, add an external soft-start circuit in the feedback network as show in Figure 7. This circuit removes the output voltage overshoot by slowly increasing the current through the opto LED.

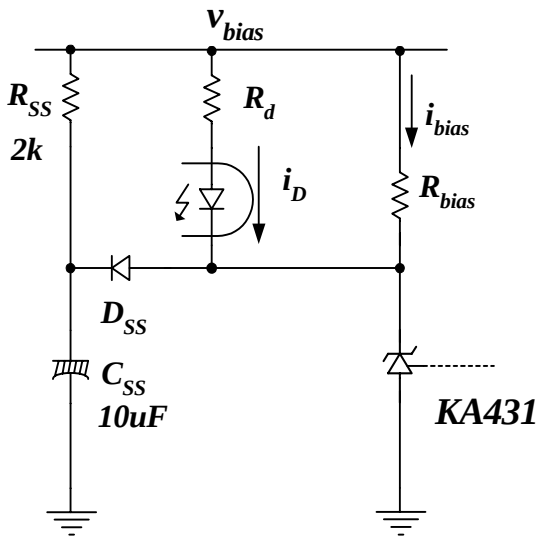


Figure 7. External soft-start circuit

4. When the peak drain voltage exceeds the rated voltage.

Figure 8 shows a typical MOSFET drain voltage waveform for the universal input application. Many customers make it a rule to keep the maximum drain voltage under 80% of the BVdss of the MOSFET. When the maximum drain voltage in normal operation exceeds its specification, reduce the snubber capacitor voltage (Vsn) by reducing the reflected output voltage (V_{RO}). V_{RO} can be reduced by decreasing the primary side turns with other winding turns fixed. Because this increases the voltage stress in the secondary side diodes, the voltage stresses on the secondary side diodes should be checked again. The snubber capacitor voltage can be also reduced by decreasing the snubber resistor. However, this method has a limitation, since it increases the loss in the snubber network. It is typical to set the snubber capacitor voltage to be around twice the reflected output voltage as shown in Figure 8. For detailed design equations, refer to the application note AN4137. If the drain voltage exceeds its specification only when it starts up, use the soft-start circuit in Figure 7.

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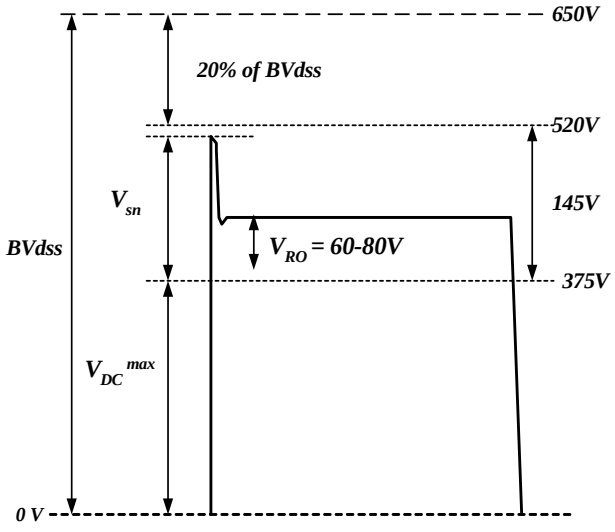


Figure 8. Drain voltage

5. When sub-harmonic oscillation occurs.

Most FPS employ current mode control except for the low power FPS for battery charger applications. In the case of the current mode controlled FPS, sub-harmonic oscillation occurs when the duty cycle exceeds 50% in continuous conduction mode (CCM) operation as shown in Figure 9. When sub-harmonic oscillation occurs, the converter can become unstable or generate audible noise. In that case, the followings should be checked.

- Check if the converter is over loaded.

- Check if the maximum duty ratio is set too large. If this is the case , reduce the primary to secondary turn ratio (Np/Ns).

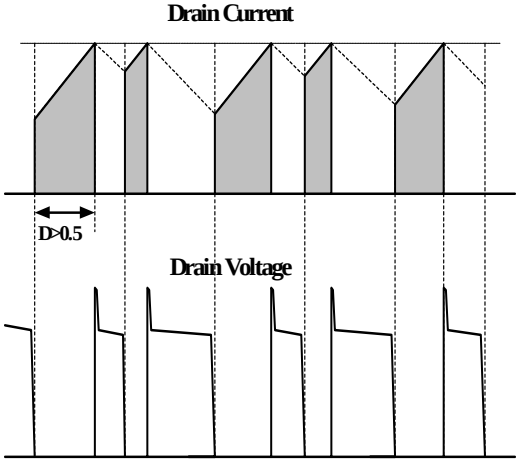


Figure 9. Sub-harmonic oscillation

In the case of a 650V rated FPS application with a universal input, the maximum duty ratio is typically designed as below 50%. However, for 100V input voltage applications, a duty ratio larger than 50% is required to minimize the conduction loss of the MOSFET and the voltage stress on the secondary side diode. In that case, a slope compensation circuit shown in Figure 10 can be used.

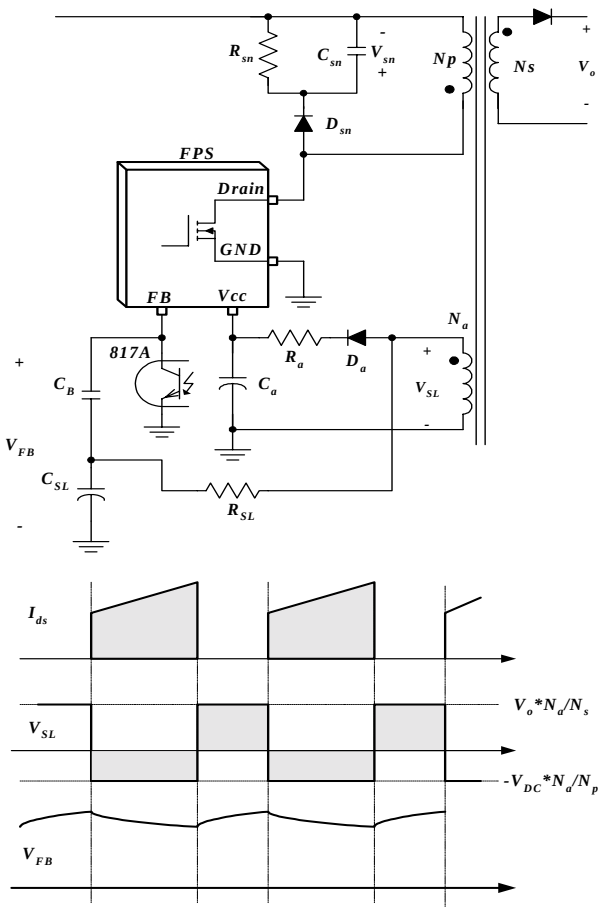


Figure 10. Slope compensation circuit

6. When the line frequency ripple on the output voltage is too large.

- Too low a bandwidth in the feedback loop can cause this problem. Increase the opto LED series resistor (Rd) or the resistors (R1 and R2) in the voltage divider network to increase the bandwidth.

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7. When the power conversion efficiency is too low.

- Check if the snubber capacitor voltage is too low. It is typical to set the snubber capacitor voltage to be about twice of the reflected output voltage. By increasing the snubber resistor, the capacitor voltage can be increased.

- When the efficiency at the minimum input voltage is too low, the efficiency can be improved by increasing the DC link capacitor (C_{DC}) or by increasing the inductance of the transformer.

8. When audible noise occurs

Even though the switching frequency of FPS is above the range of human hearing, audible noise can be generated during transient or burst operation. In most flyback converters, the major noise sources are the transformers and capacitors.

(a) Transformer audible noise

Transformers can produce audible noise, since it contains many physically movable elements, such as coils, isolation tape and bobbins. The current in the coil produces electro-magnetic fields and therefore generates repulsive and/or attractive forces between coils. This can produce a physical vibration in the coils, ferrite cores or isolation tapes.

The most effective way to reduce the audible noise in the transformer is to remove the possibility of physical movement of the transformer elements by using adhesive material or by varnishing.

(b) Capacitor audible noise

Ceramic capacitors can also produce audible noise, since they have piezoelectric characteristics. If there is still too much audible noise in burst operation, after gluing or varnishing the transformer properly, the capacitor in the snubber network should be examined.

By replacing the ceramic capacitor with a film capacitor, the audible noise can be reduced. Another way is to reduce the snubber capacitor value, which decreases the pulse current that charges the capacitor every time the FPS resumes switching operation in burst mode as shown in Figure 11.

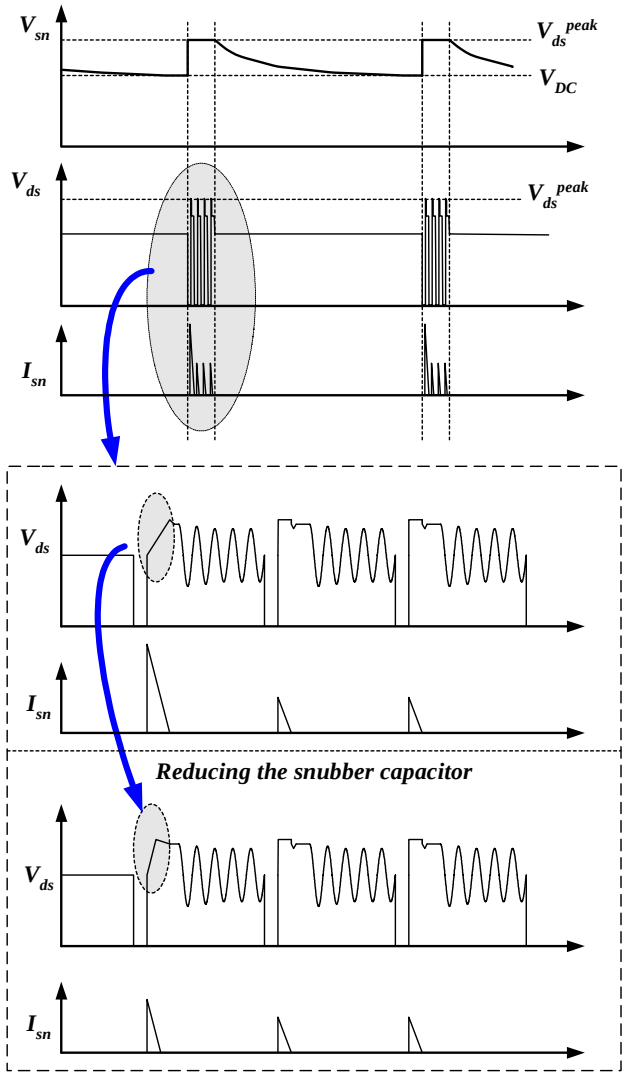


Figure 11. Audible noise reduction by reducing the snubber capacitor

9. PCB layout consideration

Figure 12 shows the typical layout for FPS application. The layout should be done to minimize the switching noise in the Vcc pin and feedback pin. Signal ground should be connected directly to the GND pin of FPS without sharing the trace with the power ground. The Vcc capacitor (C_a) and feedback capacitor (C_B) should be placed as close to FPS as possible to minimize noise. The cathode of snubber diode should be close to the drain pin of FPS to minimize the stray inductance. The Y-capacitor (C_Y) should be connected directly to the ground of the DC link capacitor (C_{DC}) to maximize the surge immunity.

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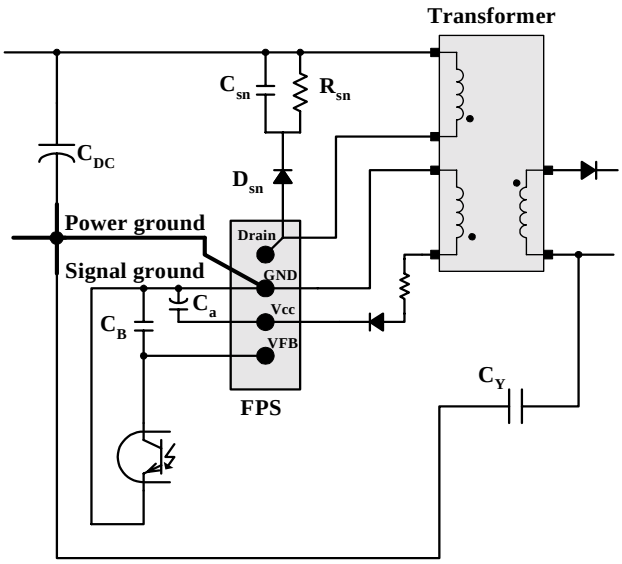


Figure 12. Typical PCB layout

10. Application circuit for delayed shutdown in an overload protection.

In order to avoid premature triggering of over load protection (OLP) during transient, FPS employs delayed shutdown. When the feedback voltage (V_{FB}) reaches 2.7V, V_{FB} is clamped inside of FPS and delay current (I_{delay}) charges the feedback capacitor (C_B). The shutdown delay time is given by the time required to charge C_B from 2.7V to OLP threshold. The shutdown delay time can be extended by increasing C_B. However, too large a feedback capacitor can limit the control loop bandwidth.

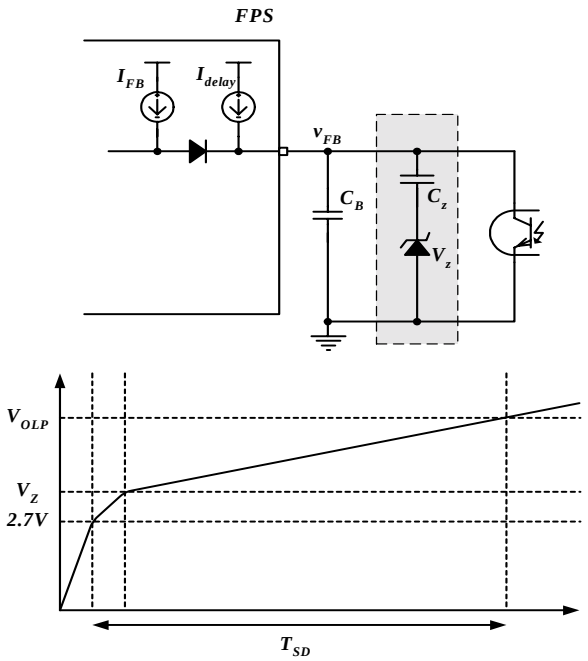


Figure 13. Delayed shutdown

Application circuit to extend the shutdown time without limiting the control bandwidth is shown in Figure 13. By setting the zener breakdown voltage (Vz) slightly higher than 2.7V, the additional delay capacitor (Cz) is isolated from the feedback circuit in normal operation. When the feedback voltage exceeds the zener breakdown voltage (Vz), Cz together with C_B determine the shutdown time.

11. Application circuit for multiple output with a very tight output regulation

When it comes to multiple output applications, the output with the most tight regulation requirement is used for the feedback control and other outputs are determined by the transformer turns ratio. With this conventional approach, it is difficult to precisely regulate more than two outputs at the same time. If more than two outputs require a very tight regulation, regulate the highest current output with a feedback control and other outputs with a linear regulator as shown in Figure 14. If the output current is smaller than 1A, standard linear regulator such as KA7805 can be used. If the output current is larger than 1A and the output voltage is not standard, linear regulator circuit with discrete component should be used.

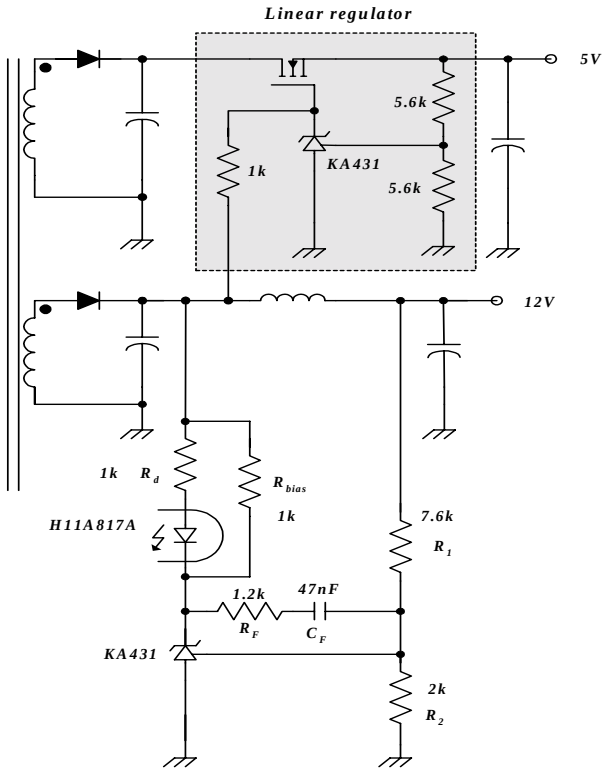


Figure 14. Linear regulator circuit for tight regulation

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12. Application circuit to convert auto-restart mode into latch mode

These days, most protections in FPS are implemented in auto-restart mode. However, in some applications, latch mode protection is preferred rather than auto restart mode protection. In that case, auto restart mode can be converted into latch mode using the application circuit of Figure 15 which shows latch mode over load protection. Once the feedback voltage (VFB) exceeds the zener breakdown voltage, the latch circuit is triggered and pull down the Vcc voltage. Then, the FPS remains off until Vcc capacitor (Ca) is fully discharged by the power off.

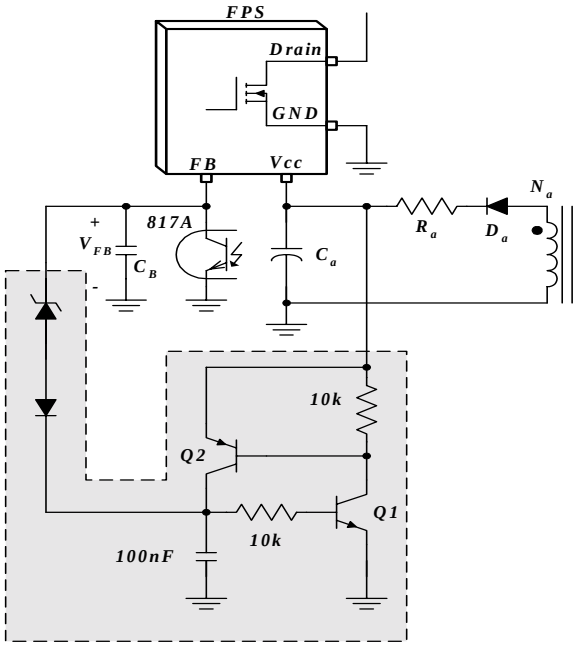


Figure 15. Latch mode protection circuit

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