M62354P/FP/GP

8-bit 6ch D/A Converter with Buffer Amplifiers

REJ03D0872-0300
Rev.3.00
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Description

The M62354 is an integrated circuit semiconductor of CMOS structured with 6 channels of built-in D/A converters with output buffer operational amplifiers.

The 3-wire serial interface method is used for the transfer format of digital data to allow connection with microcomputer with minimum wiring.

It is able to cascading serial use with DO terminal.

The output buffer operational amplifier operates in the whole voltage range from power supply to ground for both input/output.

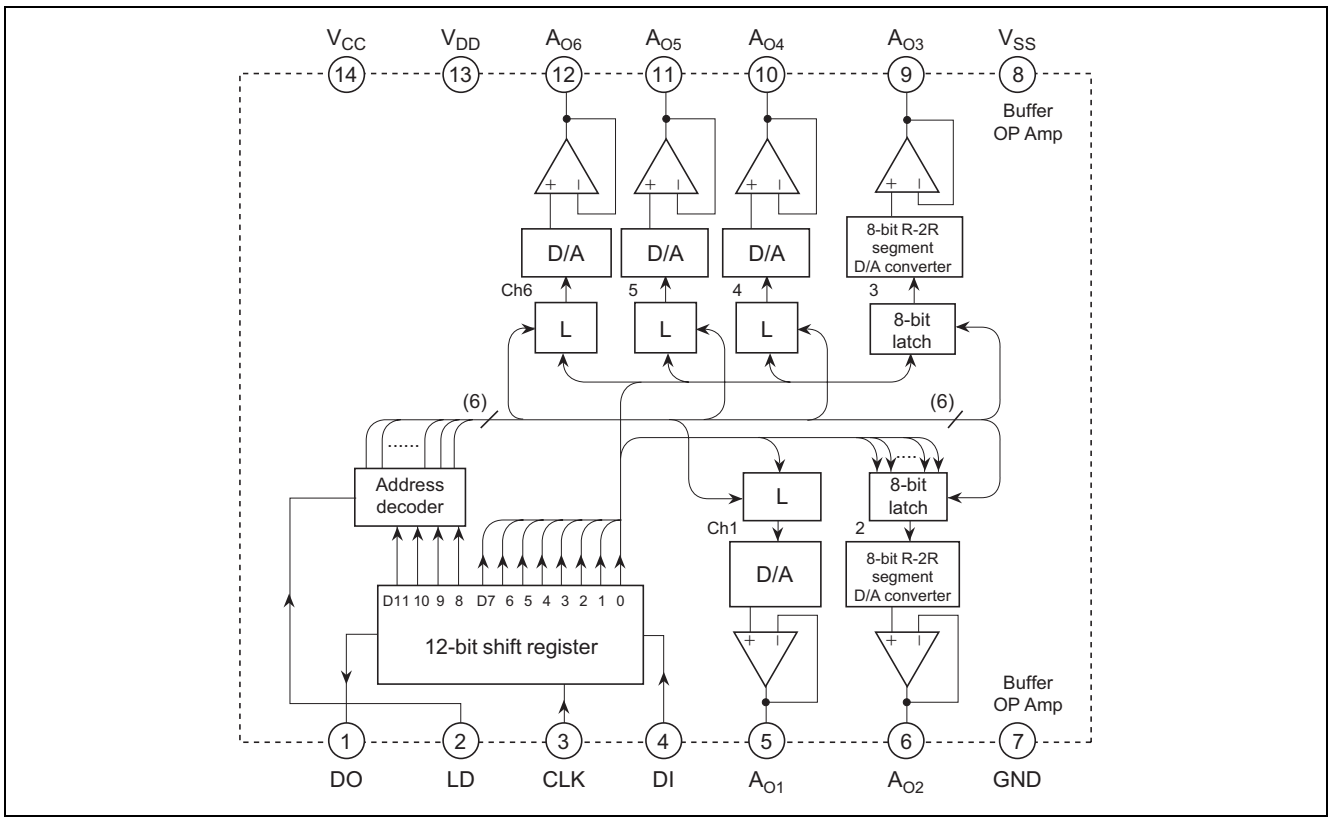
Features

- 12-bit serial data input (3-wire serial data transfer method)
- Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.

Application

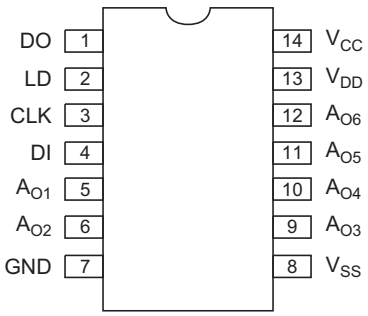
Adjustment/control of industrial or home-use electronic equipment, such as VTR camera, VTR set, TV, and CRT display.

Block Diagram



Pin Arrangement

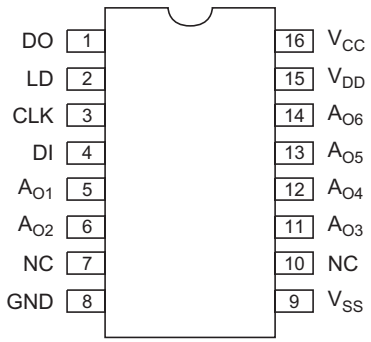
M62354P/FP



(Top view)

Outline: 14P4
PRSP0014DD-A (14P2N-A)

M62354GP



NC: No connection

(Top view)

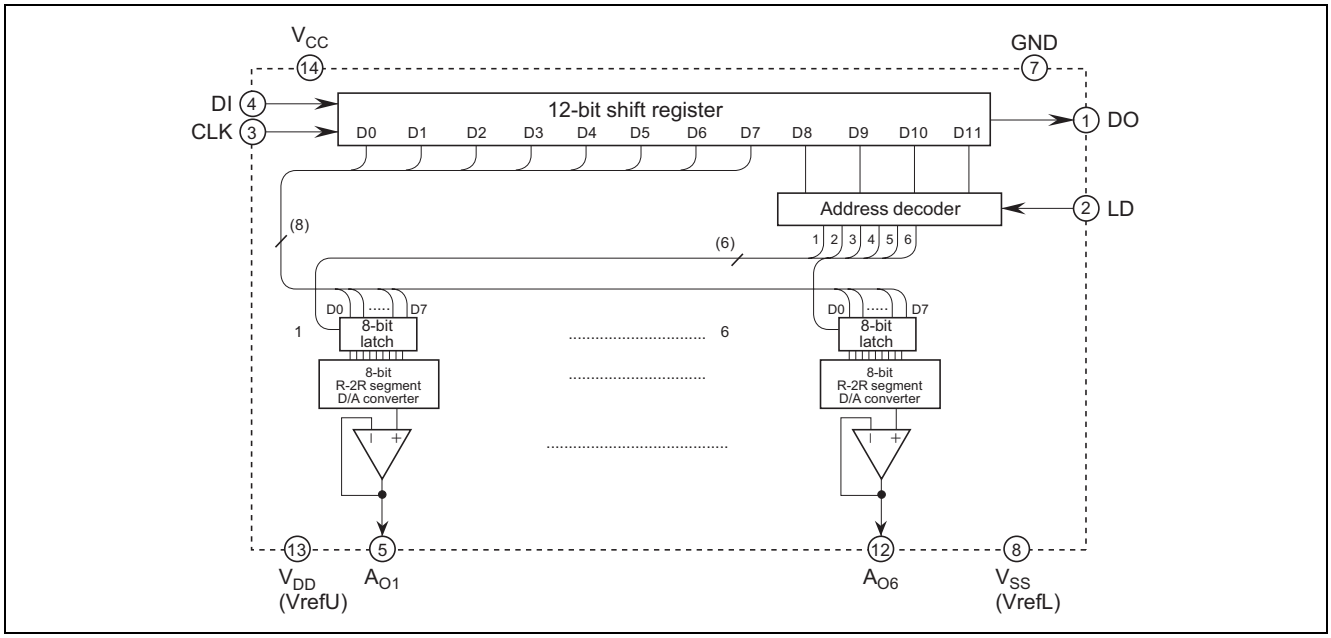
Outline: PLSP0016JA-A (16P2E-A)

Pin Description

Pin No.	Pin Name	Function
4 (4)	DI	Serial data input terminal
1 (1)	DO	Serial data output terminal
3 (3)	CLK	Serial clock input terminal
2 (2)	LD	LD terminal input high level then latch circuit data load
5 (5)	A_{O1}	8-bit D/A converter output terminal
6 (6)	A_{O2}	
9 (11)	A_{O3}	
10 (12)	A_{O4}	
11 (13)	A_{O5}	
12 (14)	A_{O6}	
14 (16)	V_{CC}	Power supply terminal
7 (8)	GND	Digital and analog common GND
13 (15)	V_{DD}	D/A converter upper reference voltage input terminal
8 (9)	V_{SS}	D/A converter lower reference voltage input terminal

Note: ( ) : M62354GP

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
D/A converter upper reference voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
Power dissipation	Pd	440 (P) / 250 (FP) / 150 (GP)	mW
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–40 to +125	°C

Electrical Characteristics

<Digital Part>

(V_{CC}, VrefU = 5 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Circuit current	I_{CC}	—	0.7	2.5	mA	CLK = 1 MHz operation V_{CC} = 5 V, I_{AO} = 0 μA
Input leak current	I_{ILK}	–10	—	10	μA	V_{IN} = 0 to V_{CC}
Input low voltage	V_{IL}	—	—	0.2 V_{CC}	V	
Input high voltage	V_{IH}	0.8 V_{CC}	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 μA

<Analog Part>

(V_{CC}, VrefU = 5 V ± 10%, V_{CC} ≥ VrefU, Ta = –20 to +85°C, unless otherwise noted.)

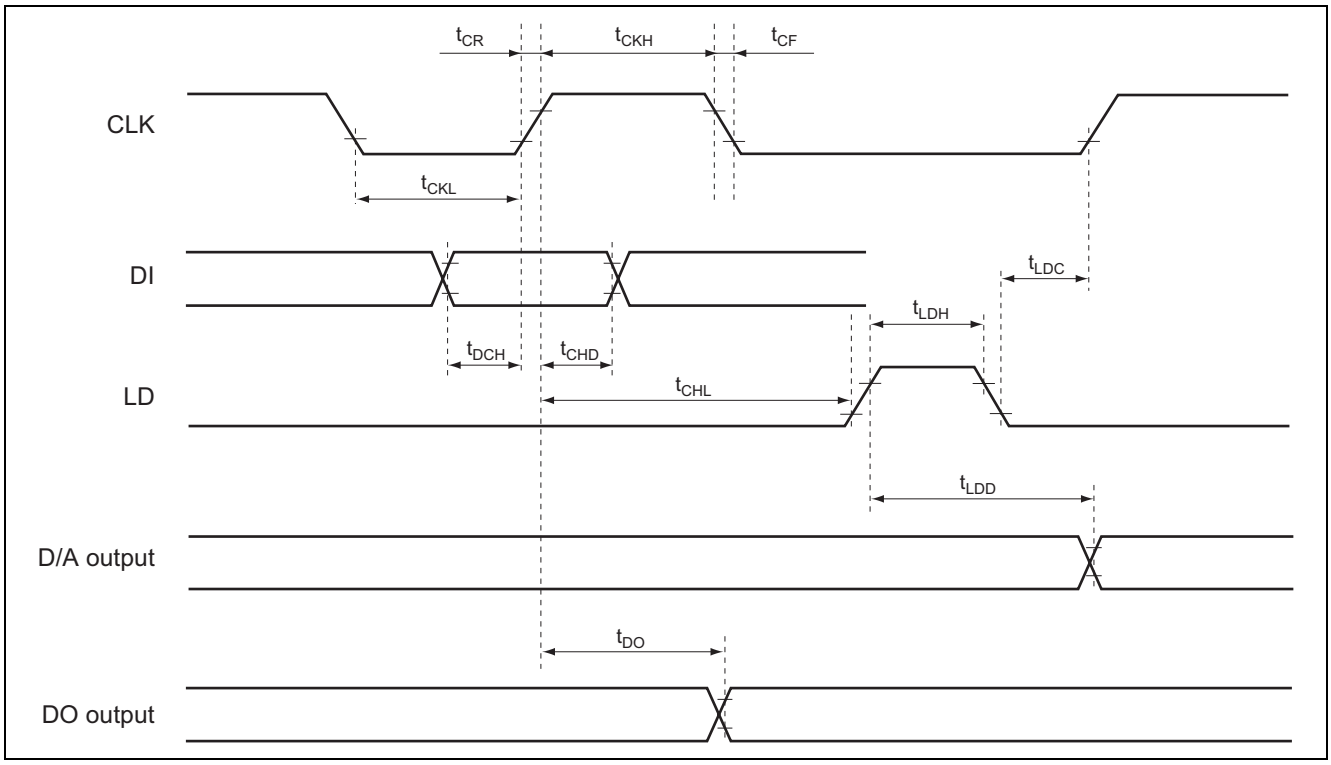
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current dissipation	I_{DD}	—	0.7	1.3	mA	VrefU = 5 V, VrefL = 0 V Data condition: at maximum current
D/A converter upper reference voltage range	V_{DD}	3.5	—	V_{CC}	V	The output does not necessarily be the value within the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range (V_{AO}).
D/A converter lower reference voltage range	V_{SS}	GND	—	V_{CC} – 3.5	V	
Buffer amplifier output voltage range	V_{AO}	0.1	—	V_{CC} – 0.1	V	I_{AO} = ± 100 μA
		0.2	—	V_{CC} – 0.2		I_{AO} = ± 500 μA
Buffer amplifier output drive range	I_{AO}	–1	—	1	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity error	S_{DL}	–1.0	—	1.0	LSB	VrefU = 4.79 V VrefL = 0.95 V V_{CC} = 5.5 V (15 mV/LSB) Without load (I_{AO} = ±0 μA)
Nonlinearity error	S_L	–1.5	—	1.5	LSB	
Zero code error	S_{ZERO}	–2	—	2	LSB	
Full scale error	S_{FULL}	–2	—	2	LSB	
Output capacitive load	C_O	—	—	0.1	μF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

AC Characteristics

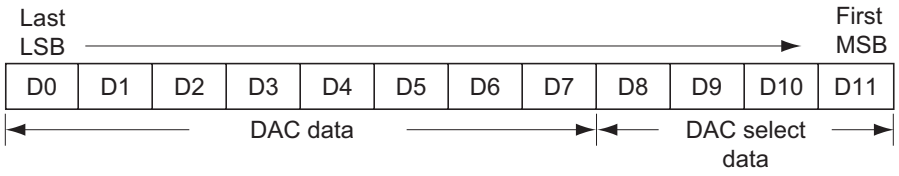
(V_{CC}, VrefU = 5 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" pulse width	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	C_L ≤ 100 pF
D/A output setting time	t_{LDD}	—	—	300	µs	C_L ≤ 100 pF, V_{AO}: 0.5 ↔ 4.5 V The time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format



DAC Data

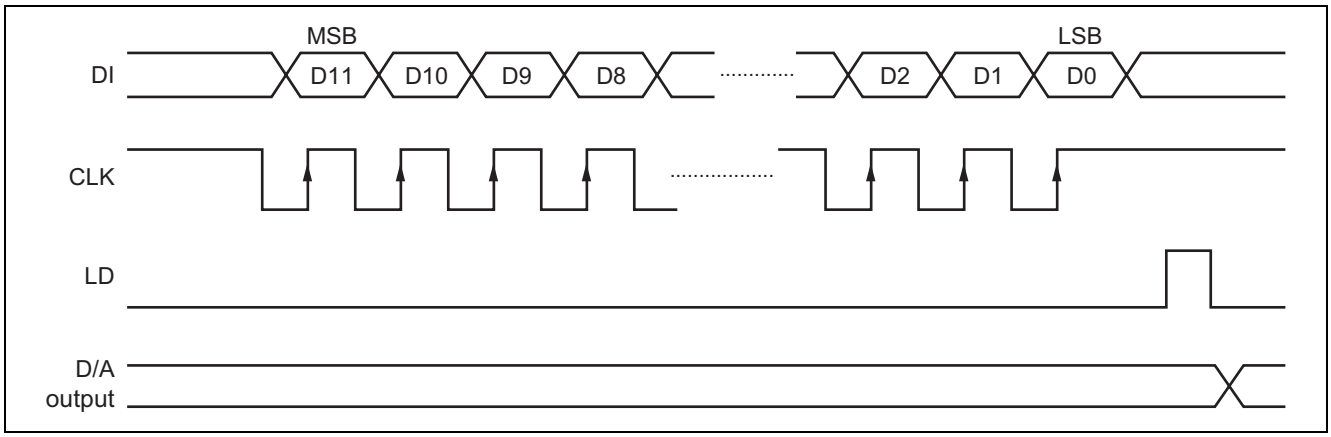
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 1 + VrefL
1	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 2 + VrefL
0	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 3 + VrefL
1	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 4 + VrefL
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	(VrefU – VrefL) / 256 × 255 + VrefL
1	1	1	1	1	1	1	1	VrefU

Note: VrefU = V_{DD}, VrefL = V_{SS}

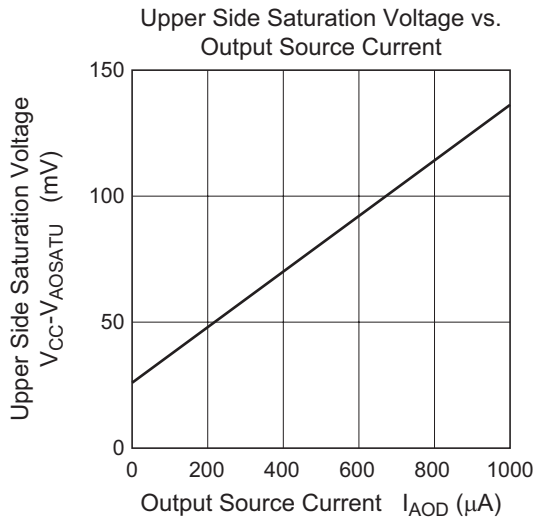
DAC Select Data

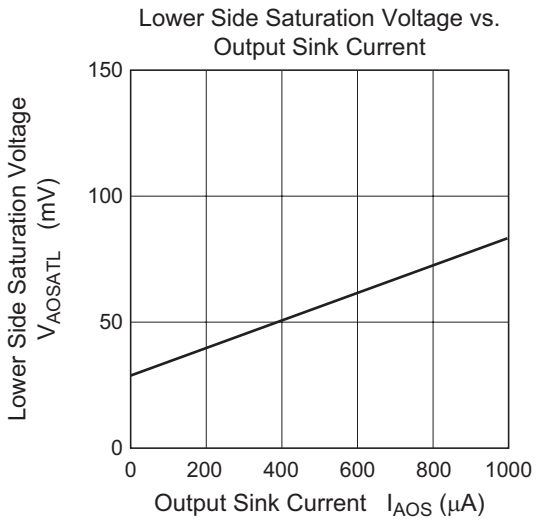
D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	A_{O1} selection
0	0	1	0	A_{O2} selection
0	0	1	1	A_{O3} selection
0	1	0	0	A_{O4} selection
0	1	0	1	A_{O5} selection
0	1	1	0	A_{O6} selection
0	1	1	1	Don't care
1	0	0	0	Don't care
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



Typical Characteristics



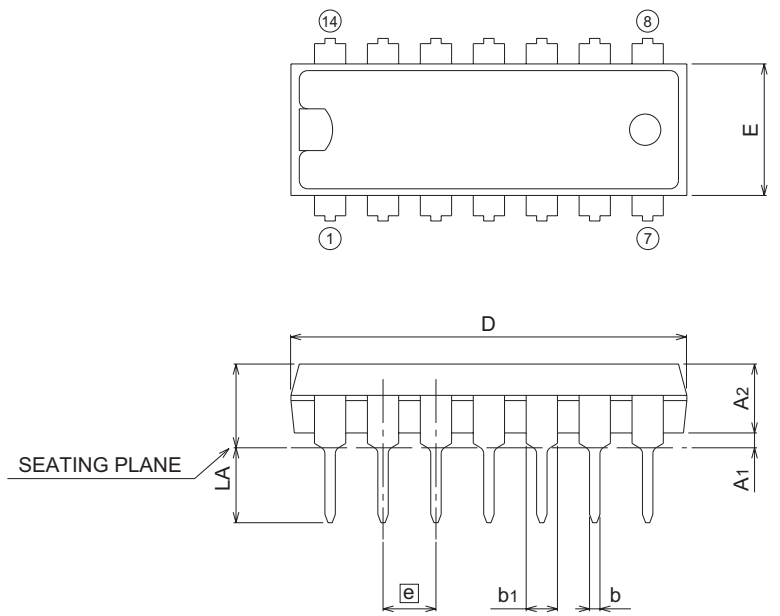


Package Dimensions

14P4

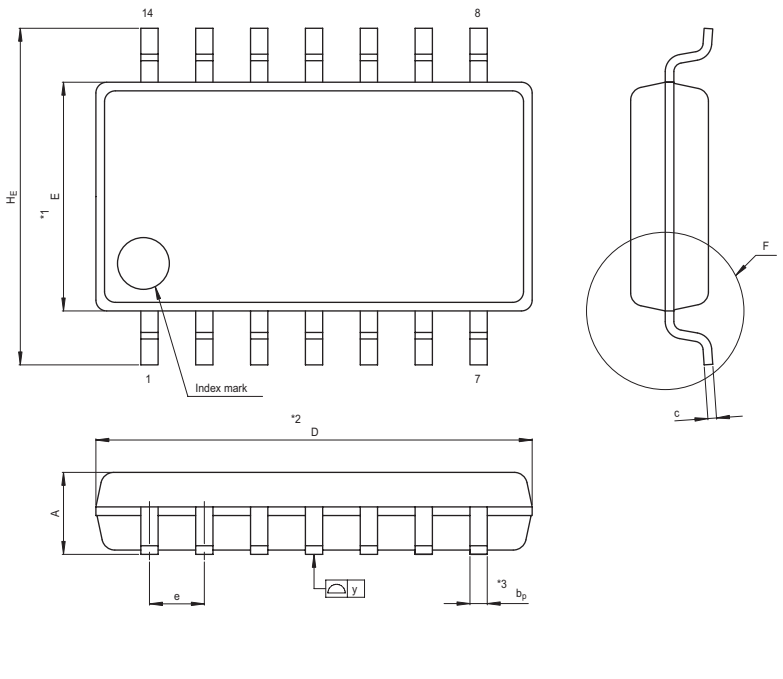
Plastic 14pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
DIP14-P-300-2.54	—	1.0	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.4	0.5	0.6
b1	1.4	1.5	1.8
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	2.54	—
e1	—	7.62	—
L	3.0	—	
θ	0°	—	15°

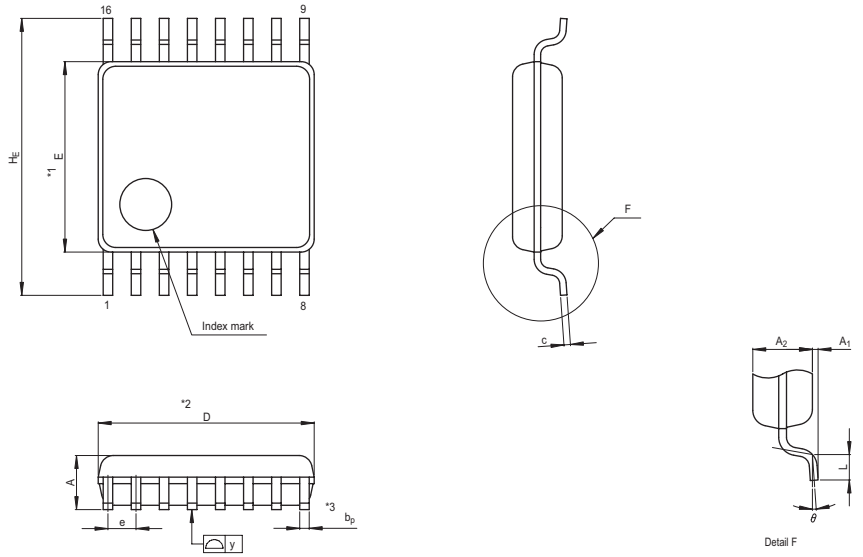
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.3x10.1-1.27	PRSP0014DD-A	14P2N-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP16-4.4x5-0.65	PLSP0016JA-A	16P2E-A	0.06g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

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Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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