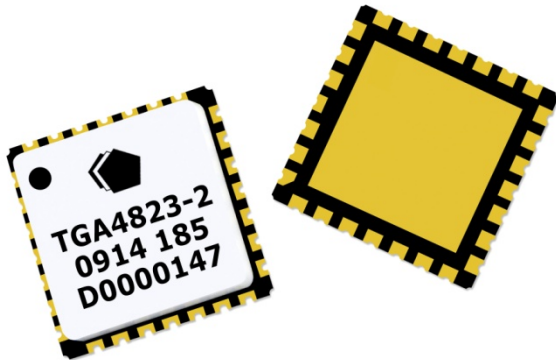


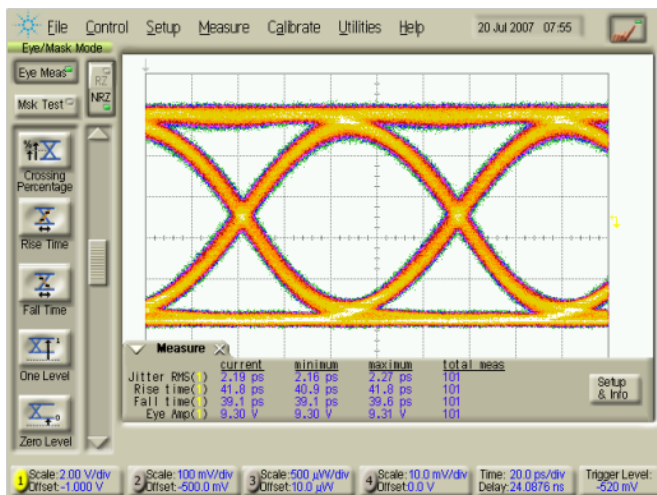
## 9.9 - 12.5 Gb/s Linear/Limiting Optical Modulator Driver



### Measured Performance

Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  
 $V_g \approx -0.3\text{ V}$  Typical

PRBS =  $2^{31}-1$ ; CPC = 50%, 10.7 GB/s;  $V_{in} = 1\text{Vpp}$



### Key Features

- Up to 10 Vpp Linear Output Voltage
- > 12 Vpp Limiting Mode Output Voltage
- Gain: 19 dB
- Integrated High Frequency Bias Tee
- Internal DC blocks
- Single-ended Input / Output
- Bias:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  
 $V_g = -0.3\text{ V}$  Typical for Linear operation
- Package Dimensions: 8 x 8 x 2.1 mm

### Primary Applications

- Mach-Zehnder Modulator Driver for Metro and Long Haul

### Product Description

The TriQuint TGA4823-2-SM is part of a series of optical driver amplifiers suitable for a variety of driver applications.

The TGA4823-2-SM is a high power wideband AGC amplifier that typically provides 19 dB small signal gain with 19 dB AGC range.

The TGA4823-2-SM is an excellent choice for applications requiring high drive combined with high linearity. The TGA4823-2-SM has demonstrated capability to deliver 10Vpp while maintaining output harmonic levels near -30dBc for a 2GHz fundamental.

The TGA4823-2-SM requires a low frequency choke and control circuitry.

RoHS compliant and Lead-Free finish. MSL1 per IPC/JEDEC J-STD-020C . Evaluation boards available on request.

**Table I**  
**Absolute Maximum Ratings 1/**

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	12 V	
Vd	Drain Voltage	9 V	2/
Vg	Gate Voltage Range	-5 to 0 V	2/
Vctrl	Control Voltage Range	-1 to +2 V	2/
Id	Drain Current	400 mA	2/
Ig	Gate Current Range	-1.8 to 18.9 mA	
Ictrl	Control Current Range	-1.8 to 18.9 mA	
Pin	Input Continuous Wave Power	27.8 dBm	
Tchannel	Channel Temperature	200 °C	2/

- 1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

**Table II**  
**Recommended Linear Operating Conditions**

Symbol	Parameter 1/	Value
Vd	Drain Voltage	8 V
Id	Drain Current	310 mA
Id_Drive	Drain Current under RF Drive	350 mA
Vg	Typical Gate Voltage	-0.3 V
Vctrl	Control Voltage	1 V

- 1/ See assembly diagram for bias instructions.

**RF Characterization Table**

 Bias:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g = -0.3\text{ V}$ , typical

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOMINAL	MAX	UNITS
Gain	Small Signal Gain	$f = 1.5 - 2.5\text{ GHz}$	18.5	20	23	dB
		$f = 0.1 - 4\text{ GHz}$	-	20	-	
		$f = 6\text{ GHz}$	-	19	-	
		$f = 8\text{ GHz}$	-	18	-	
3dB BW	Small Signal 3 dB Bandwidth <u>1/</u>	$f = 0.1 - 12\text{ GHz}$	7.5	9.5	-	GHz
IRL	Input Return Loss	$f = 0.1 - 7\text{ GHz}$	-	15	-	dB
		$f = 7.1 - 10\text{ GHz}$	-	15	-	
		$f = 10.1 - 16\text{ GHz}$	-	9	-	
ORL	Output Return Loss	$f = 0.1 - 4\text{ GHz}$	-	15	-	dB
		$f = 4.1 - 7\text{ GHz}$	-	15	-	
		$f = 7.1 - 11\text{ GHz}$	-	15	-	
		$f = 11.1 - 16\text{ GHz}$	-	12	-	
Gain Ripple	S21 peak-peak gain variation <u>2/</u>	$f = 0.1 - 0.5\text{ GHz}$	-0.8		0.8	dB
		$f = 0.6 - 5\text{ GHz}$	-1.2		1.2	
		$f = 5.1 - 10\text{ GHz}$	-3		3	
DLP	Deviation from S21 Linear Phase	$f = 2 - 10\text{ GHz}$	-40	+/- 30	40	deg
		$f = 10.1 - 15\text{ GHz}$	-175	+/- 150	175	
P2	2 <sup>nd</sup> Harmonic	$f = 0.5, 2.0, 5.0\text{ GHz}$ $P_{out} = 22\text{ dBm}$	-	-	-22	dBc
P3	3 <sup>rd</sup> Harmonic	$f = 0.5, 2.0, 5.0\text{ GHz}$ $P_{out} = 22\text{ dBm}$	-	-	-26	dBc
Psat	Saturated Output Power	$f = 2\text{ GHz}$	-	26 (12.5)	-	dBm (Vpp)
P1dB	Output Power @ 1dB Compression	$f = 2\text{ GHz}$	-	25	-	dBm
AGC Range	Small Signal AGC Range		-	19	-	dB

1/ Fit the S21 curve to 4<sup>th</sup> order polynomial. Assign Ave gain = |S21| measured between 1.5 and 2.5 GHz. Determine 3dB point from polynomial fit to S21 curve.

2/ Ripple calculation is defined the difference between measured S21 value (dB) and a 4<sup>th</sup> order (or less) polynomial fit for S21 (dB) for frequency range = 0.1 to 12 GHz.

## Table IV Power Dissipation and Thermal Properties

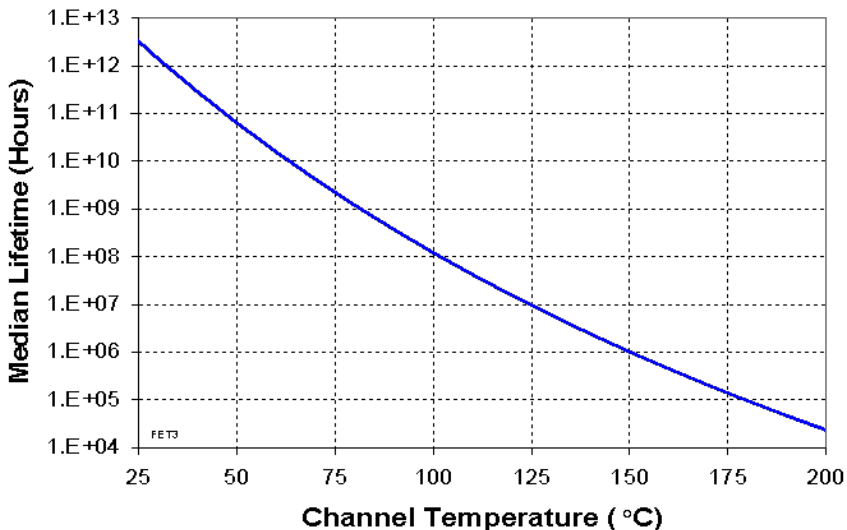
Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 70 °C	Pd = 3.17 W Tchannel = 150 °C Tm = 1.0E+6 Hrs	<u>1/2/</u>
Thermal Resistance, $\theta_{jc}$	Vd = 8 V Id = 310 mA Pd = 2.48 W	$\theta_{jc}$ = 24.3 (°C/W) Tchannel = 130 °C Tm = 5.8E+6 Hrs	
Thermal Resistance, $\theta_{jc}$ Under RF Drive	Vd = 8 V Id = 350 mA Pout = 26.5 dBm Pd = 2.36 W	$\theta_{jc}$ = 24.3 (°C/W) Tchannel = 127 °C Tm = 7.6E+6 Hrs	
Mounting Temperature		Refer to Solder Reflow Profiles (pp16)	
Storage Temperature		-65 to 150 °C	

1/ For a median life of 1E+6 hours, Power Dissipation is limited to  

$$Pd(max) = (150\text{ °C} - Tbase\text{ °C})/\theta_{jc}.$$

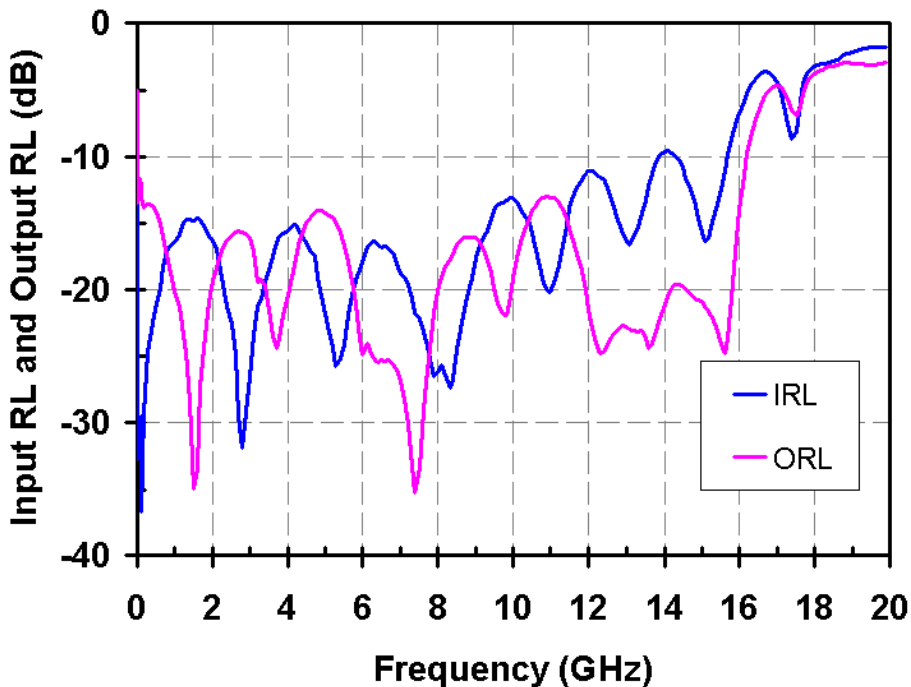
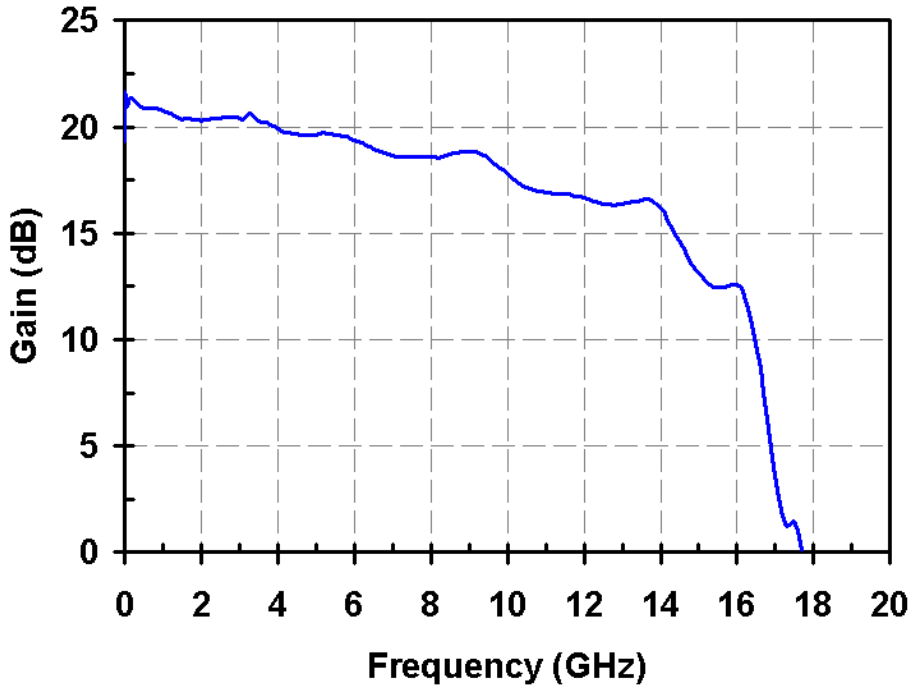
2/ Channel operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

### Median Lifetime (Tm) vs. Channel Temperature



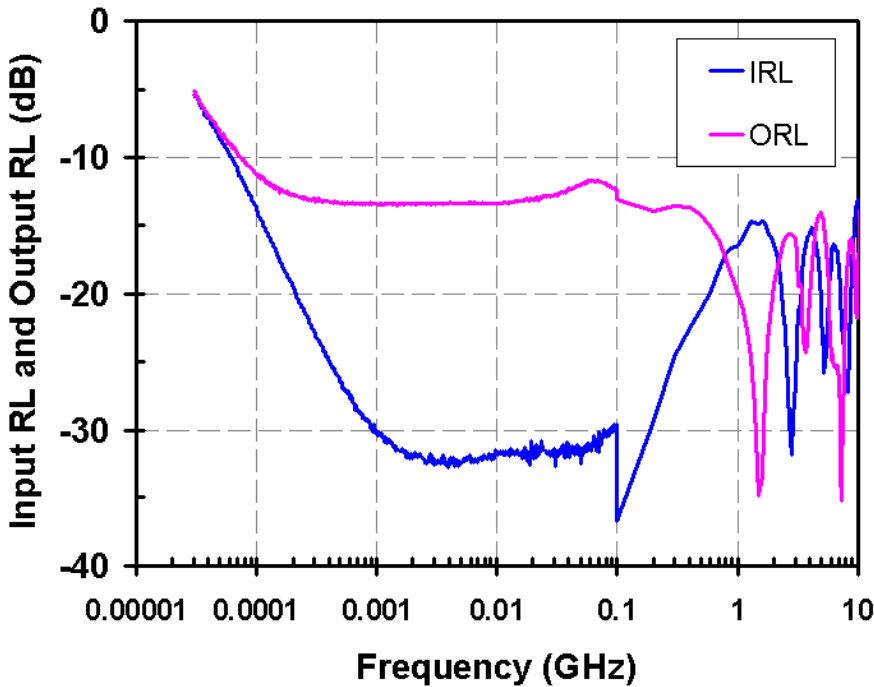
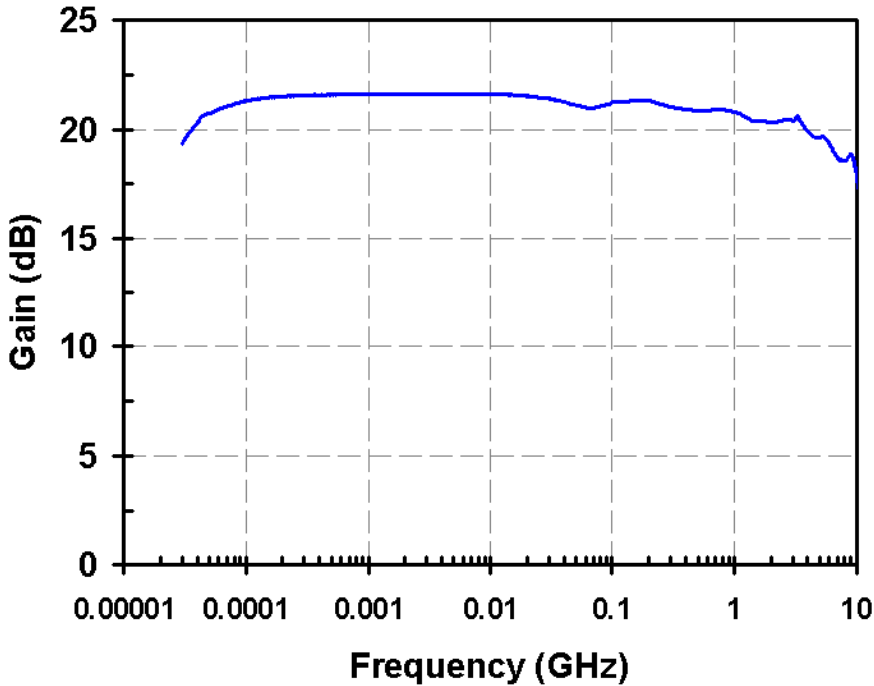
**Measured Data**

Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g \approx -0.3\text{ V}$  Typical



**Measured Data**

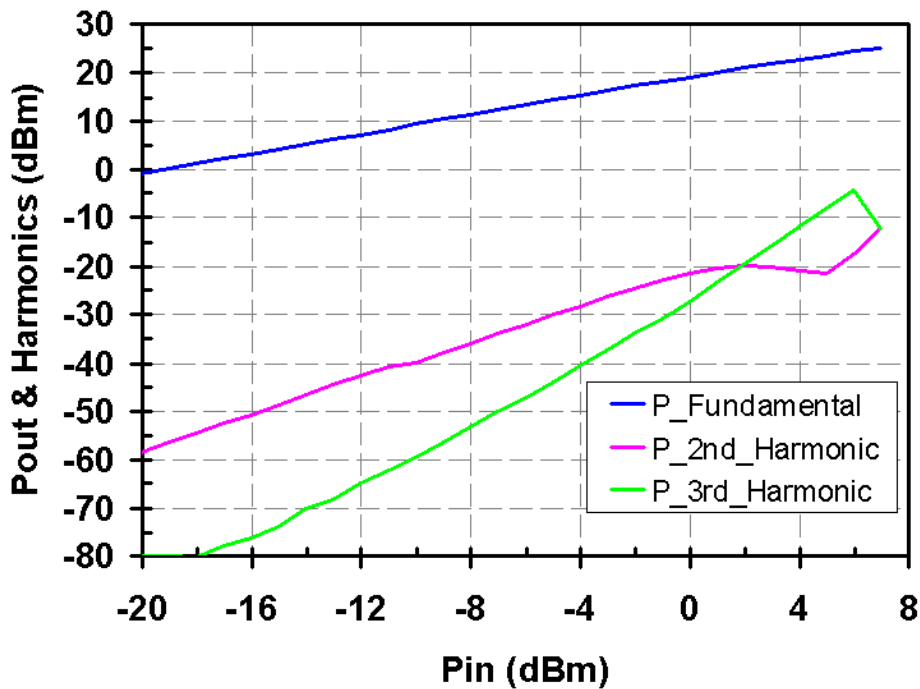
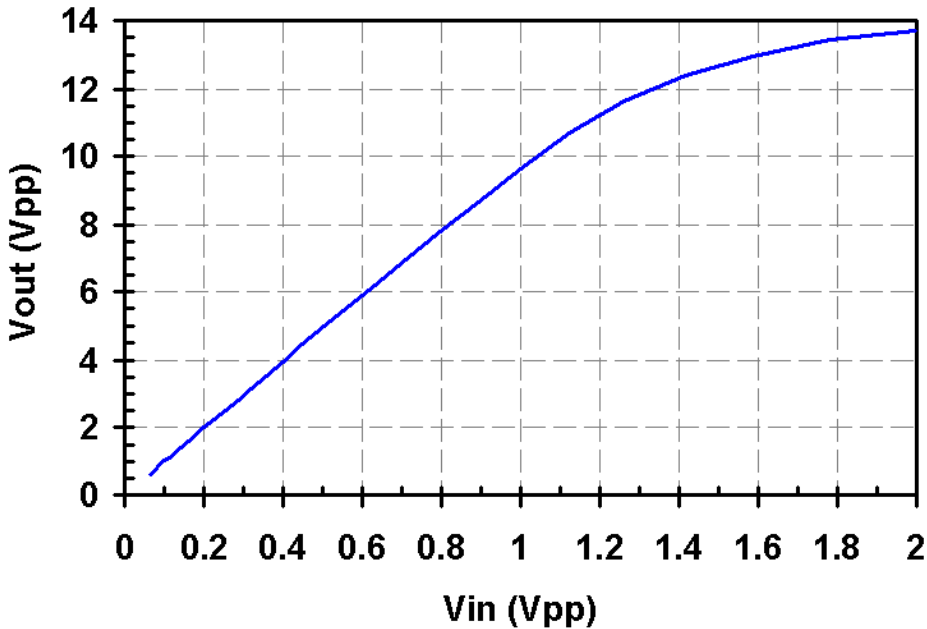
Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g \approx -0.3\text{ V}$  Typical



**Measured Data**

Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g \approx -0.3\text{ V}$  Typical

Freq = 2 GHz

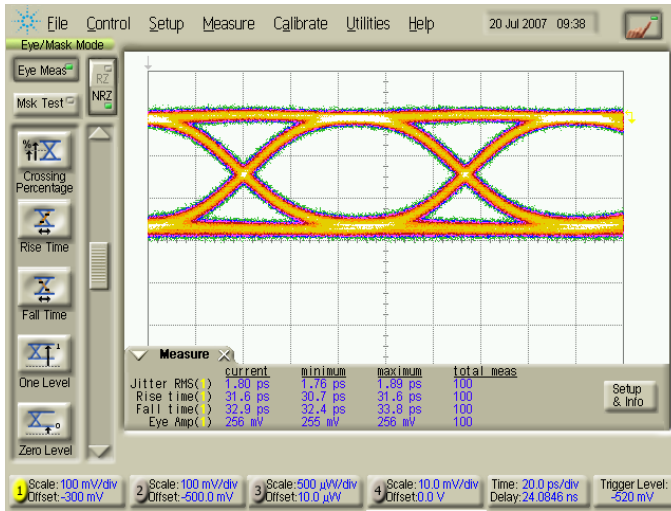


**Measured Data**

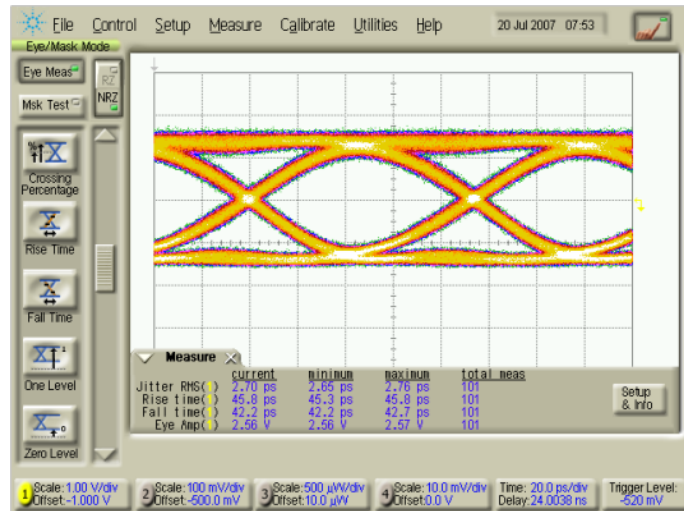
**Linear Mode:**

**Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g \approx -0.3\text{ V}$  Typical**

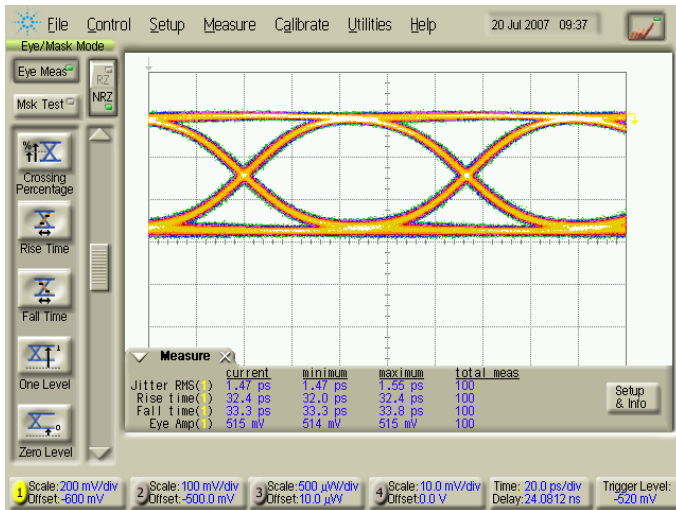
**PRBS =  $2^{31}-1$ ; CPC = 50%, 10.7 GB/s**



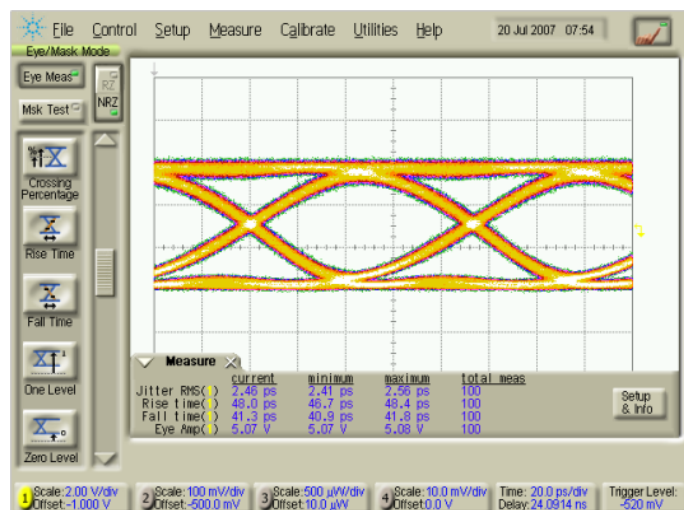
**Input Eye:  $V_{in} = 250\text{ mV}_{pp}$**



**Output Eye:  $V_{in} = 250\text{ mV}_{pp}$ ,  $V_{o_{pp}} = 2.5\text{ V}_{pp}$**



**Input Eye:  $V_{in} = 500\text{ mV}_{pp}$**



**Output Eye:  $V_{in} = 500\text{ mV}_{pp}$ ,  $V_{o_{pp}} = 5\text{ V}_{pp}$**

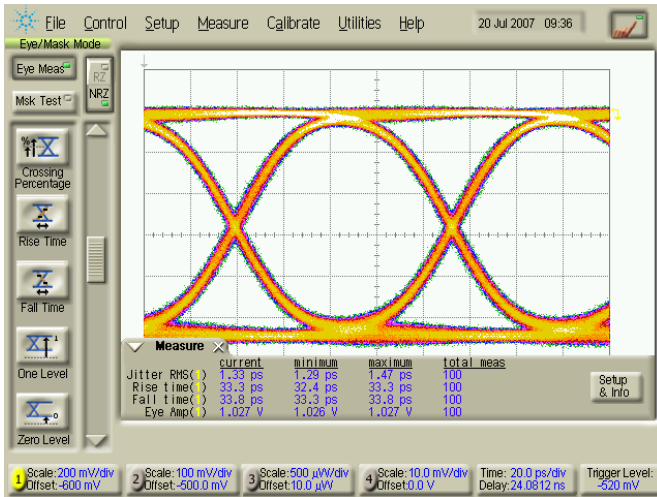


**Measured Data**

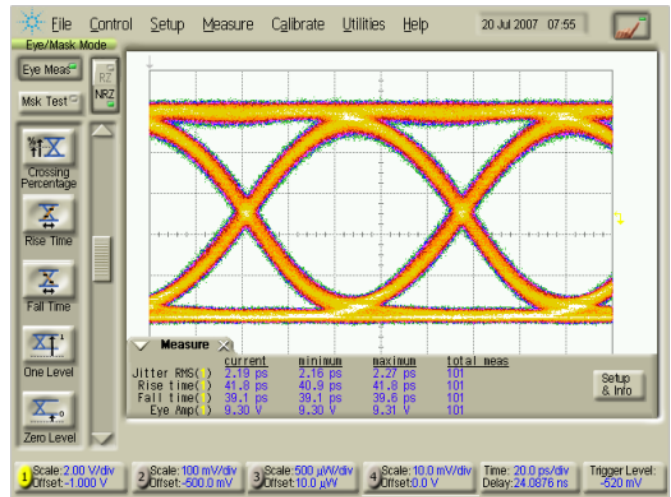
**Linear Mode:**

**Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g \approx -0.3\text{ V}$  Typical**

**PRBS =  $2^{31}-1$ ; CPC = 50%, 10.7 GB/s**



**Input Eye:  $V_{in} = 1\text{ V}_{pp}$**



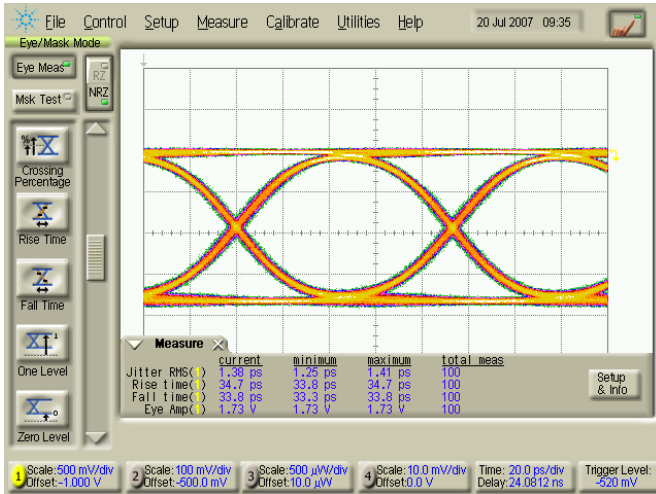
**Output Eye:  $V_{in} = 1\text{ V}_{pp}$ ,  $V_{o_{pp}} = 9.3\text{ V}_{pp}$**

## Measured Data

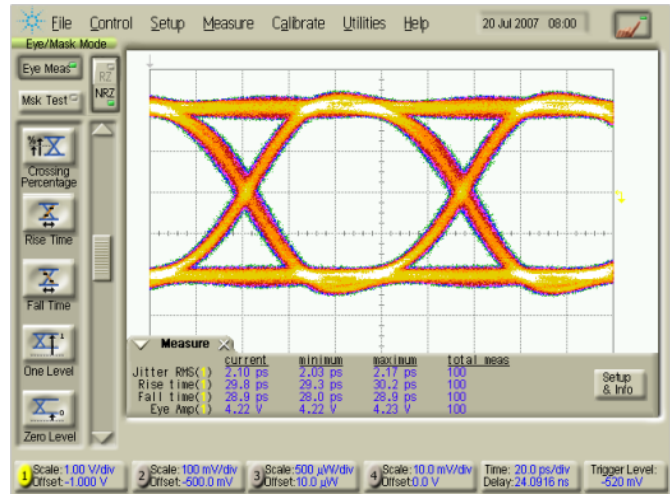
Limiting Mode:

Bias conditions:  $V_d = 8\text{ V}$ ,  $I_d = 310\text{ mA}$ ,  $V_{ctrl} = +1\text{ V}$ ,  $V_g \approx -0.3\text{ V}$  Typical

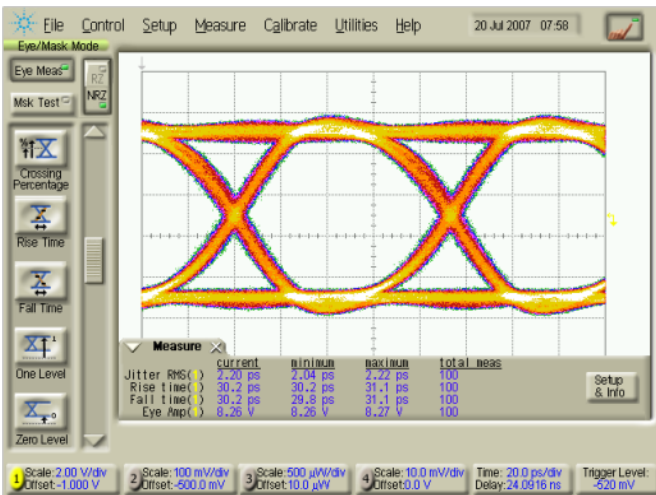
PRBS =  $2^{31}-1$ ; CPC = 50%, 10.7 GB/s



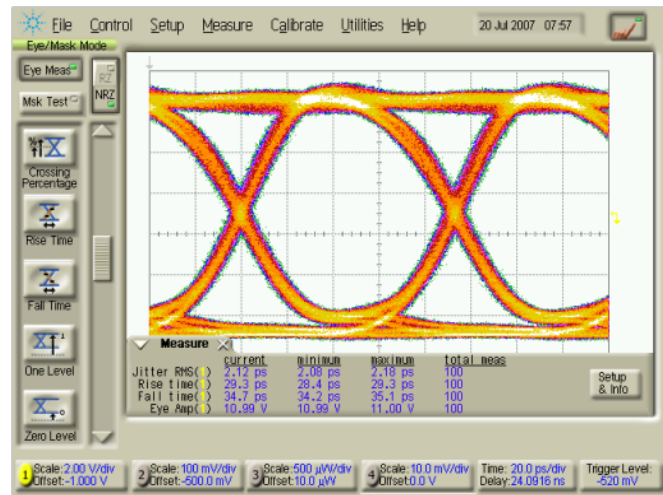
Input Eye:  $V_{in} = 1700\text{ mV}_{pp}$



Output Eye:  $V_{in} = 1700\text{ V}_{pp}$ ,  $V_{o_{pp}} = 4.2\text{ V}_{pp}$

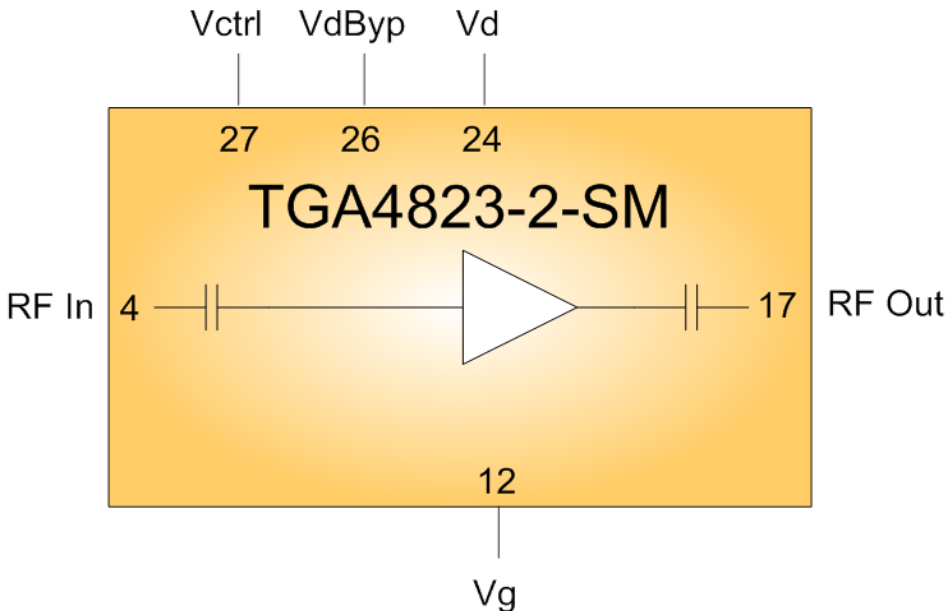


Output Eye:  $V_{in} = 1700\text{ V}_{pp}$ ,  $V_{o_{pp}} = 8.3\text{ V}_{pp}$



Output Eye:  $V_{in} = 1700\text{ V}_{pp}$ ,  $V_{o_{pp}} = 11\text{ V}_{pp}$

**Electrical Schematic**



**Bias Procedures**

**Vd=8V, CPC=50%**

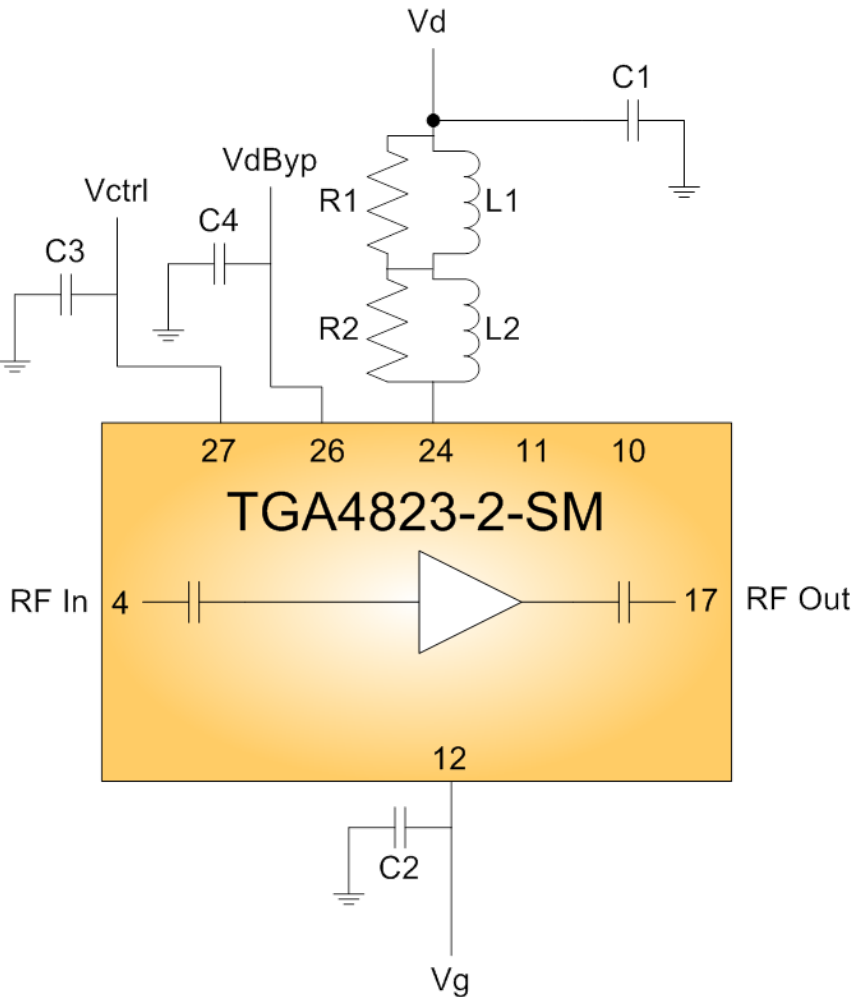
**Bias ON**

1. Disable the output of the PPG
2. Set Vd = 0V, Vctrl = 0V & Vg = 0V
3. Set Vg = -1.5V
4. Increase Vd to 8V observing Id  
- Assure Id = 0mA
5. Set Vctrl = +1V  
- Id should still be 0mA
6. Make Vg more positive until Id = 310mA.  
Vg will be approximately -0.3V.
7. Enable the output of the PPG.
8. Output Swing Adjust: Adjust Vctrl slightly positive to increase output swing or adjust Vctrl slightly negative to decrease the output swing.
9. Crossover Adjust: Adjust Vg slightly positive to push the crossover down or adjust Vg slightly negative to push the crossover up.

**Bias OFF**

1. Disable the output of the PPG
2. Set Vctrl = 0V
3. Set Vd = 0V
4. Set Vg = 0V

**Recommended Application Circuit**

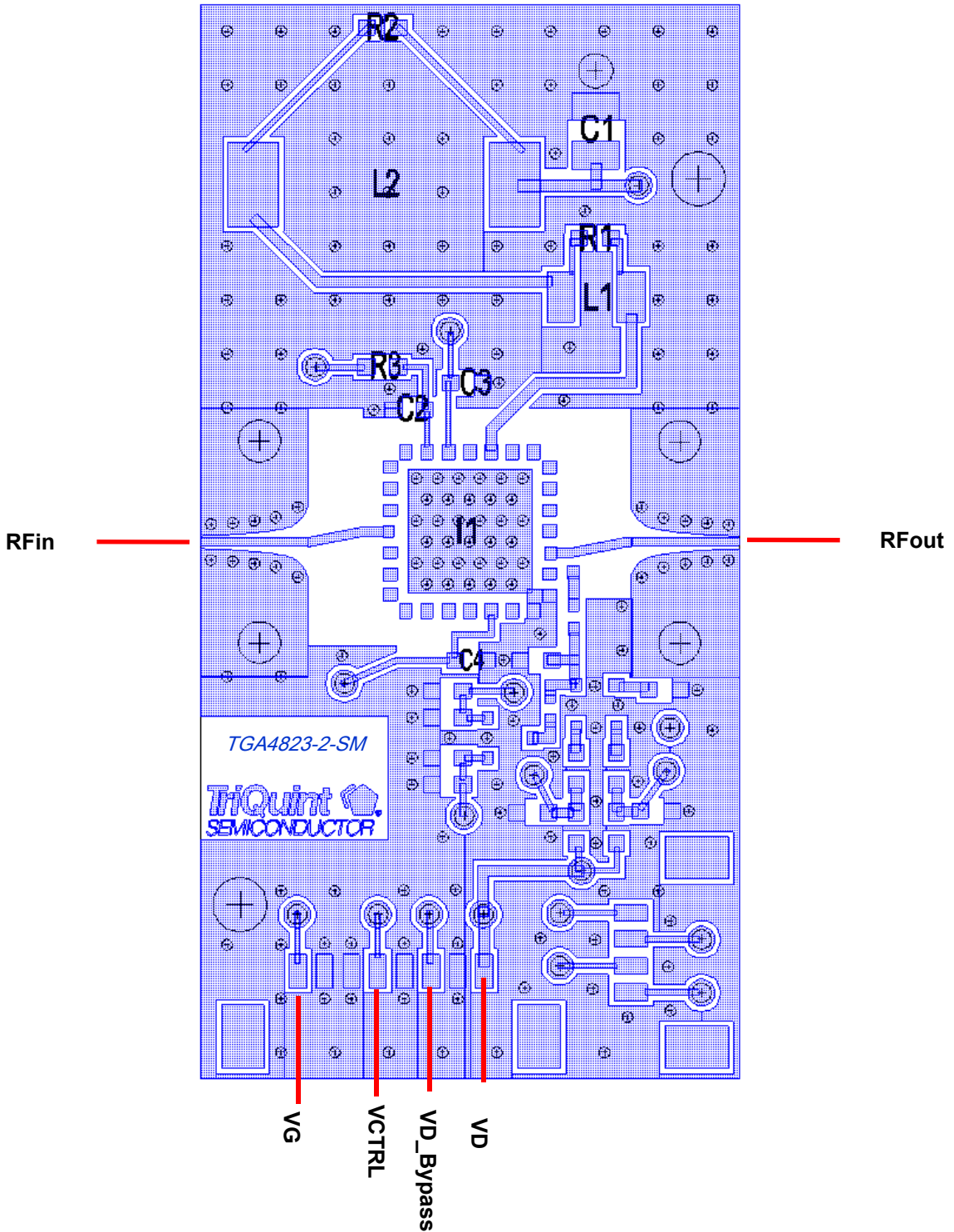


Label	Value	Part Number	Vendor
L1	330nH	ELJ-FAR33MF2	Panasonic
L2	220uH	ELL-CTV221M	Panasonic
R1,R2	270 Ohm	ERJ-3GEYJ271V	Panasonic
R3	620 Ohm	ERJ-3GEYJ621V	Panasonic
C1	10uF	TAJA106K016R	AVX
C2,C3	1uF	0603YG105ZAT2A	AVX
C4	10uF	GRM188R60J106ME47D	Murata
U1		TGA4823-SM	TriQuint

\*\* Note: For Hot-Pluggable option, R3 is limited to Rx ohms,  
for a maximum Vctrl\_user such that Vctrl pin on package does not exceed + 2 V  
Where Rx = (Vctrl\_user - Vctrl\_pin) / Ictrl\_max = (Vctrl\_user - 2V) / 18.9 mA

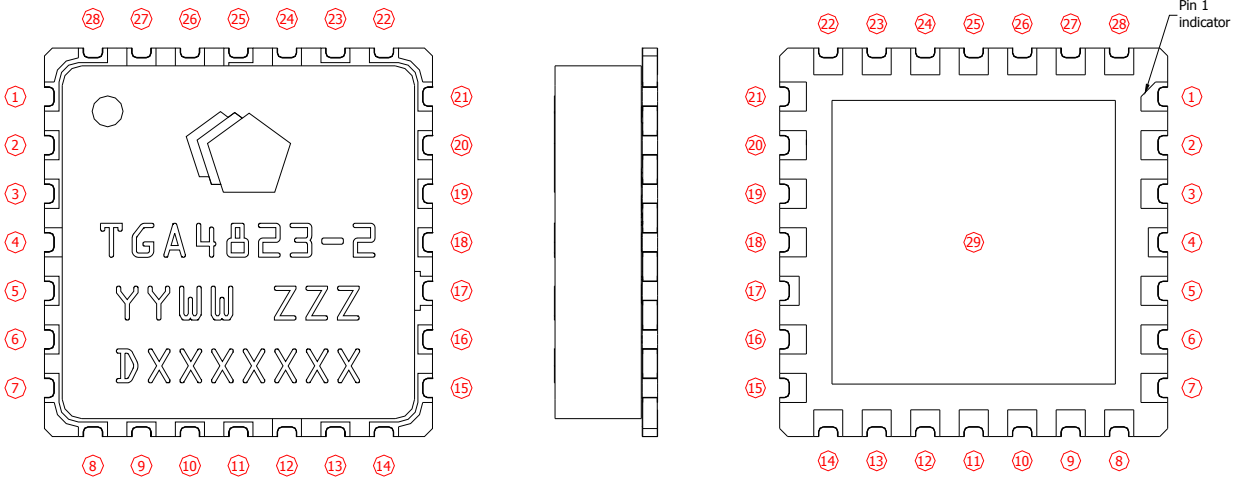
**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

**Recommended Assembly Diagram**

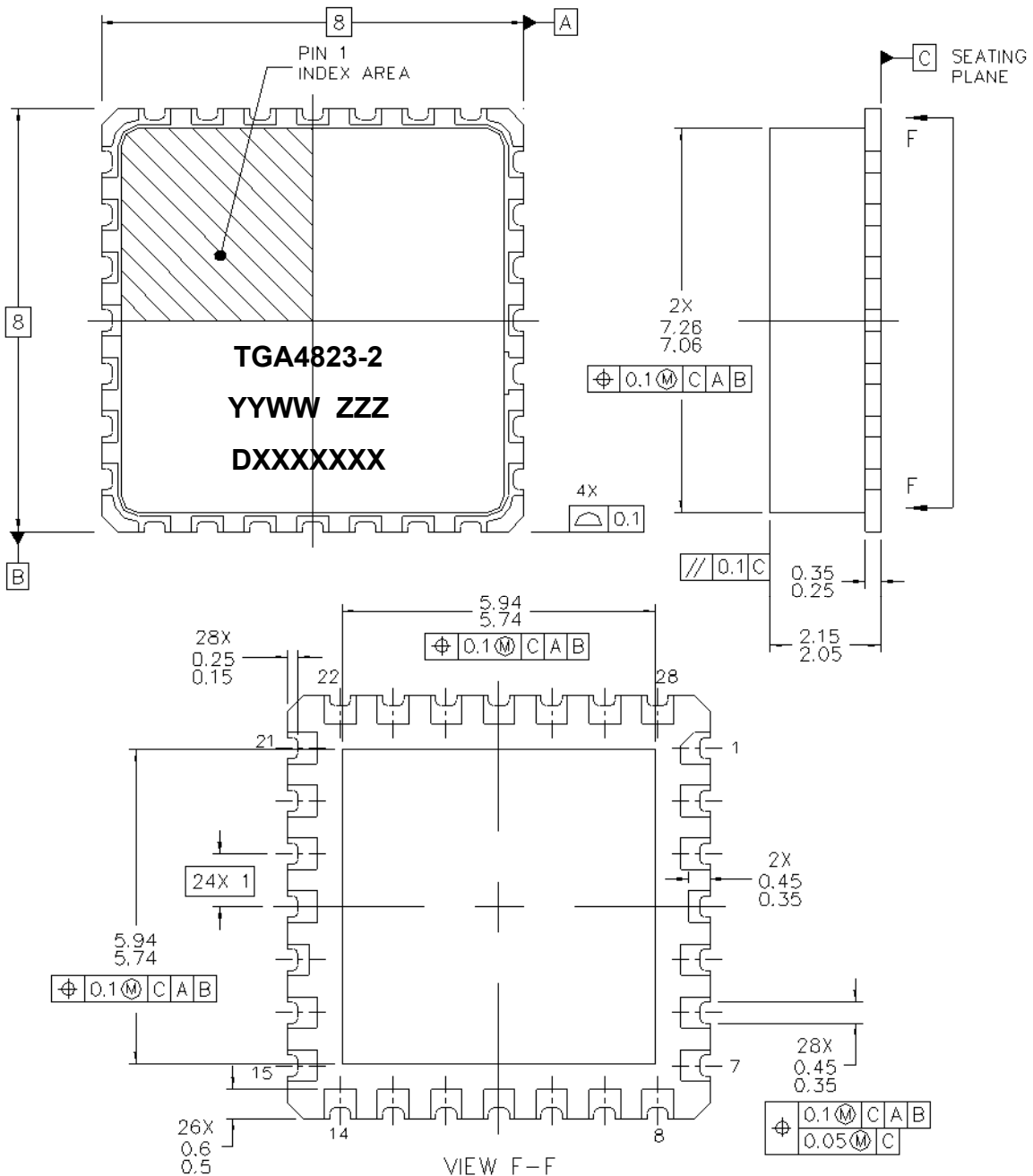


**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

**Package Pinout**



Pin	Description
1,2,3,5,6,7,8,9,10, 11,13,14,15,16,18, 19,20,21,22, 23,25,28	N/C
4	RF In
12	Vg
17	RF Out
24	Vd
26	Vd_Bypass
25, 27	Vctrl
29	GND



**Part Markings:**

YY = Assembly year, WW = Assembly week, ZZZ = Serial Number, DXXXXXXX = Batch ID

**Materials:**

Package base Aluminum Nitride (AlN)  
Package lid White Alumina (Al<sub>2</sub>O<sub>3</sub>)

**Pad finish on package base:**

Electroless gold (Au) 0.5 – 1.0 um  
Over  
Electroless nickel (Ni) 2.0 um min.

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**



## Assembly Notes

### Recommended Surface Mount Package Assembly

- Proper ESD precautions must be followed while handling packages.
- Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.
- TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.
- Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.
- Clean the assembly with alcohol.

## Typical Solder Reflow Profiles

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

## Ordering Information

Part	Package Style
TGA4823-2-SM	8x8 Surface Mount

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***