Class-D Audio Power Amplifier

Preliminary Technical Data

AD1990/AD1992/AD1994/AD1996

FEATURES

Integrated Stereo Modulator & Power Stage
0.005% THD+N
101.5dB Dynamic Range
PSRR > 65 dB
R_{DS-ON} < 0.3 Ω (per transistor)
Efficiency > 80% @ 5W/6 Ω
EMI Optimized Modulator
On-Off-Mute Pop Noise Suppression
Short Circuit Protection
Over-Temperature Protection
Low Cost DMOS Process

APPLICATIONS

Flat Panel Televisions
Automotive Amplifiers
PC Audio Systems
Mini Components

GENERAL DESCRIPTION

The AD199x is a two channel Bridge Tied Load (BTL) switching audio power amplifier with integrated ∑Δ modulator. The modulator accepts a 1Vrms input signal (maximum power) and generates a switching waveform to drive speakers directly. One of the two modulators can control both output stages providing twice the current for single-channel applications. A digital, microcontroller-compatible interface provides control of reset, mute and PGA gain as well as output signals for thermal and over-current error conditions. The output stage can operate from supply voltages ranging from 8V to 20V. The analog modulator and digital logic operate from a 5V supply.

AD1990: 5Wx2 (10Wx1)
AD1992: 10Wx2 (20Wx1)
AD1994: 25Wx2 (50Wx1)
AD1996: 40Wx2 (80Wx1)

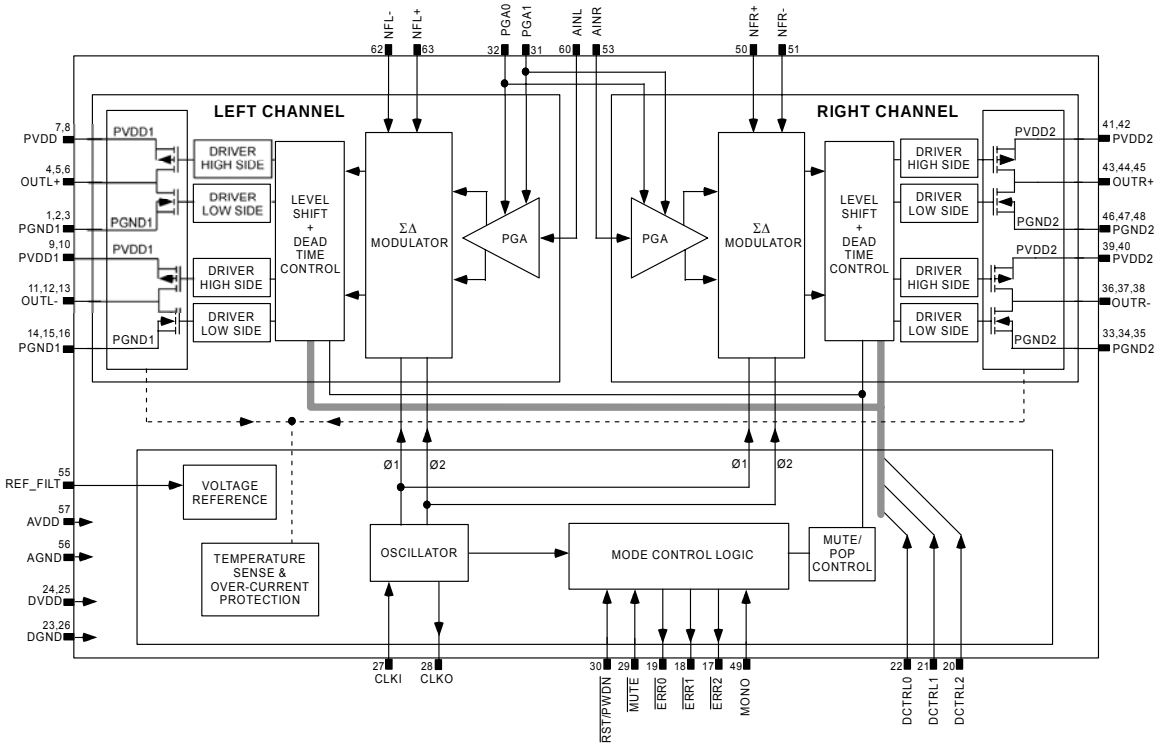


Figure 1. Block Diagram

Rev. PrA – 1/20/05
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AD199X—SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages

AV_{DD}	5 V
DV_{DD}	5 V
PV_{DDX}	12 V
Ambient Temperature	25 °C
Load Impedance	6 Ω
Clock Frequency	11.2896 MHz
Measurement Bandwidth	20 Hz to 20 KHz

Table 1. Performance of both channels is identical

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
OUTPUT POWER (P_O)					R_L = 6Ω, PV_{DD} = 20 V, 1 kHz (FTC)
AD1990		4		W	@ <0.01% THD+N
		5		W	@ 10% THD+N (FTC)
AD1992		8		W	@ <0.01% THD+N
		10		W	@ 10% THD+N (FTC)
AD1994		16		W	@ <0.01% THD+N
		25		W	@ 10% THD+N (FTC)
AD1996		25		W	@ <0.01% THD+N
		40		W	@ 10% THD+N (FTC)
Efficiency		84		%	f_{IN} =1 kHz, P_O = 5 W, R_L = 6Ω
R_{ON}					
per High Side Transistor			0.3	Ω	@ 1 A
per Low Side Transistor			0.2	Ω	@ 1 A
Maximum Current Through OUTx			4	A	
Thermal Warning Active		135		°C	Die temperature
Thermal Shutdown Active		150		°C	Die temperature
Overcurrent Shutdown Active		4		A	
Nominal Input Level		1.0		V_{RMS}	PGA gain = 0 dB
Modulation Factor			90	%	
PERFORMANCE SPECIFICATIONS					
Total Harmonic Distortion (THD+N)		0.005		%	PGA = 0 dB, P_O = 5 W
		0.007		%	PGA = 6 dB, P_O = 5 W
		0.01		%	PGA = 12 dB, P_O = 5 W
		0.02		%	PGA = 18 dB, P_O = 5 W
Signal/Noise Ratio (SNR)		102		dB	
Dynamic Range (DNR)		102		dB	-60 dB Input
Crosstalk		-100		dB	Measured channel input = 0 V_{RMS}, other channel = 1 kHz at 5W
Power supply rejection (PSRR)	60			dB	20 Hz - 1 kHz
	45			dB	20 Hz – 20 kHz
DC SPECIFICATIONS					
Input Impedance		20		kΩ	AINL and AINR analog inputs
Output DC Offset Voltage		±10		mV	

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLIES					
Supply Voltage AV_{DD}	4.5	5	5.5	V	
Supply Voltage DV_{DD}	4.5	5	5.5	V	
Supply Voltage PV_{DDX}	6.5	8-20	22.5	V	
Powerdown Current					$\overline{\text{RST/PDN}}$ held low
AV_{DD}		0.1	0.5	µA	
DV_{DD}		0.1	0.5	µA	
PV_{DDX}		19	25	µA	
Mute Current					$\overline{\text{MUTE}}$ held low
AV_{DD}		19		mA	
DV_{DD}		2.7		mA	
PVDD		1.5		mA	
Quiesent Current					Inputs Grounded, Non-Overlap Time = TBD
AV_{DD}		20		mA	
DV_{DD}		5.2		mA	
PV_{DDX}		3.2		mA	
Operating Current					V_{IN} = 1V_{RMS}, P_O = 5 W
AV_{DD}		22		mA	
DV_{DD}		5.8		mA	
PV_{DD}			4	A	per FET
DIGITAL I/O					
Input Voltage High	2.0		DV_{DD}	V	
Input Voltage Low			0.8	V	
Output Voltage High	DV_{DD}-0.8			V	@ 2 mA
Output Voltage Low			0.4	V	@ 2 mA
Leakage Current on Digital Inputs			10	µA	

Table 2 DIGITAL TIMING (Guaranteed over -40°C to +85°C, AV_{DD} = DV_{DD} = 5.0V ± 10%, PV_{DDX} =12V ± 10%, Non Overlap Time t_{NOL} = Shortest, See Table 6: Non-Overlap Time Settings)

Parameter	Min	Typ	Max	Units	Comments
t_{PDRP}	500			ns	$\overline{RST/PDN}$ minimum low pulsewidth
t_{MPDL}			5	µs	$\overline{MUTE}$ asserted to output initial response
$t_{MUTEDLY}$		1		sec	$\overline{RST/PDN}$ high to $\overline{MUTE}$ high delay

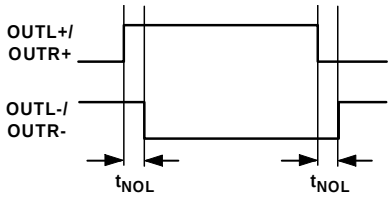


Figure 2. Output Timing

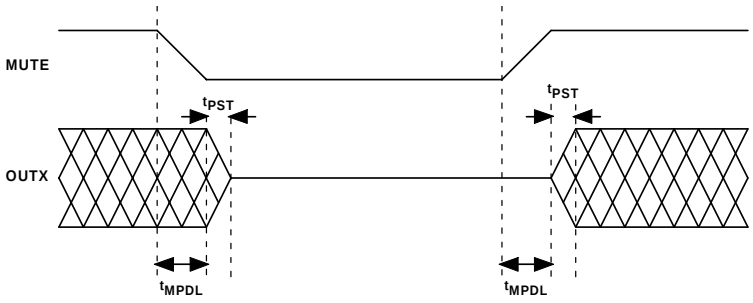


Figure 3. Mute Timing

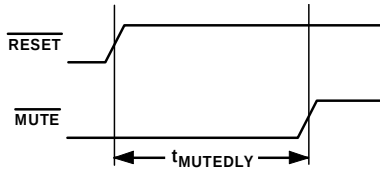


Figure 4. Reset to Mute Delay

ABSOLUTE MAXIMUM RATINGS

Table 3. AD199x Absolute Maximum Ratings[1]

Parameter	Rating
AV_{DD}, DV_{DD} to AGND, DGND	-0.3 V to +6.5 V
PV_{DDX} to PGND	-0.3 V to +30.0 V[2]
AGND to DGND to PGND	-0.3 V to +0.3 V
AV_{DD}, to DV_{DD}	-0.5 V to +0.5 V
Audio Inputs	AGND to AV_{DD}
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
θ_{JC} Thermal Impedance (LFCSP)	3°C/W
θ_{JC} Thermal Impedance (PSOP)	1°C/W
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Including any induced voltage due to inductive load

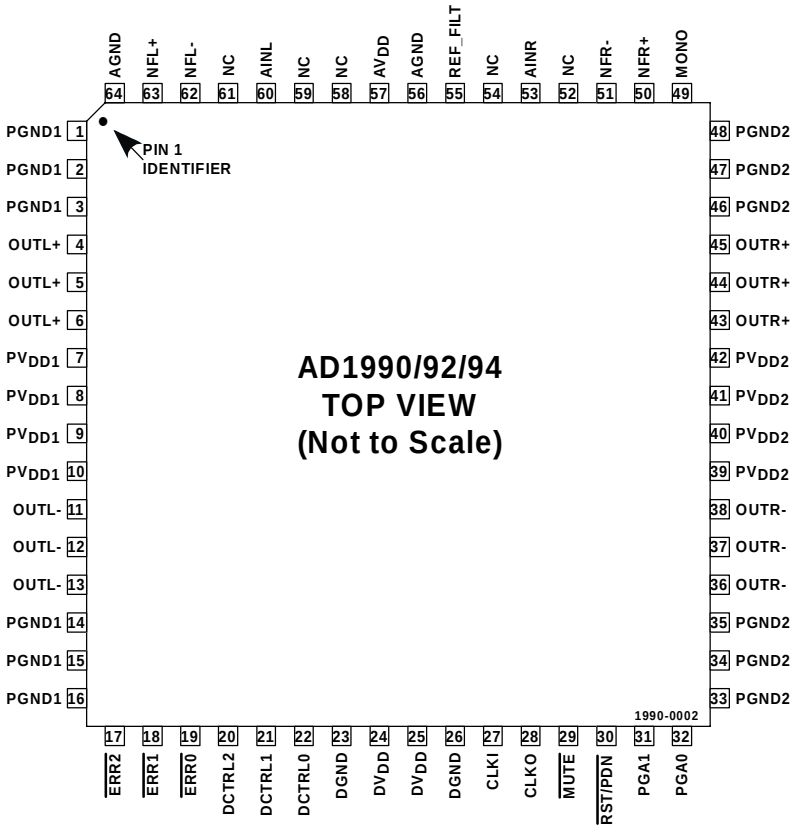


Figure 5. 64 Lead LFCSP Package

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

Table 4. Pin Function Descriptions

LFCSP Pin No.	PSOP Pin No.	Name	In/Out	Description
1,2,3	3	PGND1		Negative power supply for high power transistors A2 and B2
4,5,6	2	OUTL+	O	Output of high power transistor pair, left channel positive polarity
7,8,9,10	1,36	PVDD1		Positive power supply for high power transistors, left channel high-side
11,12,13	35	OUTL-	O	Output of high power transistor pair, left channel negative polarity
14,15,16	34	PGND1		Negative power supply for high power transistors, left channel low-side
17	33	$\overline{\text{ERR2}}$	O	Active low thermal shutdown error output
18	32	$\overline{\text{ERR1}}$	O	Active low thermal warning error output
19	31	$\overline{\text{ERR0}}$	O	Active low overcurrent error output
20		DCTRL2	I	Non-overlap time setting MSB
21		DCTRL1	I	Non-overlap time setting
22		DCTRL0	I	Non-overlap time setting LSB
23,26	29,30	DGND		Negative power supply for low power digital circuitry
24,25	28	DVDD		Positive power supply for low power digital circuitry
27	27	CLKI	I	Clock input for 256 × f_S audio modulator clock
28	26	CLKO	O	Inverted version of CLKI for use with external crystal oscillator
29	25	$\overline{\text{MUTE}}$	I	Active low mute input
30	24	$\overline{\text{RST/PDN}}$	I	Active low reset/power-down input
31	23	PGA1	I	Programmable gain amplifier (PGA) gain MSB
32	22	PGA0	I	Programmable gain amplifier (PGA) gain LSB
33,34,35	21	PGND2		Negative power supply for right channel high power transistors
36,37,38	20	OUTR-	O	Output of high power transistor pair, right channel negative polarity
39,40,41,42	18,19	PVDD2		Positive power supply for right channel high power transistors
43,44,45	17	OUTR+	O	Output of high power transistor pair, right channel positive polarity
46,47,48	16	PGND2		Negative power supply for right channel high power transistors
49	15	AGND		Negative power supply for low power analog circuitry
50	14	NFR+	I	Right channel negative feedback – positive input
51	13	NFR-	I	Right channel negative feedback – negative input
52		NC		Not Connected. This pin is not used and should be left floating
53	12	AINR	I	Analog input for right channel
54		NC		Not Connected. This pin is not used and should be left floating
55	11	REF_FILT	O	Filter pin for bandgap reference - should be bypassed to AGND
56	10	AGND		Negative power supply for low power analog circuitry
57	9	AVDD		Positive power supply for low power analog circuitry
58		NC		Not Connected. This pin is not used and should be left floating
59		NC		Not Connected. This pin is not used and should be left floating
60	8	AINL	I	Analog input for left channel
61	4	NC		Not Connected. This pin is not used and should be left floating
62	7	NFL-	I	Left channel negative feedback – negative input
63	6	NFL+	I	Left channel negative feedback – positive input
64	5	MONO	I	Mono mode (drive left and right output transistors from same modulator)

TYPICAL PERFORMANCE CHARACTERISTICS

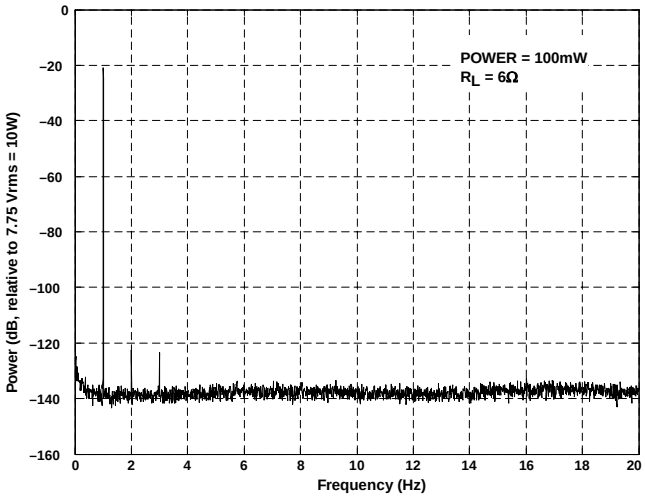


Figure 6. 1KHz, 100mW into a 6Ω Load

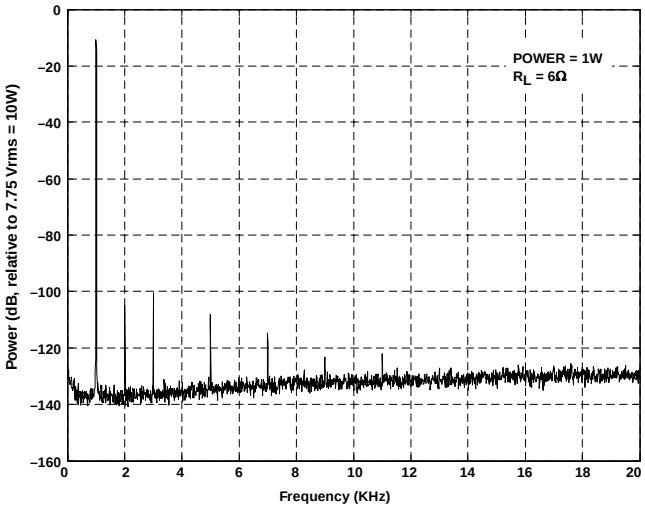


Figure 7. 1KHz, 1W into a 6Ω Load

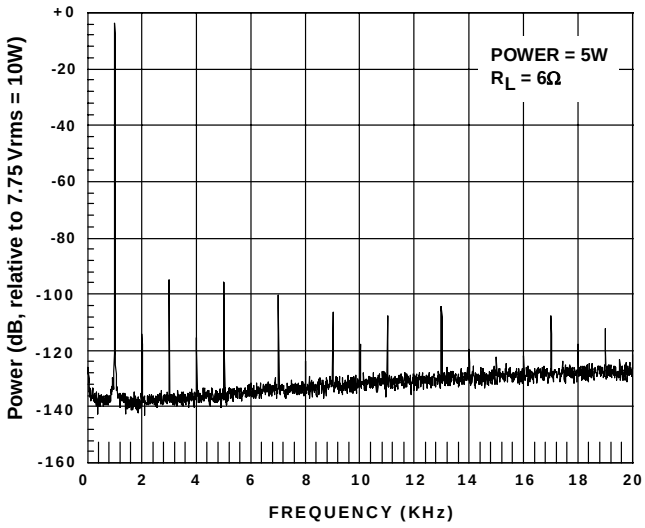


Figure 8. 1KHz, 5W into a 6Ω Load

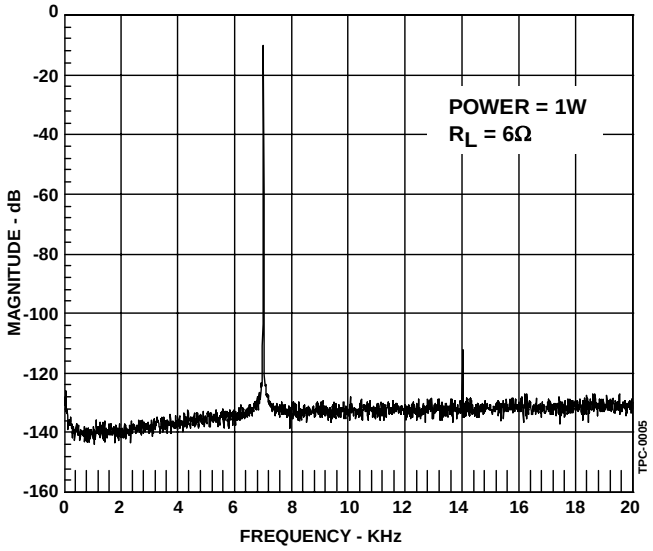


Figure 9. 7KHz, 1W into a 6Ω Load

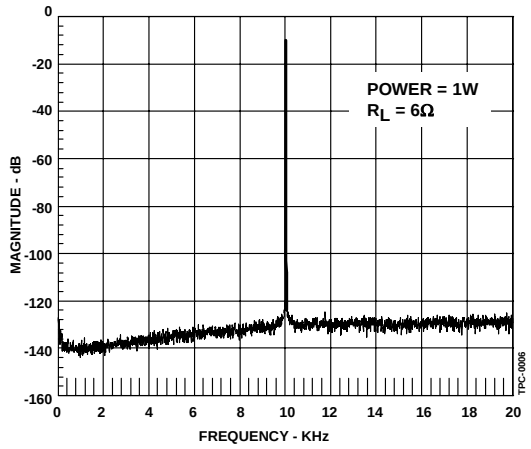


Figure 10. 10KHz, 1W into a 6Ω Load

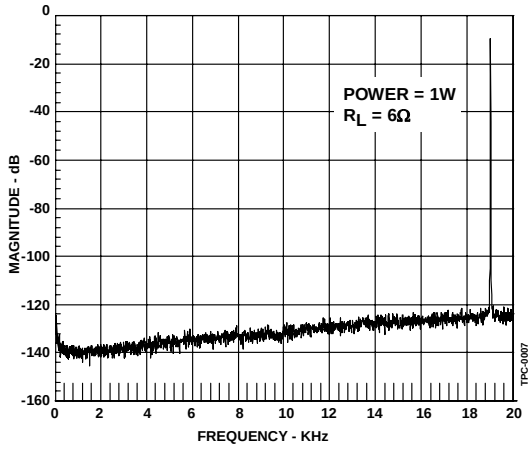


Figure 11. 19KHz, 1W into a 6Ω Load

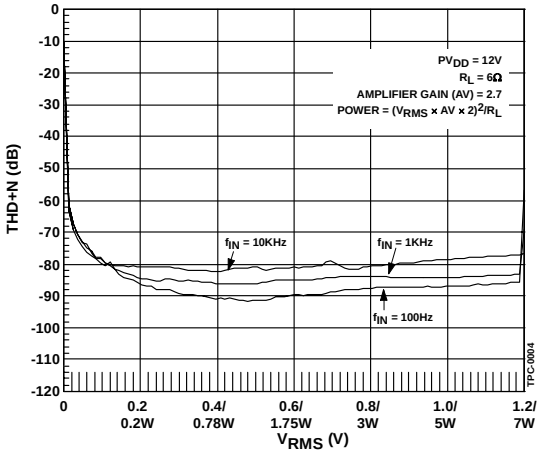


Figure 12. THD+N vs Input Signal/Power Output

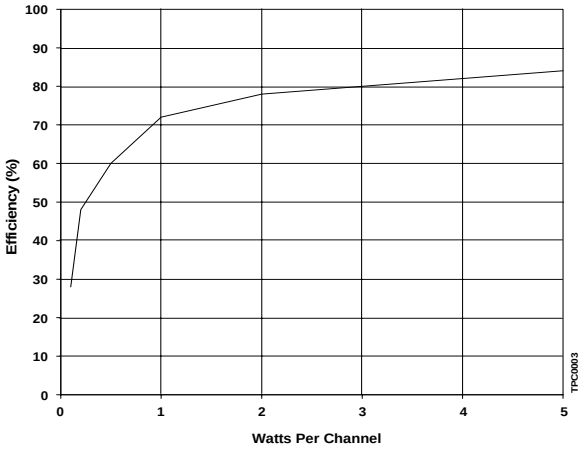


Figure 13. Efficiency vs Power

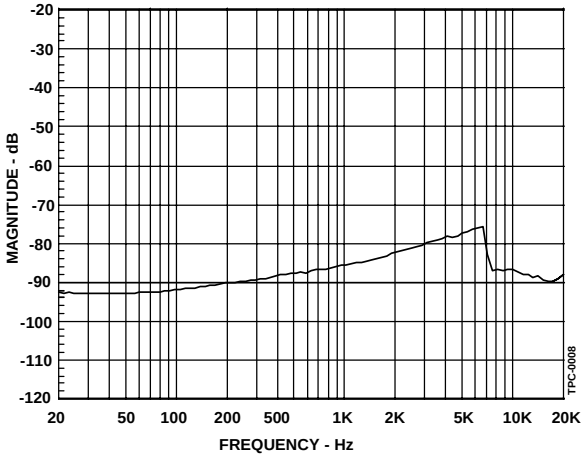


Figure 14. THD+N vs Distortion, 1W into a 6Ω Load

FUNCTIONAL DESCRIPTION

DEVICE ARCHITECTURE

The AD199x is an audio quality, switching amplifier with an integrated sigma-delta modulator. The power stage of the AD199x is arranged internally as four transistor pairs, which are used as two H-bridge outputs to provide stereo amplification. The transistor pairs are driven by the output of the ∑Δ modulator. A user selectable non-overlap time is provided between the switching of the high side transistor and low side transistor to ensure that both transistors are never on at the same time. The AD199x implements turn on pop suppression to eliminates any pops or clicks following a reset or un-mute.

Analog Input Section

The analog input section uses an internal amplifier to bias the input signal to the reference level. A DC blocking capacitor should be connected as shown in Figure 15 to remove any external DC bias contained in the input signal

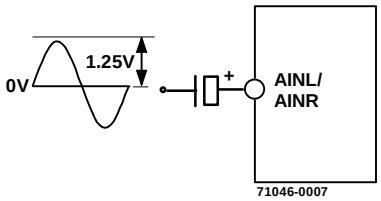


Figure 15. Normal Operation

The Sigma-Delta Modulator

Detailed description pending on patents pending, as well as announcements, conference proceedings and other scheduled public disclosures.

Selecting Stereo or Mono Mode

Driving the H-Bridge

Each channel of the switching amplifier is controlled by a 4 transistor H-bridge to give a differential output stage. The outputs of the H-bridges, OUTR+, OUTR-, OUTL+ and OUTL- will switch between PVDD and PGND as determined by the sigma delta modulator. The power supply that is used to drive the power stage of the AD199x should be typically in the range of +8 V to +20 V and should be capable of supplying enough current to drive the load. This power supply is connected across the PVDD and PGND pins. The feedback pins, NFR+, NFR-, NFL+ and NFL-, are used to supply negative feedback to the modulator. The pins are connected to the outputs of the H-bridge via a resister divider network as shown in Figure 16. See the section on Selecting the Modulator Gain for more information.

External schottky diodes can be used to reduce power loss during the non-overlap time when neither of the high-side or low-side transistors is on. During this time neither transistor is driving the OUTx pin. The nature of the inductors is to keep current flowing. For example the OUTx pin may approach and pass the PGND level to achieve this. When the voltage at the OUTx pin is 0.7V below PGND the parasitic diode associated with the low-side transistor will become forward biased and turn on. When the high-side transistor turns on the voltage at OUTx will rise to PVDD and will reverse bias the parasitic diode. However, by its nature the parasitic diode has a long reverse recovery time and current will continue to flow through it to PGND thus causing the entire circuit to draw more current than necessary. The addition of the schottky diodes prevents this happening. When the OUTx pin goes more than 0.3V below PGND the schottky diode becomes forward biased. When the high-side transistor turns on the schottky diode becomes reverse biased. The reverse recovery time of the schottky diode is significantly faster than the parasitic diode so far less current is wasted. A similar effect happens when the inductor induces a current which drives the OUTx pin above PVDD. Figure 16 shows how the external components of a system are connected to the pins of the AD199x to form the H-bridge configuration.

AMPLIFIER GAIN

Selecting the Modulator Gain

The AD199x modulator can be thought of as a switching analog amplifier with a voltage gain controlled by two external resistors forming a resistor divider between the OUTxx pins and PGND. The centre of the resistor divider is connected to the appropriate feedback pin NFx. Selecting the gain along with the PVDD Voltage will determine how much power can be delivered to a load for a fixed input signal. The gain of the modulator is controlled by the values of R1 and R2 (see Figure 16) according to the equation below.

$$Gain = (R1 + R2)/R2$$

The gain should be selected such that a 1Vrms input signal doesn't cause the modulator to generate an output signal which has a peak to peak value greater than 90% of PVDD. Selecting a gain that meets this criteria will ensure that the modulator remains in a stable operating condition.

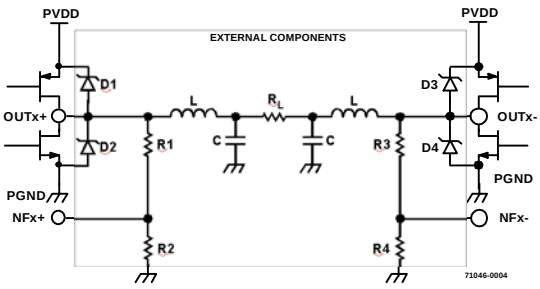


Figure 16. H-Bridge Configuration

Programmable Gain Amplifier (PGA)

The AD199x incorporates a single-ended to differential converter for each channel in the analog front-end section. Both single-ended to differential converters feature a programmable gain amplifier with four different gain settings. The gain is set using the pins PGA1 and PGA0 as shown in Table 5. The PGA1 and PGA0 pins are continuously monitored allow the gain to be changed at any time.

Table 5. PGA Gain Settings

PGA1	PGA0	PGA Gain (dB)
0	0	0
0	1	6
1	0	12
1	1	18

SYSTEM DESIGN

Clocking

The AD199x has two clock pins, CLKI and CLKO which are used to configure the clocking scheme for the device. The AD199x should be driven by a clock which is 256 × f_S where f_S is the desired sampling rate. If a crystal is to be used as the clock source it should be connected across the CLKI and CLKO pins as shown in Figure 17. Crystal Connection The values and type of capacitors used will be determined by the crystal manufacturer. A square-wave clock source may be connected directly to the CLKI pin. The logic levels of the square wave should be compatible with those defined in the Digital I/O section of the specifications page.

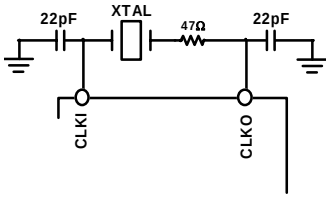


Figure 17. Crystal Connection

Output Transistor Non-Overlap Time

Ipsum lorum...

Power-up Considerations

Careful power-up is necessary when using the AD199x to ensure correct operation and avoid possible latch-up issues. The AD199x should be powered-up with RST/PDN and MUTE held low until all the power supplies have stabilized. Once the supplies have stabilized the AD199x can be brought out of reset by bringing RST/PDN high and then MUTE can be brought high as required.

On/Off/Mute Pop Noise Suppression

The AD199x features pop suppression which is activated when the part is reset or taken out of mute. The pop suppression is achieved by pulsing the power outputs to bring the outputs of the LC filter from 0V to mid-scale in a controlled fashion. This feature eliminates unwanted transients on both the outputs and the high voltage power supply.

Thermal Protection

The AD199x features thermal protection. When the die temperature exceeds approximately 135°C the Thermal Warning Error output (ERR1) is asserted. If the die temperature exceeds approximately 150°C the Thermal Shutdown Error output (ERR2) is asserted. If this occurs, the part shuts down to prevent damage to the part. When the die temperature drops below approximately 120°C both error outputs are negated and the part returns to normal operation.

Over-current Protection

The AD199x features over current or short circuit protection. If the current through any power transistors exceeds 4A the part goes into mute and the Over-current error output (ERR0) is asserted. This is a latched error and does not clear automatically. To clear the error condition and restore normal operation, the part must be either reset, or MUTE must be asserted and negated.

Application Considerations

Good board layout and decoupling are vital for correct operation of the AD199x. Due to the fact that the part switches high currents there is the potential for large PVDD bounce each time a transistor transitions. This can cause unpredictable operation of the part. To avoid this potential problem, close chip decoupling is essential. It is also recommended that the decoupling capacitors are placed on the same side of the board as the AD199x, and connected directly to the PVDD and PGND pins. By placing the decoupling capacitors on the other side of the board and decoupling through vias the effectiveness of the decoupling is reduced. This is because vias have inductive properties and therefore prevent very fast discharge of the decoupling capacitors. Best operation is achieved with at least one decoupling capacitor on each side of the AD199x, or optionally two capacitors per side can be used to further reduce the series resistance of the capacitor. If these decoupling recommendations cannot be followed and decoupling through vias is the only option, the vias should be made as large as possible to increase surface area, thereby reducing inductance and resistance.

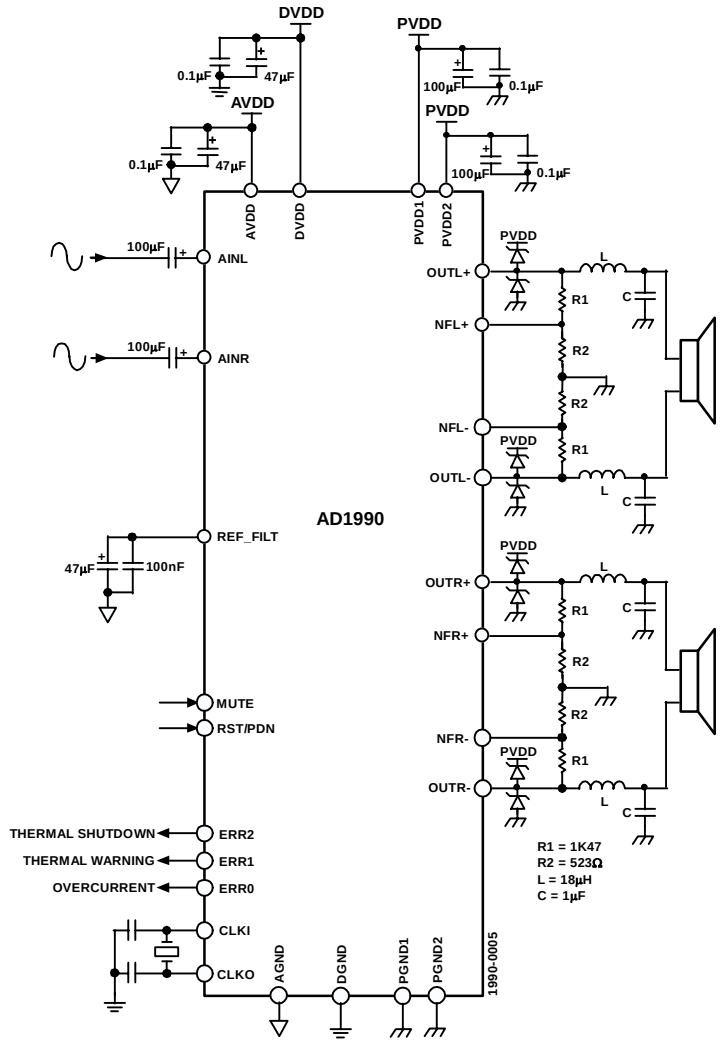


Figure 18. Typical Stereo Mode Application Circuit

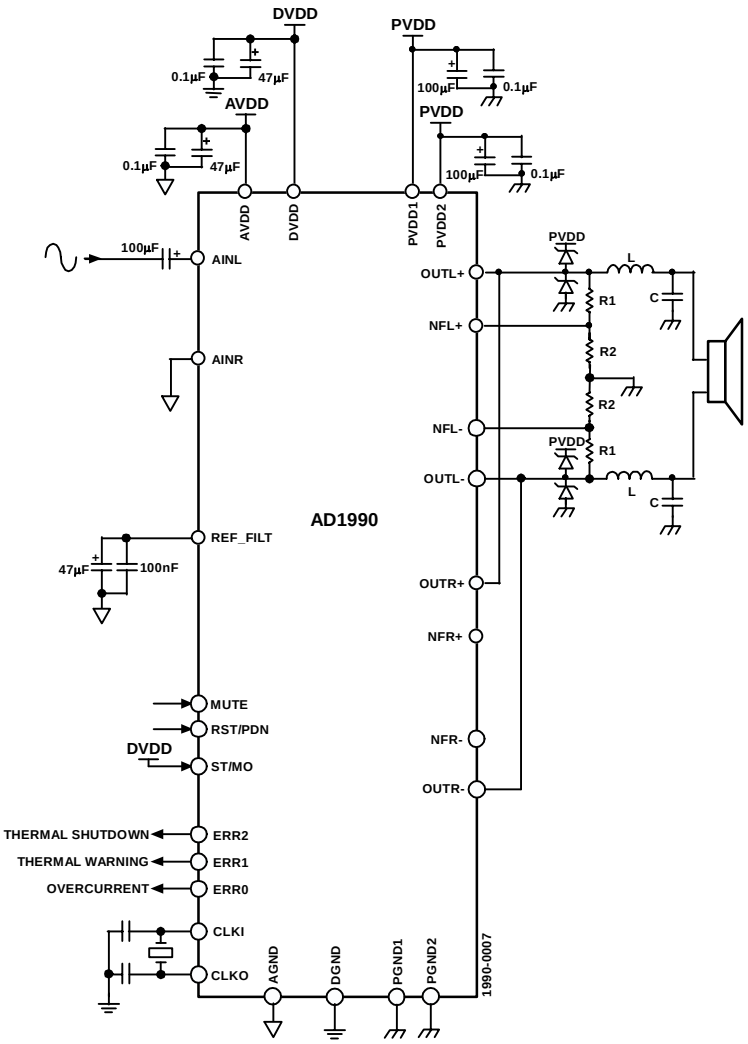


Figure 19. Mono Mode Circuit

OUTLINE DIMENSIONS

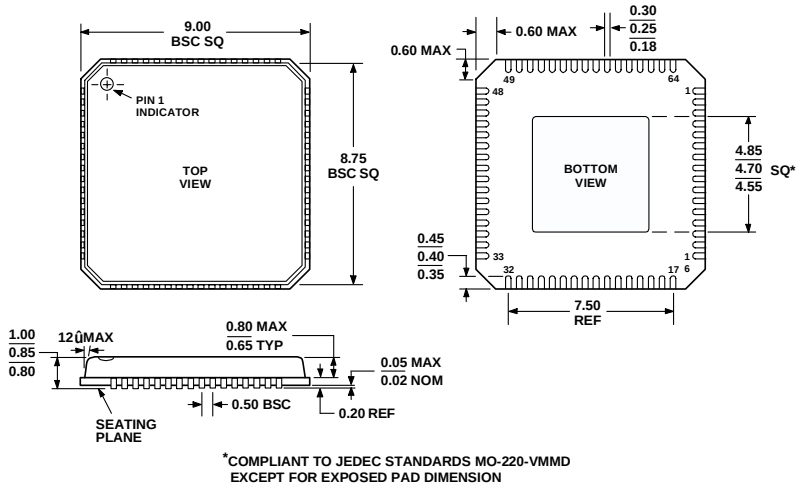


Figure 20. 64-Lead Frame Chip Scale Package (LFCSP)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 6. Ordering Guide

Products	Package Temperature	Power Rating	Package Description	Package Outline
AD1990ACPZ	–40°C to +85°C	5W per channel	Lead Frame Chip Scale Package	CP-64
AD1992ACPZ	–40°C to +85°C	10W per channel	Lead Frame Chip Scale Package	CP-64
AD1994ACPZ	–40°C to +85°C	25W per channel	Lead Frame Chip Scale Package	CP-64
AD1996ACPZ	–40°C to +85°C	40W per channel	Power Small Outline Package	PSOP-36

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Printed in the U.S.A.
PR05380-0-1/05(PrA)

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