PROGRAMMABLE INTERVAL TIMER

TMP8253P-5

1. GENERAL DESCRIPTION

The TMP8253P-5 (hereinafter referred to as TMP8253) is a programmable counter/timer chip designed for use as the TLCS-85A microcomputer peripheral. It is organized as 3 independent 16 bit counters, each operates with a count rate of up to 2.6MHz. All modes of operation are software programmable.

2. FEATURES

- Count Binary or BCD
- 3 Independent 16 Bit Counters
- Single +5V Supply
- Count rate DC to 2.6MHz
- 6 programmable Counter Modes
- Compatible with Intel's 8253-5

3. PIN CONNECTIONS

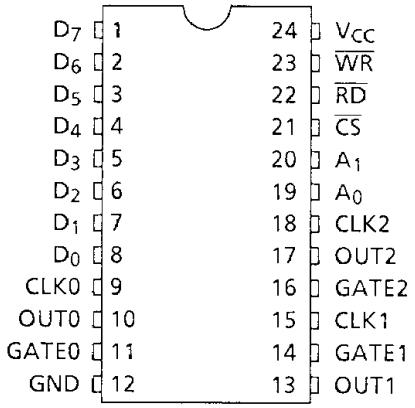
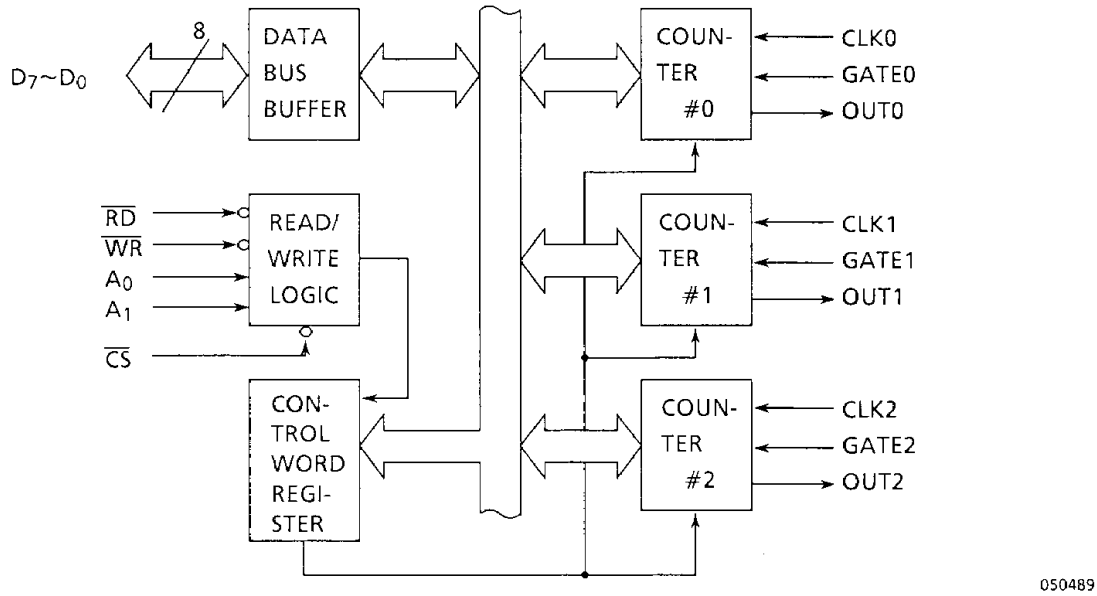


Table 3.1 Pin Names

D_7~D_0	Data Bus (8 bit)
CLK N	Counter Clock Input
GATE N	Counter Gate Input
OUT N	Counter Output
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0~A_1	Counter Select
V_{CC}	+5V
GND	Ground (0V)

050489

4. BLOCK DIAGRAM



5. PIN NAMES AND PIN DESCRIPTION

- GND (Power Supply)

  Ground.

- V_{CC} (Power Supply)

  +5V during operation.

- $\overline{CS}$ (Input)

  A low level input on this pin enables $\overline{RD}$ and $\overline{WR}$ communicaiton between the MPU and the TMP8253. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

- A0, A1 (Input)

  These inputs acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. This pin is used to select one of the three counters to be operated on and to address the control word register for mode selection.

- $\overline{WR}$ (Input)

  A low level input on this pin when $\overline{CS}$ is low enables the TMP8253 to accept mode information or loading counters from the MPU.

- $\overline{RD}$ (Input)

  A low level input on this pin when $\overline{CS}$ is low enables the TMP8253 to output a counter value onto the data bus for the MPU.

- D0~D7 (Input/Output)

  Bidirectional Data Bus. Mode information, the information loading counter or the count values are transfered via this data bus.

- CLK0~CLK2 (Input)

  Clock inputs to counters. Falling edge on this pin enables the counter to countdown.

- GATE0~GATE2 (Input)

  Gate inputs to counters. The function of this pin differs by the mode selection of counter operation.

- OUT0~OUT2 (Output)

  Outputs from the counters. The output signal from this pin differs by the mode seleciton of counter operation.

6. FUNCTIONAL DESCRIPTION

[Block Description]

Data Bus Buffer

This is 3-state, bidirectional, 8 bit buffer used for interfacing the TMP8253 to the system data bus. The Data Bus Buffer has three functions as follows. Programming the Modes of the TMP8253, Loading the count registers, and Reading the count values.

Read/Write Logic

The Read/Write logic accepts inputs from the system bus and in turn generates control signals for overall device operation.

Table 6.1 Addressing

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter # 0
0	1	0	0	1	Load Counter # 1
0	1	0	1	0	Load Counter #2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter # 0
0	0	1	0	1	Read Counter # 1
0	0	1	1	0	Read Counter # 2
0	0	1	1	1	Data Bus is in High-impedance state
1	×	×	×	×	
0	1	1	×	×	

050489

Control Word Register

The Control Word Reginter is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational Mode of each counter, selection of binary or BCD counting and the loading of each count register. No reading of the contents of the Control Word Register is available.

Counter #0, Counter #1, Counter #2

These three blocks are identical so only a single counter will be described. Each counter consists of a single, 16 bit, presettable, down counter. The counter can operate in either binary or BCD and its input, GATE and output are configured by the selection of Modes (Six MODES : MODE 0 to MODE 5) stored in the Control Word Register. Also the control word handles the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple read operations for event counting applications. Special commands and logic are included in the TMP8253 so that the contens of each count value can be read "on-the-fly" without having to inhibit the clock input.

[MODE Definition]

MODE 0 : Interrupt on Terminal Count

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count had been reached.

Rewriting a counter register during counting results in the following :

(1) Write 1st byte stops the current counting.

(2) Write 2nd byte starts the new count.

MODE 1 : Programmable One Shot

The output will go low on the count following the rising edge of the GATE input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the GATE input.

MODE 2 : Rate Generater

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The GATE input, when low, will force the output high. When the GATE input goes high, the counter will start form the initial count. Thus, the GATE input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3 : Square Wave Rate Generator

Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count.

This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decriments the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N − 1)/2 counts.

MODE 4 : Software Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses, counting will continue from the new value, The count will be inhibited while the GATE input is low, Reloading the counter register will restart counting beginning with the new number.

MODE 5 : Hardware Triggered Strobe

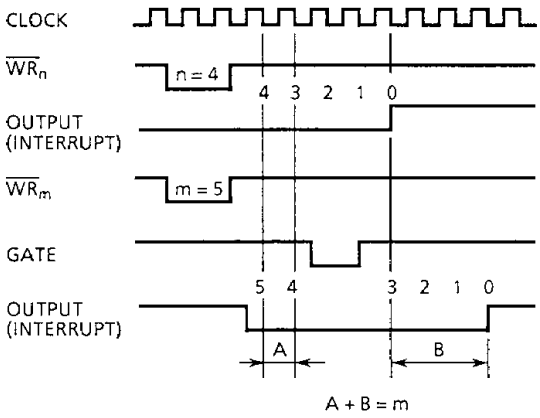
The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Table 6.2 Gate Pin Operaions

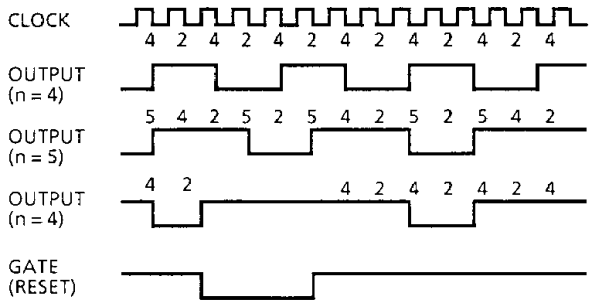
Status Modes	Low or Going Low	Rising	High
0	Disables counting	–	Enables counting
1	–	(1) Initiates counting (2) Resets output after next clock	–
2	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enables counting
4	Disables counting	–	Enables counting
5	–	Initiates counting	–

050489

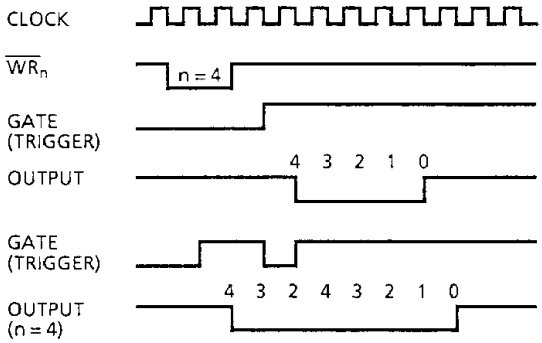
MODE 0 : Interrupt on Terminal Count



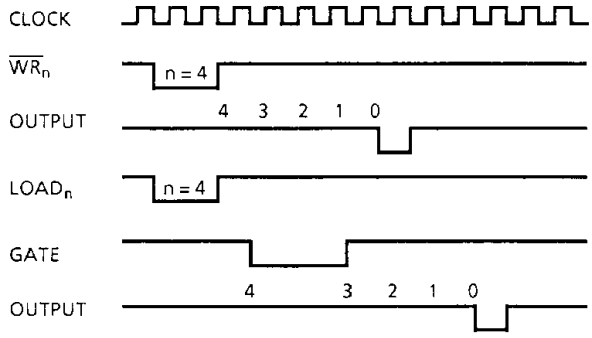
MODE 3 : Square Wave Generator



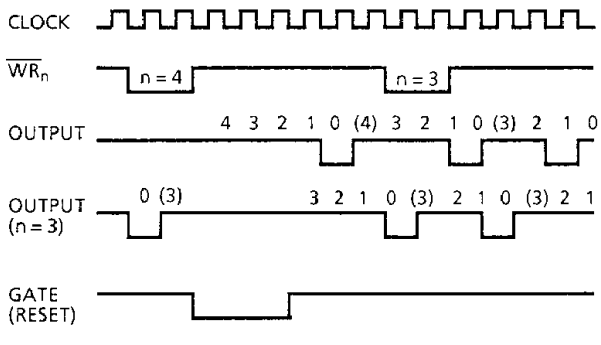
MODE 1: Programmable One-Short



MODE 4 : Software-Triggered Strobe



MODE 2 : Rate Generator



MODE 5 : Hardware-Triggered Strobe

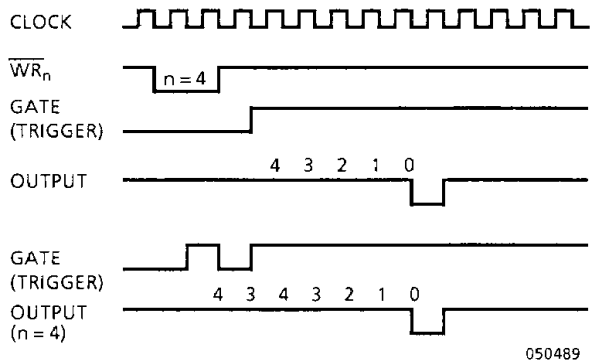
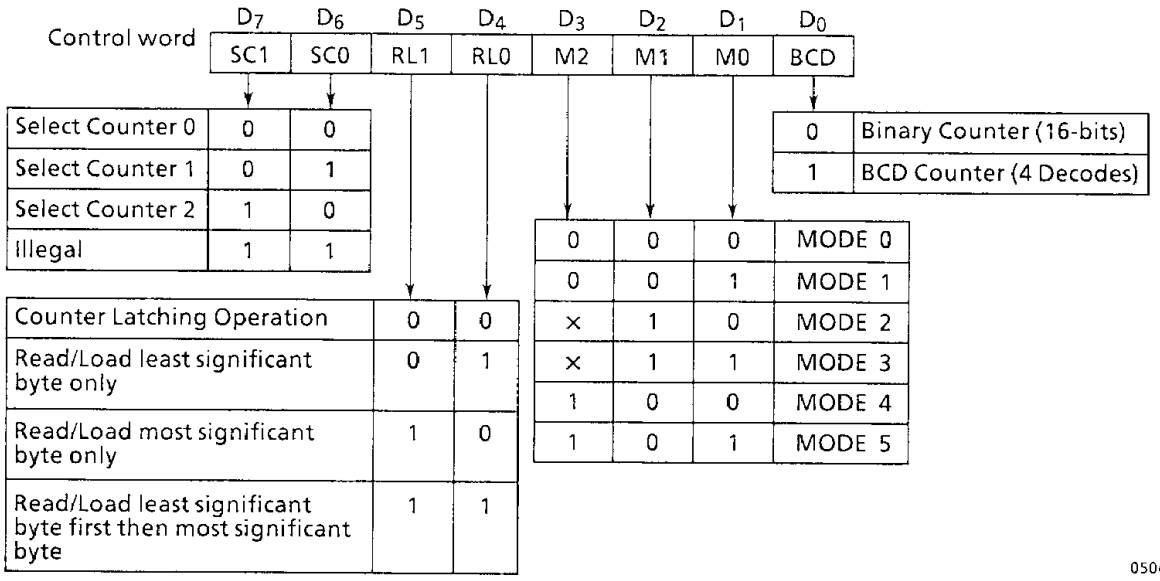


Figure 6.1 TMP8253 Timing Diagrams

7. PROGRAMMING THE TMP8253

All of the Modes for each counter are programmed by the systems software by simple I/O operations.

Each counter of the TMP8253 is individually programmed by writing a control word into the Control Word Register. ($\overline{CS}=0$, A0 = A1 = 1, $\overline{WR}=0$).



Note SC: Select Counter, RL: Read/Load, M: Mode, BCD: Binary Coded Decimal.

The programmer must write out to the TMP8253 a Mode Control Word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The acctual order of the programming is quite flixible. Writing out ot the Mode Control Word can be in any sequence of counter selection.

The loading of the Count Register with actual count value, however, must be done in exactly the sequence programmed in the Mode Control Word (RL0, RL1).

8. COUNTER LOADING

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock.

The count register must be loaded with the number of bytes programmed in the Mode Control Word. The one or two bytes to be loaded in the count register do not have to follow the associated Mode Control Word. They can be programmed at any time following the Mode Control Word loading as long as correct number of bytes is loaded in order.

All counters are down counters. Loading all zeros will result in the maximum count (2^{16} for Binary or 10^4 forBCD). In MODE 0 and MODE 4, the new count will not restart until the load has been completed.

9. READ OPERATIONS

The TMP8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations. By controlling the A0, A1 inputs to the TMP8253, the programmer can select the counter to be read. The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the GATE input or by external logic that inhibits the clock input.

The contents of the counter selected must be read in the sequence programmed in the Mode Control Word (RL0, RL1). When RL0, RL1 is 11. First I/O read contains the least significant byte (LSB), second I/O read contains the most significant byte (MSB), and the two bytes must be read before any loading WR command can be sent to the same counter.

The second method allows the programmer to read the contents of any counter without affecting or disturbing the counting operation. When the programmer wishes to read the contents of a selected counter "On-the-fly", he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter. The contents of the latched register must be read in the sequence programmed in the Mode Control Word (RL0, RL1). This commands has no effect on the counters mode.

10. PROGRAM EXAMPLE

```
Set up sequence for counter #0
    MVI   A, 00110000B  ..... #0, LSB → MSB, MODE 0, Binary
    OUT   CWAD          ..... The address of Control Word Register
    MVI   A, 53H        ..... LSB for counter #0
    OUT   CNT0          ..... The address of counter #0
    MVI   A, 82H        ..... MSB for counter #0
    OUT   CNT0          ..... The address of counter #0
    :
READ the contents of counter #0
    MVI   A, 0000XXXXB
    OUT   CWAD          ..... Latching count
    IN    CNT0          ..... Read LSB of counter #0
    MOV   L, A
    IN    CNT0          ..... Read MSB of counter #0
    MOV   H, A
    :
RELOAD to counter #0
    MVI   A, 82H        .....
    OUT   CNT0          ..... Load LSB for counter #0
    MVI   A, 53H        .....
    OUT   CNT0          ..... Load MSB for counter #0
```

11. ELECTRIC CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	V_{CC} Suply Voltage (with respect to GND (V_{SS}))	− 0.5V to + 7.0V
V_{IN}	Input Voltage (with respect to GND (V_{SS}))	− 0.5V to + 7.0V
V_{OUT}	Output Voltage (with respect to GND (V_{SS}))	− 0.5V to + 7.0V
P_D	Power Dissipation	1W
T_{sol}	Soldering Temperature (Soldering Time 10 sec)	260°C
T_{stg}	Storage Temperature	− 65°C to + 150°C
T_{opr}	Operating Temperature	0°C to 70°C

050489

11.2 DC CHARACATERISTICS (Ta = 0°C to 70°C, V_{CC} = 5.0V ± 5%, GND = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		− 0.5		0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = − 400μA	2.4			V
I_{IL}	Input Leak Current	$0V \leqq V_{IN} \leqq V_{CC}$			± 10	μA
I_{OFL}	Output Leak Current	$0.45V \leqq V_{OUT} \leqq V_{CC}$			± 10	μA
I_{CC}	Supply Current				140	mA

050489

11.3 INPUT CAPACITANCE (Ta = 25°C, V_{CC} = GND = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	f_C = 1 MHz Unmeasured pins, 0V			10	pF
$C_{I/O}$	Inputy/Output Capacitance				20	pF

050489

11.4 AC CHARACTERISTICS

(Ta = 0°C to 70°C, V_{CC} = 5.0V ± 5%, GND = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AR}	Address Set up Time ($\overline{RD}\downarrow$)		30			ns
t_{RA}	Address Hold Time ($\overline{RD}\uparrow$)		5			ns
t_{RR}	$\overline{RD}$ Pulse Width		300			ns
t_{RD}	Valid Data ($\overline{RD}\downarrow$)	C_L = 150pF			200	ns
t_{DF}	Data Floating ($\overline{RD}\uparrow$)		25		100	ns
t_{RV}	Recovery Time		1			μs
t_{AW}	Address Set up Time ($\overline{WR}\downarrow$)		30			ns
t_{WA}	Address Hold Time ($\overline{WR}\uparrow$)		30			ns
t_{WW}	$\overline{WR}$ Pulse Width		300			ns
t_{DW}	Data Set up Time ($\overline{WR}\uparrow$)		250			ns
t_{WD}	Data Hold Time ($\overline{WR}\uparrow$)		30			ns
t_{CLK}	Clock Period		380		DC	ns
t_{PWH}	CLK High Pulse width		230			ns
t_{PWL}	CLK Low Pulse Width		150			ns
t_{GW}	GATE Width High		150			ns
t_{GL}	GATE Width Low		100			ns
t_{GS}	GATE Set up Time (CLK↑)		100			ns
t_{GH}	GATE Hold Time (CLK↑)		50			ns
t_{OD}	Output Delay From (CLK↓)	C_L = 150pF			400	ns
t_{ODG}	Output Delay From (GATE↓)	C_L = 150pF			300	ns

050489

Note : AC timings measured at V_{OH} = 2.2V, V_{OL} = 0.8V

12. TIMING DIAGRAM

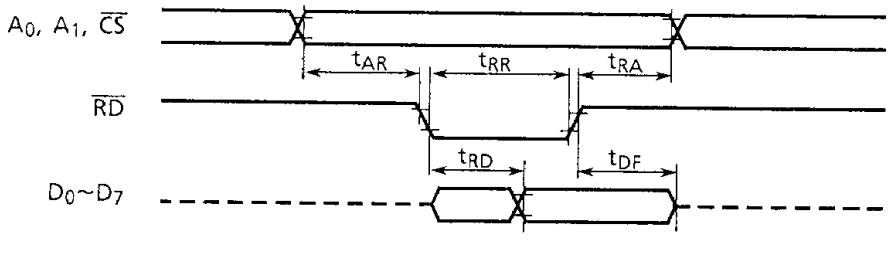


Figure 12.1 Read Timing

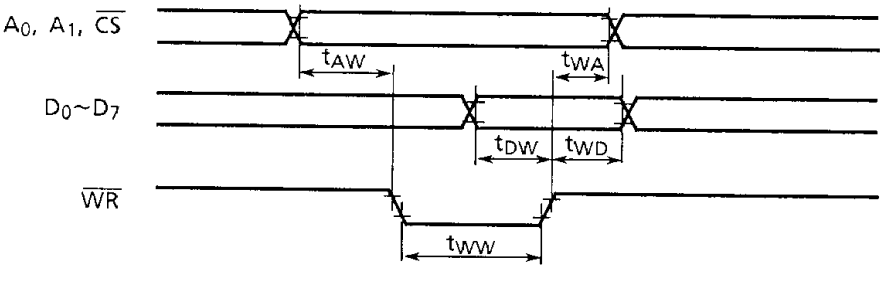


Figure 12.2 Write Timing

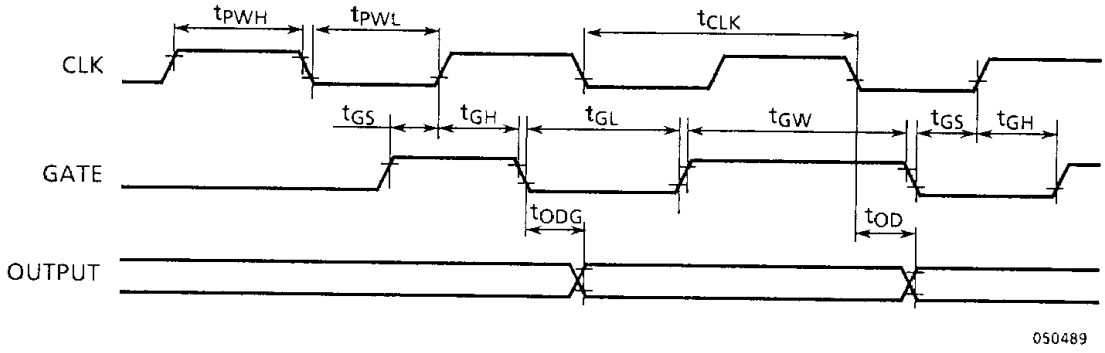


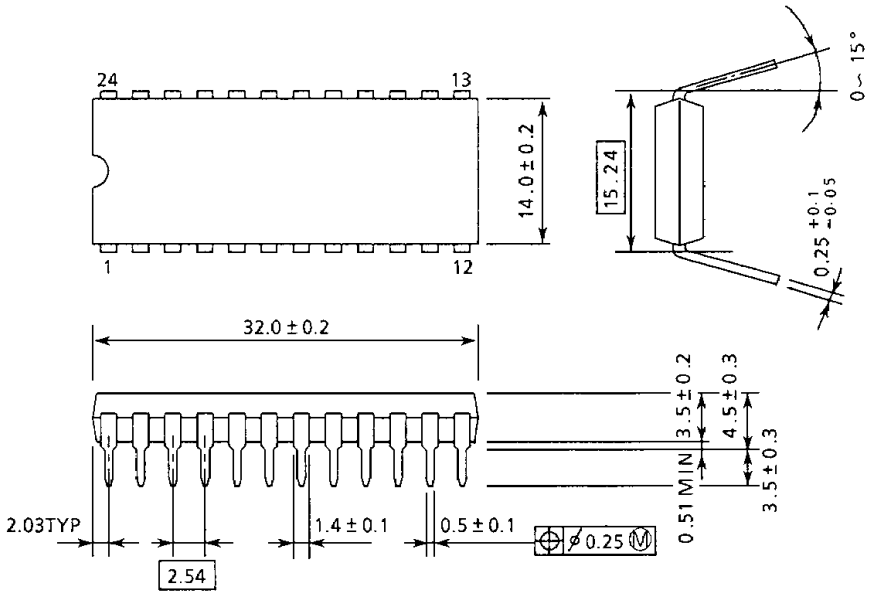
Figure 12.3 Clock & Gate Timing

13. EXTERNAL DIMENSION VIEW

13.1 24PIN DIP

DIP24-P-600

Unit : mm



270289

Note : Lead pitch is 2.54mm and tolerance is ±0.25mm against theoretical center of each lead that is obtained on the basis of No. 1 and No. 24 leads.