Level Translating Fast-Mode Plus I²C-bus/SMbus Repeater

Features

- 2 channel, bidirectional buffer isolates capacitance and allows 540pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds
- Voltage level translation from 0.6V to 5.5V and from 2.2V to 5.5V
- Footprint and functional replacement for PI6ULS5V9617A at Fast-mode speeds
- Port A operating supply voltage range of 0.6V to 5.5V with normal levels($0.4V_{CC(A)} + 0.8V \leqslant V_{CC(B)}$)
- Port B operating supply voltage range of 2.2V to 5.5V with static offset level
- 5V tolerant I²C-bus and enable pins
- 0 Hz to 1 MHz clock frequency (the maximum system operating frequency may be less than 1MHz because of the delays added by the repeater)
- Active HIGH repeater enable input referenced to $V_{CC(B)}$
- Open-drain input/outputs
- Latching free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode, Fast-mode and Fast-mode Plus I²C-bus devices, SMBus (standard and high power mode), PMBus and multiple masters
- Powered-off high-impedance I²C-bus pins
- ESD protection exceeds 8000V HBM per JESD22-A114
- Package: MSOP-8L, SOIC-8L and TDFN2x3-8L

Pin Description

Pin Name	Description
$V_{CC(A)}$	port A supply voltage (0.6V to 5.5V)
SCLA	serial clock port A bus
SDAA	serial data port A bus
GND	supply ground (0 V)
EN	active HIGH repeater enable input
SDAB	serial data port B bus
SCLB	serial clock port B bus
$V_{CC(B)}$	port B supply voltage (2.2V to 5.5V)

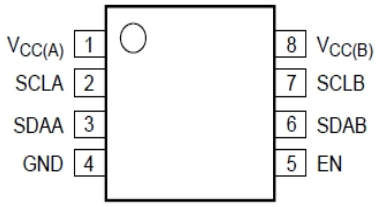
Description

The PI6ULS5V9617A is a CMOS integrated circuit intended for Fast-mode Plus (Fm+) I²C-bus or SMBus applications. It can provide level shifting between low voltage (down to 0.6V) and higher voltage (2.2V to 5.5V) in mixed-mode applications.

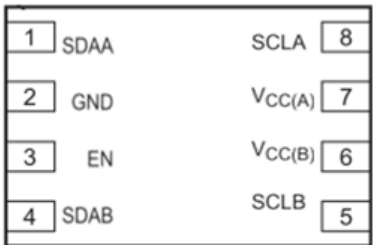
The PI6ULS5V9617A enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I²C devices or longer trace length. It also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 540 pF at 1 MHz or up to 4000 pF at lower speeds. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the PI6ULS5V9617A is unpowered.

The 2.2V to 5.5V bus port B drivers have the static level offset, while the adjustable voltage bus port A drivers eliminate the static offset voltage. This results in a LOW on the port B translating into a nearly 0V LOW on the port A which accommodates the smaller voltage swings of lower voltage logic. The EN pin is referenced to $V_{CC(B)}$ and can also be used to turn the drivers on and off under system control.

Pin Configuration

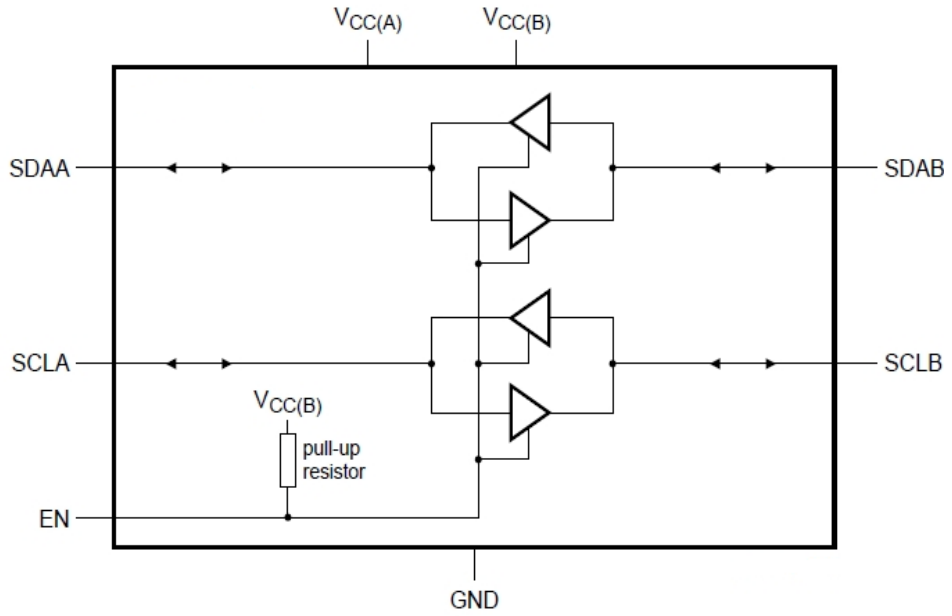


MSOP-8L, SOIC-8L(Top View)



TDFN2*3-8L(Top View)

Block Diagram



EN	Function
H	SCLA = SCLB; SDAA = SDAB;
L	disabled

Figure 1: Block Diagram

Maximum Ratings

Storage Temperature	-55°C to +125°C
Supply Voltage port B	-0.5V to +6.0V
Supply Voltage port A	-0.5V to+6.0V
DC Input Voltage	-0.5V to +6.0V
Control Input Voltage (EN)	-0.5V to+6.0V
Total Power Dissipation	100mW
Input /Output Current (port A&B)	50mA
Input current (EN, VCCA, VCCB, GND)	50mA
ESD: HBM Mode	8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

$V_{CC(A)}$ = 0.6V to 5.5V(1); $V_{CC(B)}$ = 2.2V to 5.5V; GND = 0V; T_A = -40 ℃ to +85 ℃; unless otherwise noted.

Symbol	Parameter	CONDITIONS	Min	Typ	Max	Unit
$V_{CC(B)}$	supply voltage port B	-	2.2	-	5.5	V
$V_{CC(A)}$	supply voltage port A	-	0.6	-	5.5	V
$I_{CC(A)}$	supply current on pin $V_{CC(A)}$	$V_{CC(A)}$= 0.95V	-	-	8	µA
		$V_{CC(A)}$= 5.5V	-	-	50	
$I_{CCH(B)}$	port B HIGH-level supply current	$V_{CC(B)}$ = 5.5 V SDAn = SCLn = $V_{CC(n)}$	-	0.8	2.5	mA
$I_{CCL(B)}$	port B LOW-level supply current	$V_{CC(B)}$ = 5.5 V; one SDA and one SCL = GND; other SDA and SCL open (with pull-up resistors)	-	1.7	2.9	mA
$I_{QVC(B)}$	Quiescent current on $V_{CC(B)}$	EN=GND;$V_{CC(B)}$=5.5V	-	0.4	0.8	mA

Note:

(1) $V_{CC(A)}$ may be as high as 5.5 V for over voltage tolerance but $0.4V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and functional normally.

DC Electrical Characteristics

$V_{CC(A)}$ = 0.6V to 5.5V[5]; $V_{CC(B)}$ = 2.2V to 5.5V; GND = 0V; T_A = -40 ℃ to +85 ℃; Typical values measured with $V_{CC(A)}$ = 0.95V and $V_{CC(B)}$ = 2.5V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage	-	$0.7V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage	-	-0.5	-	+0.4	V
V_{IK}	Input clamping voltage	I_I = -18 mA	-1.2	-	-	V
I_{LI}	Input leakage current	V_I = 5.5V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 150μA at $V_{CC(B)}$ = 2.2V[1]	0.47	-	-	V
		I_{OL} = 13mA at $V_{CC(B)}$ = 2.2V[2]	-	0.54	0.60	V
V_{OL} - V_{IL}	Difference between LOW-level output and LOW-level input voltage contention	V_{OL} at I_{OL} = 1 mA; guaranteed by design	60	90	160	mV
C_{io}	Input/output capacitance	V_I = 3V or 0V; $V_{CC(B)}$ = 3.3V; EN = LOW	-	7	10	pF
		V_I = 3V or 0V; $V_{CC(B)}$ = 0V	-	7	10	pF
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage	-	$0.7V_{CC(A)}$	-	5.5	V
V_{IL}	LOW-level input voltage	-	-0.5[3]	-	$+0.25V_{CC(A)}$[4]	V
V_{IK}	Input clamping voltage	I_I = -18 mA	-1.2	-	-	V
I_{LI}	Input leakage current	V_I = 5.5V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 13mA at $V_{CC(B)}$ = 2.2V	-	0.1	0.2	V
C_{io}	Input/output capacitance	V_I = 3V or 0V; $V_{CC(B)}$ = 3.3V; EN = LOW	-	7	10	pF
		V_I = 3V or 0V; $V_{CC(B)}$ = 0V	-	7	10	pF
Enable						
V_{IH}	HIGH-level input voltage	-	$0.7V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage	-	-0.5	-	$+0.3V_{CC(B)}$	V
I_{LI}	Input leakage current	V_I = $V_{CC(B)}$	-1	-	+1	μA
I_{IL}	LOW-level input current	V_I = 0.2V, EN; $V_{CC(B)}$ = 2.2V;	-18	-7	-	μA
C_{io}	Input capacitance	V_I = $V_{CC(B)}$	-	6	-	pF

Note:

(1) Pull-up should result in $I_{OL} \geq 150\mu A$.
(2) Guaranteed by design and characterization.
(3) V_{IL} for port A with envelope noise must be below $0.3V_{CC(A)}$ for stable performance.
(4) When $V_{CC(A)}$ is less than 1V, care is required to make certain that the system ground offset and noise is minimized such that there is reasonable difference between the V_{IL} present at the PI6ULS5V9617 A-side input and the $0.25V_{CC(A)}$ input threshold.
(5) $V_{CC(A)}$ may be as high as 5.5 V for over voltage tolerance but $0.4V_{CC(A)} + 0.8V \leqslant V_{CC(B)}$ for the channels to be enabled and functional normally.

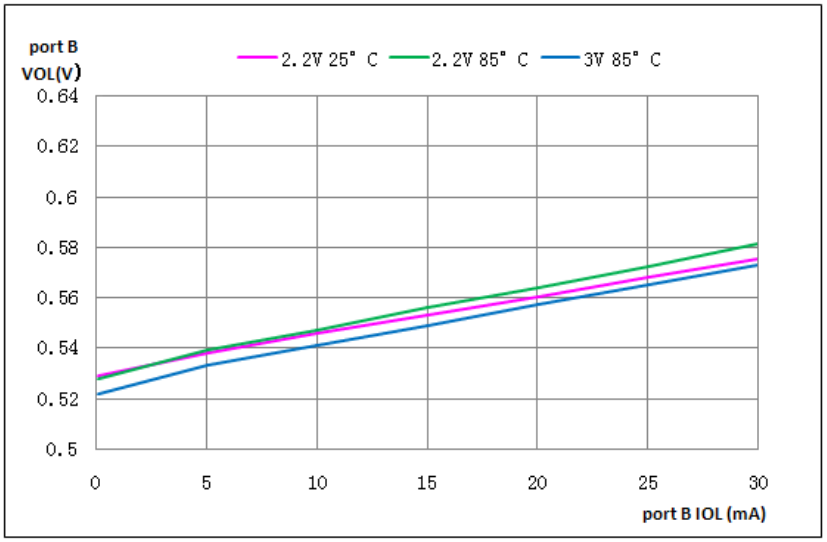


Figure 2:
Port B V_{OL} versus I_{OL}

Condition:
V_{CCB}=2.2V, T_A=25° C
V_{CCB}=2.2V,T_A=85° C
V_{CCB}=3V, T_A=85° C

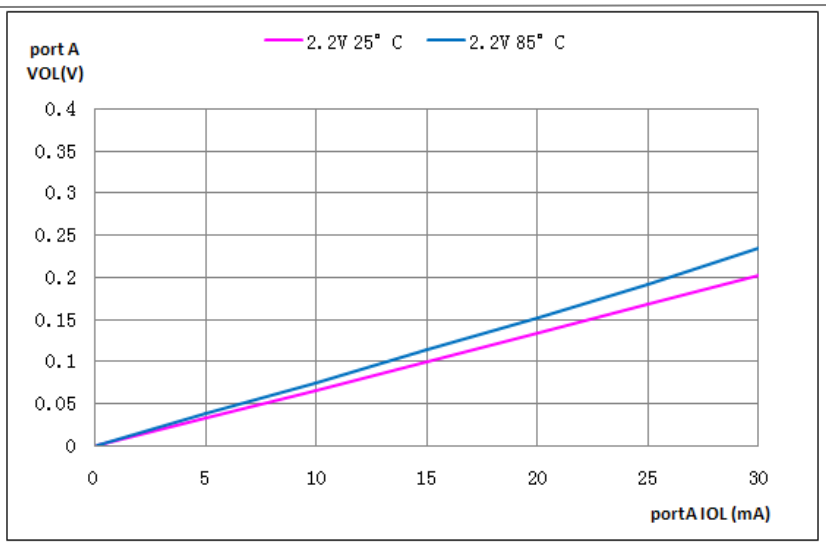


Figure 3:
Port A V_{OL} versus I_{OL}

Condition:
V_{CCA}=2.2V, T_A=25° C
V_{CCA}=2.2V, T_A=85° C

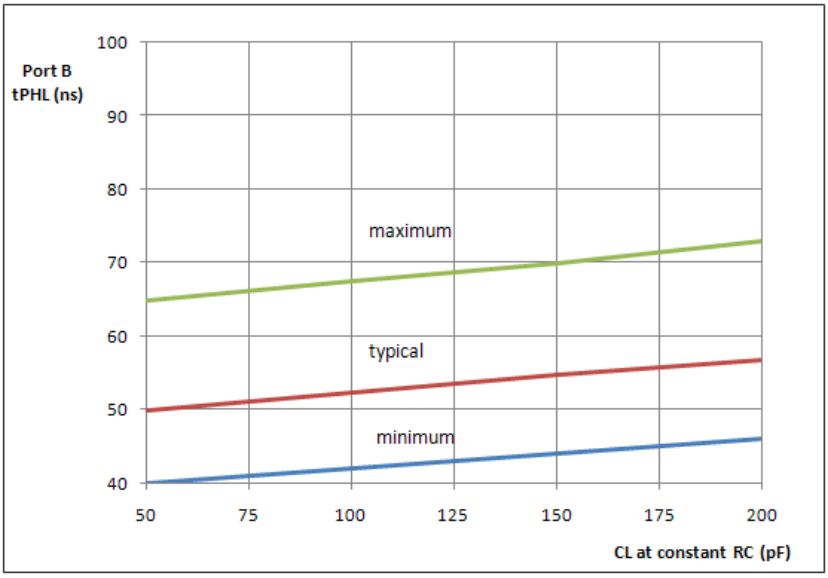


Figure 4:
Nominal port B t_{PHL} with load capacitance at constant RC

Condition:
RC = 67.5 ns, $V_{CC(A)}$ = 0.95 V,
$V_{CC(B)}$ = 2.5 V, T_A=25° C

Dynamic characteristics

$V_{CC(A)}$ = 0.6V to 5.5V[8]; $V_{CC(B)}$ = 2.2V to 5.5V; GND = 0V; T_A = -40 ℃ to +85 ℃; Typical values measured with $V_{CC(A)}$ = 0.95V and $V_{CC(B)}$ = 2.5V, unless otherwise noted.[1][2]

Symbol	Parameter	Conditions	Min	Typ[3]	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	B-side to A-side	-	-52	-103	ns
t_{PLH2}[4]	LOW-to-HIGH propagation delay2	B-side to A-side	-	94	130	ns
t_{PHL}	HIGH-to-LOW propagation delay	B-side to A-side	-	76	152	ns
t_{TLH}[5]	LOW-to-HIGH transition time	A-side	-	60	-	ns
SRf	Falling slew rate	port A; $0.7V_{CC(A)}$ to $0.3V_{CC(A)}$	-	0.037	-	ns
t_{PLH}[6]	LOW-to-HIGH propagation delay	A-side to B-side	-	45	102	ns
t_{PHL}[6]	HIGH-to-LOW propagation delay	A-side to B-side	-	50	173	ns
t_{TLH}	LOW-to-HIGH transition time	B-side	-	60	-	ns
t_{THL}	HIGH-to-LOW transition time	B-side	-	30	76	ns
t_{en}[7]	Enable time	Quiescent -0.3 V; EN HIGH to enable;	-	-	100	ns
t_{dis}[7]	Disable time	quiescent + 0.3 V; EN LOW to disable;	-	-	100	ns

Note:

(1) Times are specified with loads of 1.35 kΩ pull-up resistance and 50 pF load capacitance on port A and port B, and a falling edge slew rate of 0.05 V/ns input signals.
(2) Pull-up voltages are $V_{CC(A)}$ on port A and VCC(B) on port B.
(3) Typical values were measured with $V_{CC(A)}$ = 0.95 V, $V_{CC(B)}$=2.5V at T_A = 25 ℃, unless otherwise noted.
(4) The t_{PLH2} delay data from port B to port A is measured at 0.45 V on port B to $0.5V_{CC(A)}$ on port A.
(5) The t_{TLH} of the bus is determined by the pull-up resistance (1.35 k Ω) and the total capacitance (50 pF).
(6) The proportional delay data from port A to port B is measured at $0.5V_{CC(A)}$ on port A to $0.5V_{CC(B)}$) on port B.
(7) The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.
(8) $V_{CC(A)}$ may be as high as 5.5 V for over voltage tolerance but $0.4V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and functional normally.

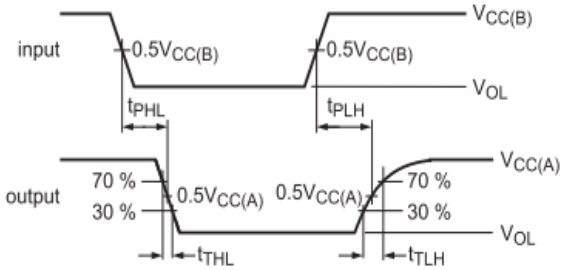


Figure 5: Propagation Delay and Transition Times B→A

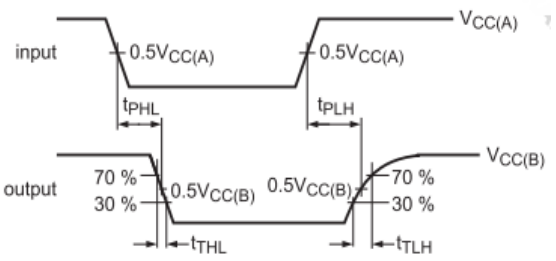
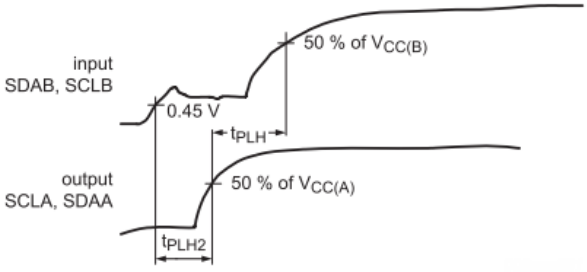


Figure 6: Propagation Delay and Transition Times A→B



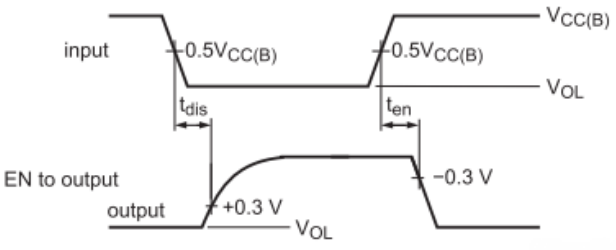
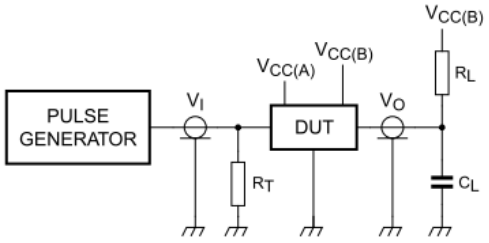


Figure7: Propagation Delay and Enable and disable time



R_L = load resistor; 1.35 kΩ on port B
C_L = load capacitance includes jig and probe capacitance; 50 pF
R_T = termination resistance should be equal to Z_0 of pulse generators

Figure 8: Test Circuit

Functional Description

The PI6ULS5V9617A enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 0.6V without degradation of system performance. The PI6ULS5V9617A contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.6V) and a 2.5V, 3.3V or 5V I²C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5V even when the device is unpowered ($V_{CC(B)}$ and/or $V_{CC(A)}$ = 0V).

The PI6ULS5V9617A includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.2V and until after the internal reference circuits have settled at about 400µs, and the $V_{CC(A)}$ is above 0.6V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up.

The PCA9617A includes a $V_{CC(A)}$ overvoltage disable that turns the channel off if $0.4V_{CC(A)} + 0.8V > V_{CC(B)}$. The PCA9617A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

The B-side drivers operate from 2.2V to 5.5V. The output low level of port B internal buffer is approximately 0.55 V, while the input voltage must be 90mV lower (0.45V) or even more lower. The nearly 0.5V low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design on B port prevents it from being used in series with another PI6ULS5V9617A (B side) or similar devices, because they don't recognize buffer low signals as a valid low.

The A-side drivers operate from 0.6V to 5.5 V. The output low level of port A internal buffer is nearly 0V, while the input low level is set at $0.35V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.6V. Port A of two or more PI6ULS5V9617As can be connected together to allow a star topography with port A on the common bus. And port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PI6ULS5V9617As can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

After power-up and with the EN HIGH, a LOW level on port A (below $0.3V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55 V. When port A rises above $0.3V_{CC(A)}$, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4 V, the port A driver is turned on and port A pulls down to about 0 V. The port A pull-down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage goes below 0.4 V, the port B pull-down driver is enabled and port B will only be able to rise to 0.55 V until port A rises above $0.3V_{CC(A)}$, then port B will continue to rise being pulled up by the external pull-up resistor. The $V_{CC(A)}$ is only used to provide the $0.35V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PI6ULS5V9617A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

The EN pin is active HIGH with thresholds referenced to $V_{CC(B)}$ and an internal pull-up to $V_{CC(B)}$ that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled. The enable does not switch the internal reference circuits so the 400µs delay is only seen when $V_{CC(B)}$ comes up. The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I²C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I²C-bus devices only specify 3mA output drive; this limits the termination current to 3mA in a generic I²C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30mA at 5 V drive strength, then lower value pull-up resistors can be used. The B-side RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

Application Information

A typical application is shown in Figure 9. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 1MHz. Master devices can be placed on either bus.

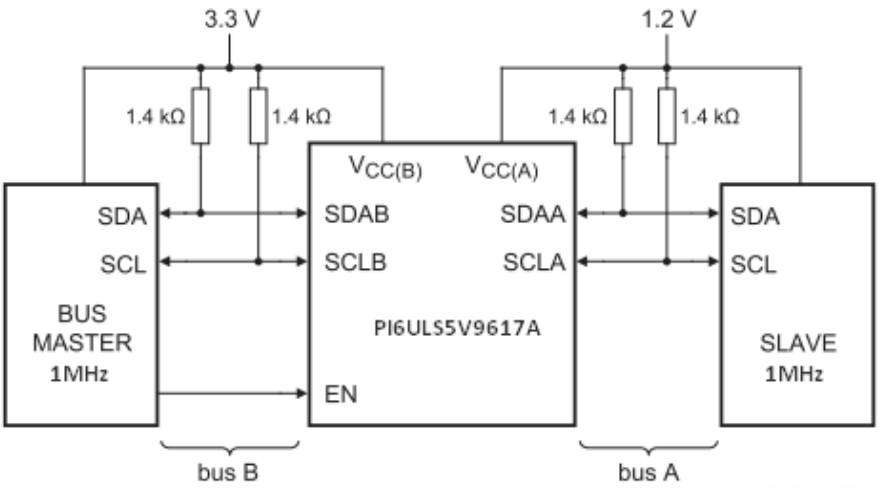


Figure 9: Typical Application

The PI6ULS5V9617A is 5V tolerant, so it does not require any additional circuitry to translate between 0.6V to 5.5V bus voltages and 2.2 V to 5.5 V bus voltages.

When port A of the PI6ULS5V9617A is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PI6ULS5V9617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 9 were to write to the slave through the PI6ULS5V9617A, waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 0.6V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the PI6ULS5V9617A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PI6ULS5V9617A. After the eighth clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PI6ULS5V9617A for a short delay while the A bus side rises above $0.3V_{CC(A)}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PI6ULS5V9617A (V_{IL}) be at or below 0.4 V to be recognized by the PI6ULS5V9617A and then transmitted to the A bus side.

Multiple PI6ULS5V9617A port A sides can be connected in a star configuration (Figure 10), allowing all nodes to communicate with each other.

Multiple PI6ULS5V9617As can be connected in series as long as port A is connected to port B(Figure 11). I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

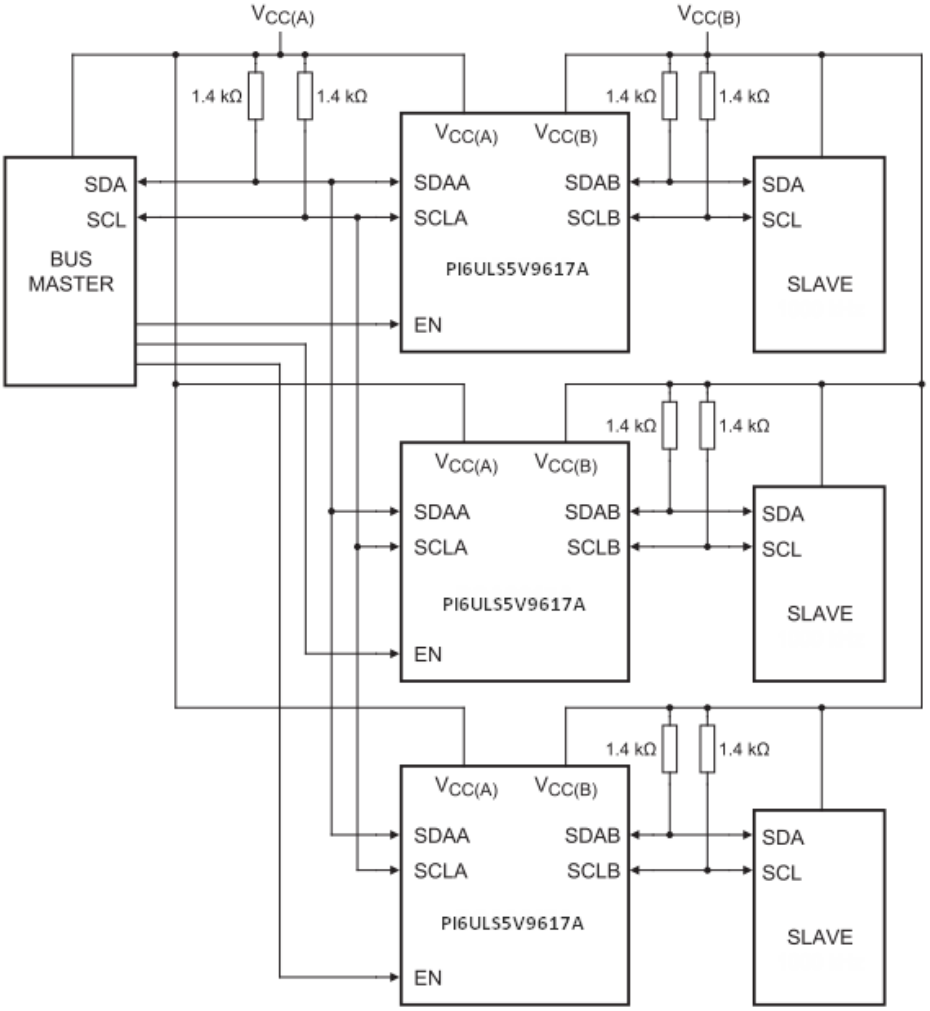


Figure 10: Typical Star Application

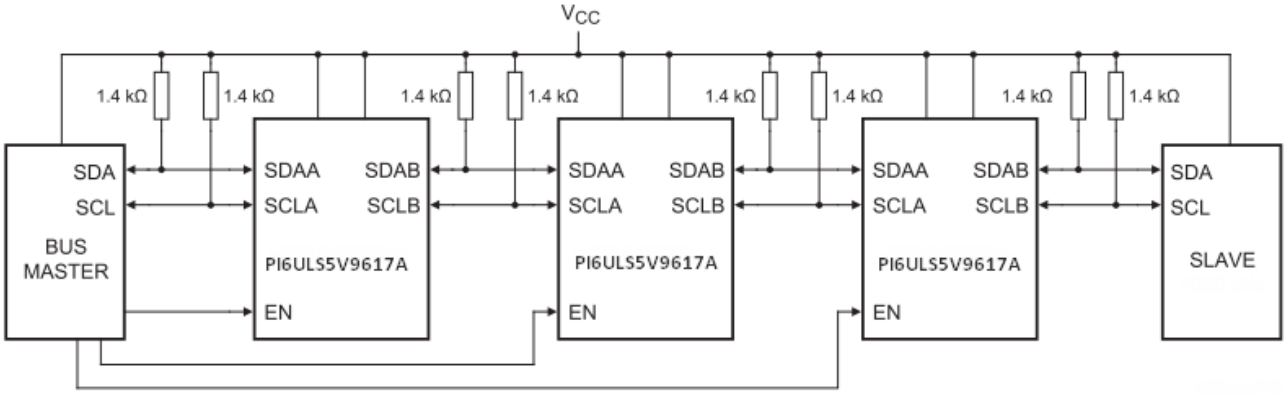


Figure 11: Typical Series Application

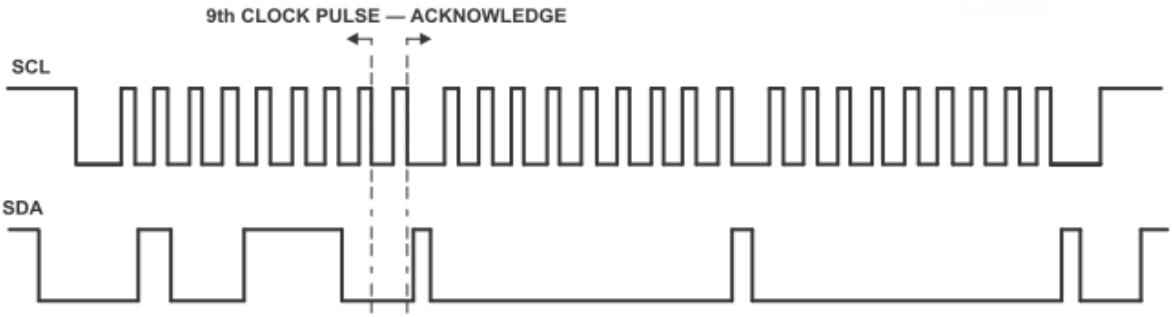


Figure 12: Bus A (0.6V to 5.5V Bus) Waveform

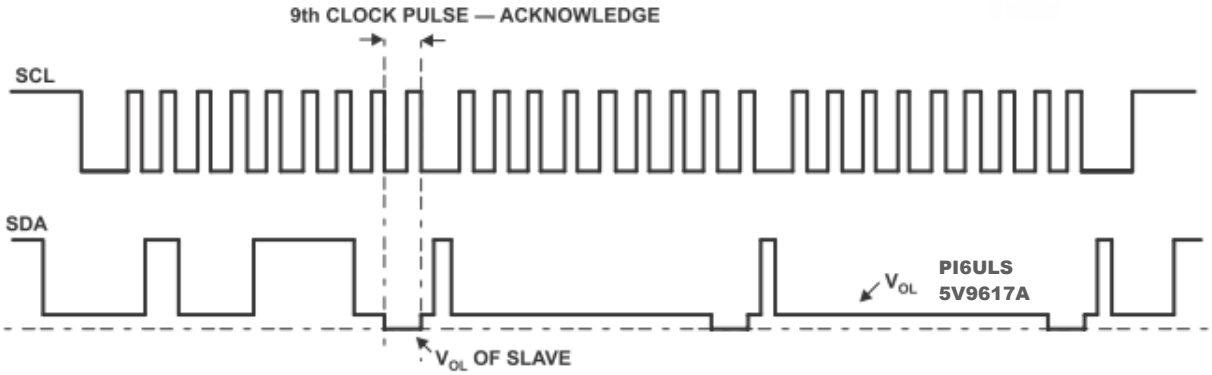
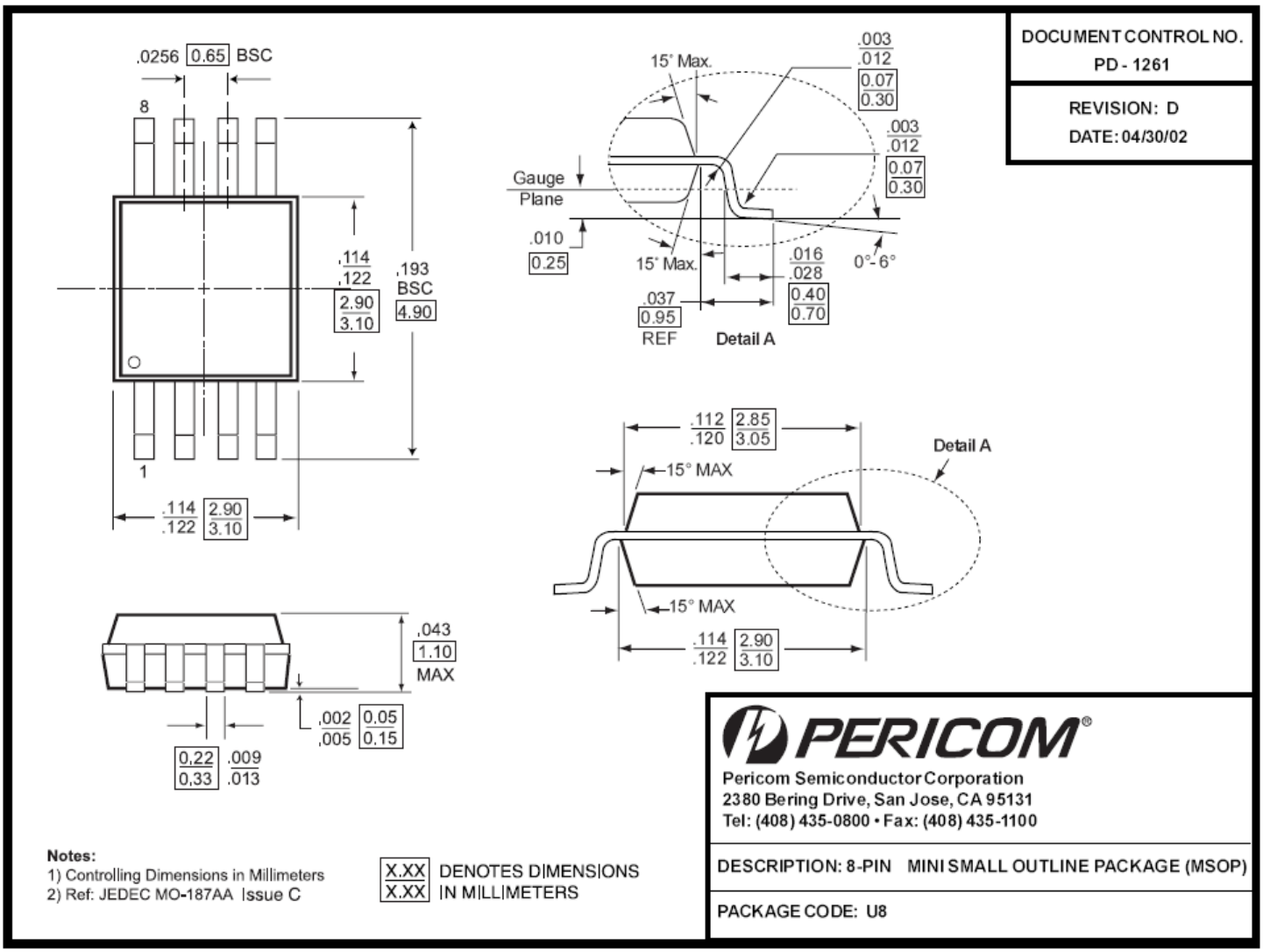


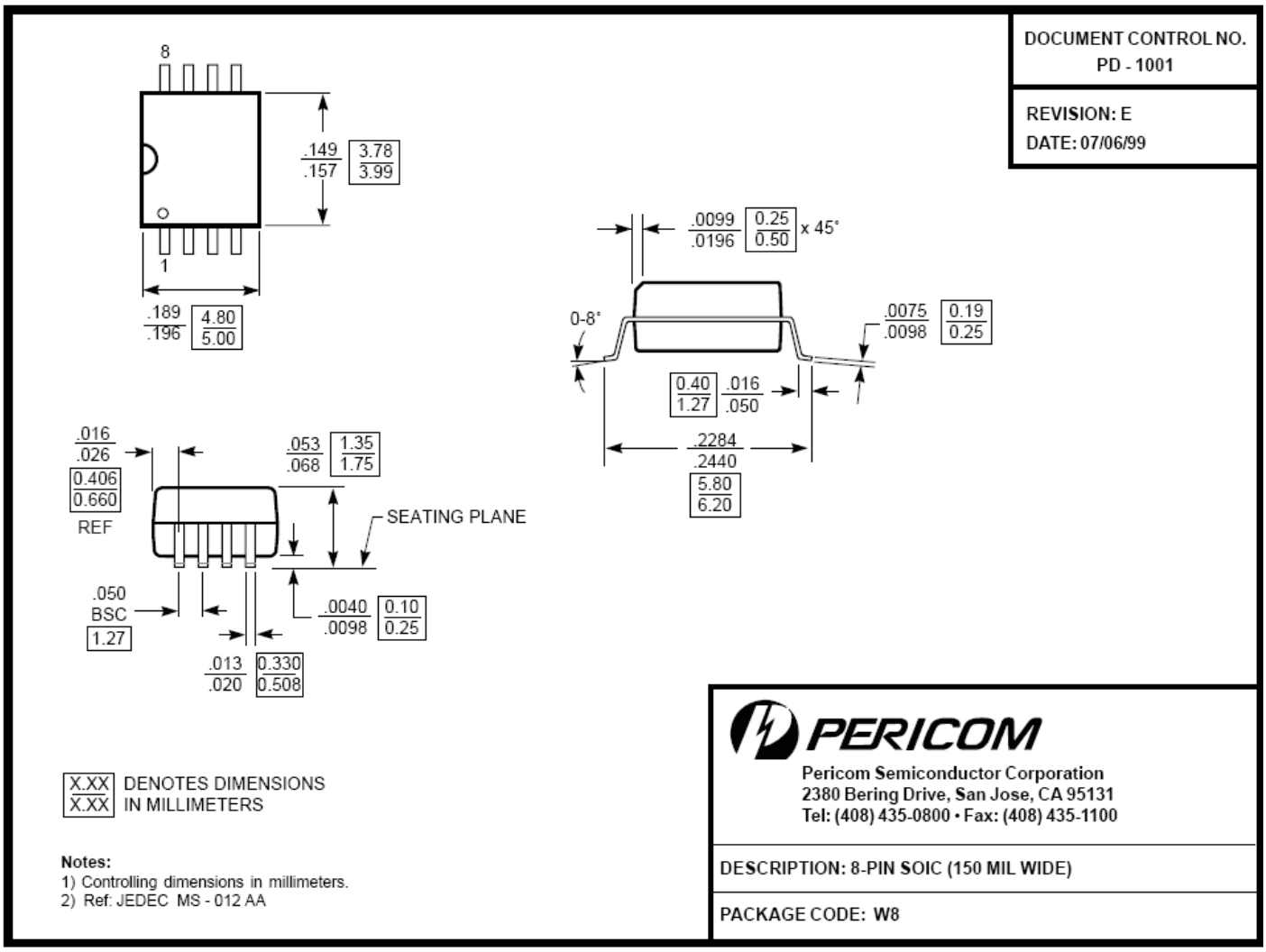
Figure 13: Bus B (2.2V to 5.5V Bus) Waveform

Mechanical Information

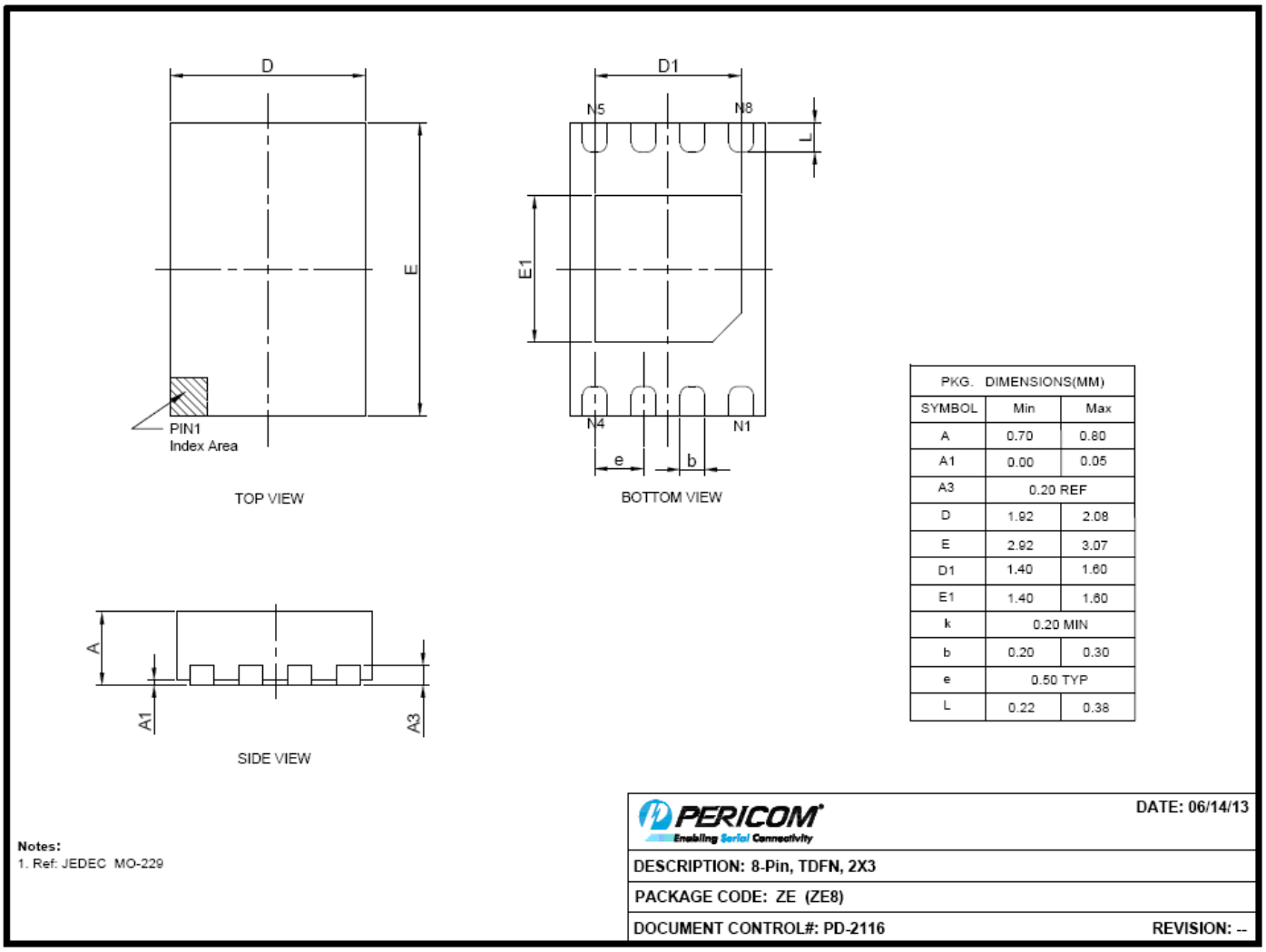
MSOP-8L



SOIC-8L


DOCUMENT CONTROL NO.
PD - 1001
REVISION: E
DATE: 07/06/99
8
1
.149 / .157 3.78 / 3.99
.189 / .196 4.80 / 5.00
.0099 / .0196 0.25 / 0.50 x 45°
0-8°
.0075 / .0098 0.19 / 0.25
0.40 / 1.27 .016 / .050
.2284 / .2440 5.80 / 6.20
.016 / .026 0.406 / 0.660 REF
.053 / .068 1.35 / 1.75
SEATING PLANE
.050 BSC 1.27
.0040 / .0098 0.10 / 0.25
.013 / .020 0.330 / 0.508
X.XX / X.XX DENOTES DIMENSIONS IN MILLIMETERS
Notes:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS - 012 AA
PERICOM
Pericom Semiconductor Corporation
2380 Bering Drive, San Jose, CA 95131
Tel: (408) 435-0800 • Fax: (408) 435-1100
DESCRIPTION: 8-PIN SOIC (150 MIL WIDE)
PACKAGE CODE: W8

TDFN2x3-8L



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Notes:
1. Ref: JEDEC MO-229

PERICOM Enabling Serial Connectivity

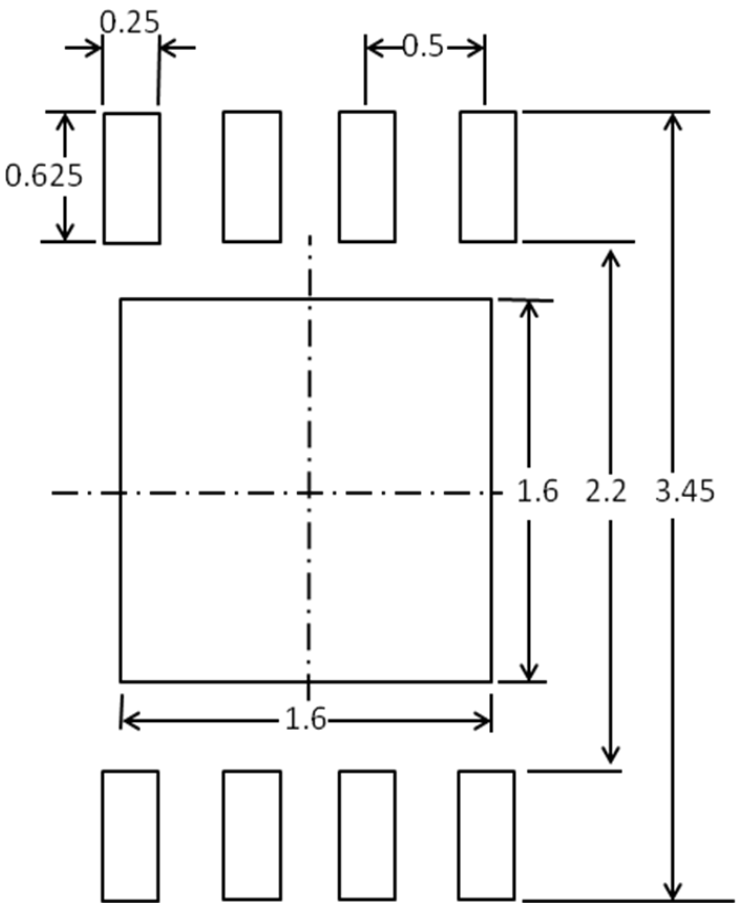
DATE: 06/14/13

DESCRIPTION: 8-Pin, TDFN, 2X3

PACKAGE CODE: ZE (ZE8)

DOCUMENT CONTROL#: PD-2116 REVISION: --

Recommended Land pattern for TDFN 2x3-8L



Note:
All linear dimensions are in millimeters

Ordering Information

Part No.	Package Code	Package
PI6ULS5V9617AUE	U	Lead free and Green 8-pin MSOP
PI6ULS5V9617AWE	W	Lead free and Green 8-pin SOIC
PI6ULS5V9617AZEE	ZE	Lead free and Green 8-pin TDFN2x3

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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