HD74SSTV16859

1:2 13-bit SSTL_2 Registered Buffer

REJ03D0832-0900
(Previous: ADE-205-337H)
Rev.9.00
Apr 07, 2006

Description

The HD74SSTV16859 is a 1:2 13-bit registered buffer designed for 2.3 V to 2.7 V Vcc operation and LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to QA, QB is controlled by differential clock pins (CLK, $\overline{\text{CLK}}$) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Features

- Supports LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16859TEL	TSSOP-64 pin	PTSP0064KA-A (TTP-64DV)	T	EL (1,000 pcs / Reel)

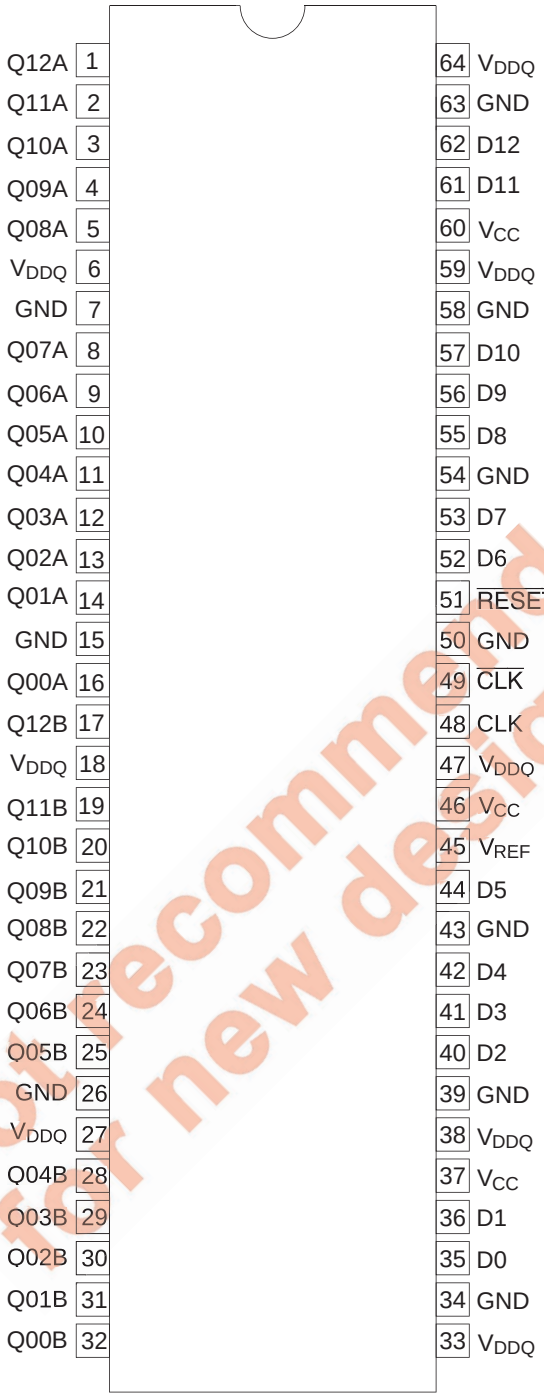
Not recommend for new design

Function Table

Inputs				Outputs	
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	QA	QB
L	X	X	X	L	L
H	↓	↑	H	H	H
H	↓	↑	L	L	L
H	L or H	H or L	X	Q_0 *1	Q_0 *1

H : High level
L : Low level
X : Immaterial
↑ : Low to high transition
↓ : High to low transition
Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Not recommend for new design

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	–0.5 to 3.6	V	
Input voltage [*1]	V_I	–0.5 to V_{DDQ}+0.5	V	
Output voltage [*1]	V_O	–0.5 to V_{DDQ}+0.5	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}
V_{CC}, V_{DDQ} or GND current / pin	I_{CC}, I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air)	P_T	1	W	TSSOP
Storage temperature	Tstg	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

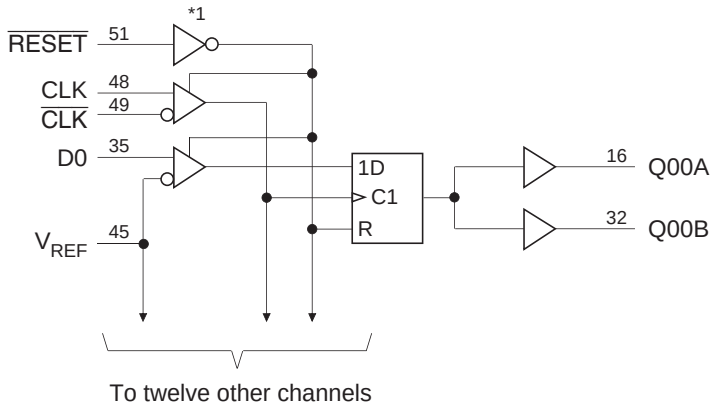
Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage		V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage		V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage		V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage		V_{TT}	V_{REF}–40 mV	V_{REF}	V_{REF}+40 mV	V	
Input voltage		V_I	0	—	V_{CC}	V	
AC high level input voltage		V_{IH}	V_{REF}+310 mV	—	—	V	D
AC low level input voltage		V_{IL}	—	—	V_{REF}–310 mV	V	D
DC high level input voltage		V_{IH}	V_{REF}+150 mV	—	—	V	D
DC low level input voltage		V_{IL}	—	—	V_{REF}–150 mV	V	D
High level input voltage		V_{IH}	1.7	—	V_{DDQ}+0.3	V	$\overline{\text{RESET}}$
Low level input voltage		V_{IL}	–0.3	—	0.7	V	$\overline{\text{RESET}}$
Differential input voltage	(Common mode range)	V_{CMR}	0.97	—	1.53	V	CLK, $\overline{\text{CLK}}$
	(Minimum peak to peak input)	V_{PP}	360	—	—	mV	CLK, $\overline{\text{CLK}}$
High level output current		I_{OH}	—	—	–20	mA	
Low level output current		I_{OL}	—	—	20	mA	
Operating temperature		Ta	0	—	70	°C	

Note: The $\overline{\text{RESET}}$ input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

Not recommend for new design

Logic Diagram



Note: 1. $\overline{\text{RESET}}$ input gate is connected to V_{DDQ}.

Electrical Characteristics

Item		Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage		V_{IK}	2.3	—	—	–1.2	V	I_{IN} = –18 mA
Output voltage		V_{OH}	2.3 to 2.7	V_{CC}–0.2	—	—	V	I_{OH} = –100 µA
			2.3	1.95	—	V_{DDQ}		I_{OH} = –16 mA
		V_{OL}	2.3 to 2.7	—	—	0.2		I_{OL} = 100 µA
			2.3	0	—	0.35		I_{OL} = 16 mA
Input current	(All inputs)	I_{IN}	2.7	—	—	±5	µA	V_{IN} = 2.7 V or 0
Quiescent supply current		I_{CC} *2	2.7	—	—	45	mA	V_{IN} = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0
Standby current		$I_{CC\ (stdy)}$	2.7	—	—	10	µA	$\overline{\text{RESET}}$ = GND
Dynamic operating clock only		I_{CCD} *2	2.7	—	—	90	µA/ clock MHz	$\overline{\text{RESET}}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle
Dynamic operating per each data input		I_{CCD} *2	2.7	—	—	20	µA/ clock MHz/ data input	$\overline{\text{RESET}}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.
Output high *3		r_{OH}	2.3 to 2.7	7	—	22 *4	Ω	I_{OH} = –20 mA
Output low *3		r_{OL}	2.3 to 2.7	7	—	22 *4	Ω	I_{OL} = 20 mA
$\lvert r_{OH} - r_{OL} \rvert$ each separate bit *3		$r_{O(\Delta)}$	2.5	—	—	4	Ω	I_O = 20 mA, Ta = 25°C
Input capacitance	Data inputs	C_{IN}	2.5 *1	2.5	—	3.5	pF	V_I = V_{REF}±310 mV
	CLK and $\overline{\text{CLK}}$			2.5	—	3.5		V_{CMR} = 1.25 V, V_{PP} = 360 mV
	$\overline{\text{RESET}}$			—	3.0	—		V_I = V_{CC} or GND

Notes: 1. All typical values are at V_{CC} = 2.5 V, Ta = 25°C.
2. Total I_{CC} (max) = I_{CC} + {I_{CCD} (clock)×f(clock)} + {I_{CCD} (Data)×1/2f(clock)×13}
3. This is effective in the case that it did terminate by resistance.
4. See figure. 1, 2

Not recommend for new design

Switching Characteristics

Item		Symbol	V_{CC} = 2.5 ± 0.2 V		Unit	Test Condition
			Min	Max		
Clock frequency *1		f_{clock}	—	200	MHz	
Setup time	Fast slew rate *4, 6	t_{su}	0.75	—	ns	Data before CLK↑, $\overline{CLK}$↓
	Slow slew rate *5, 6		0.9	—		
Hold time	Fast slew rate *4, 6	t_h	0.75	—	ns	Data after CLK↑, $\overline{CLK}$↓
	Slow slew rate *5, 6		0.9	—		
Differential inputs active time		t_{act}	22	—	ns	Data inputs must be low after $\overline{RESET}$ high.
Differential inputs inactive time		t_{inact}	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ low.
Pulse width		t_w	2.5	—	ns	CLK, $\overline{CLK}$ "H" or "L"
Output slew *3		t_{SL}	1	4	volt/ns	

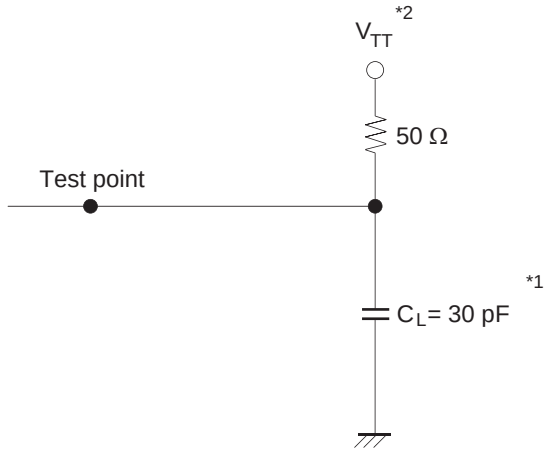
(C_L = 30 pF, R_L = 50 Ω, V_{REF} = V_{TT} = V_{DDQ} × 0.5)

Item	Symbol	V_{CC} = 2.5 ± 0.2 V			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f_{max}	200	—	—	MHz		
Propagation delay time *2	t_{PLH}, t_{PHL}	1.1	—	2.8	ns	CLK, $\overline{CLK}$	QA, QB
	t_{PHL}	—	—	5.0		$\overline{RESET}$	QA, QB

Notes: 1. Although the clock is differential, all timing is relative to CLK going high and $\overline{CLK}$ going low.
2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
6. CLK, $\overline{CLK}$ signals input slew rates are ≥ 1 V/ns.

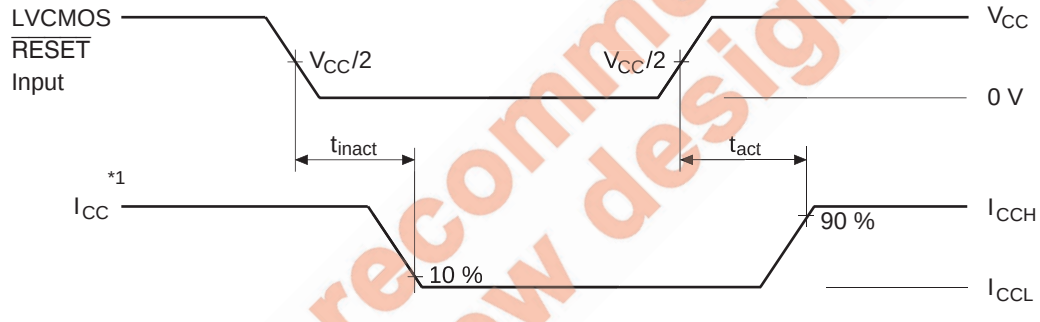
Not recommend for new design

Test Circuit

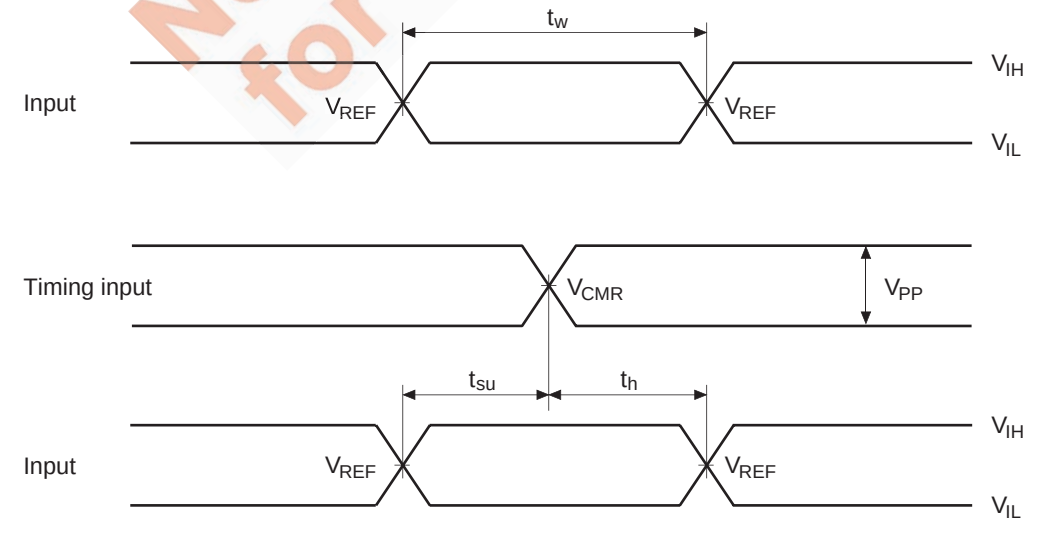


Notes: 1. C_L includes probe and jig capacitance.
2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

Waveforms – 1

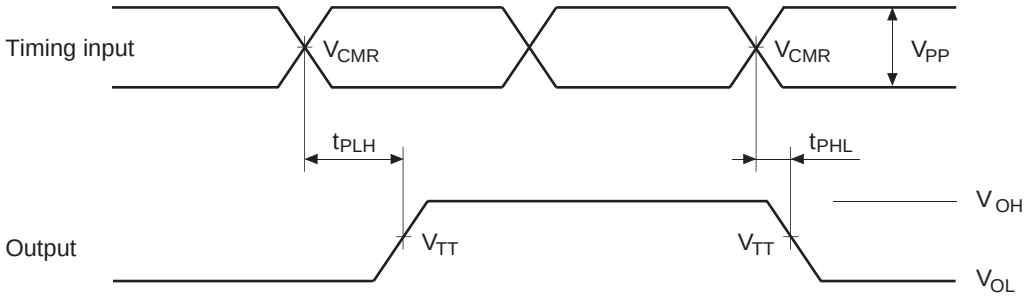


Waveforms – 2

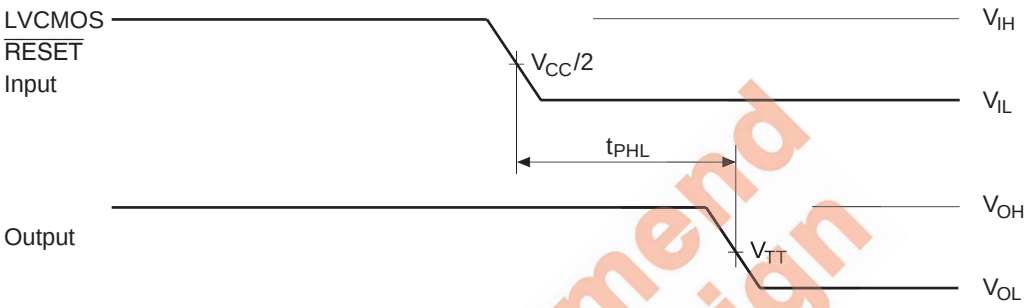


Not recommend for new design

Waveforms – 3



Waveforms – 4



Notes:
1. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
2. All input pulses are supplied by generators having the following characteristics : PRR ≤ 10 MHz, Zo = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
3. The outputs are measured one at a time with one transition per measurement.
4. $V_{TT} = V_{REF} = V_{DDQ}/2$
5. $V_{IH} = V_{REF}$+310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
6. $V_{IL} = V_{REF}$–310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
7. t_{PLH} and t_{PHL} are the same as t_{pd}

Not recommend for new design

Application Data

• Pull-down

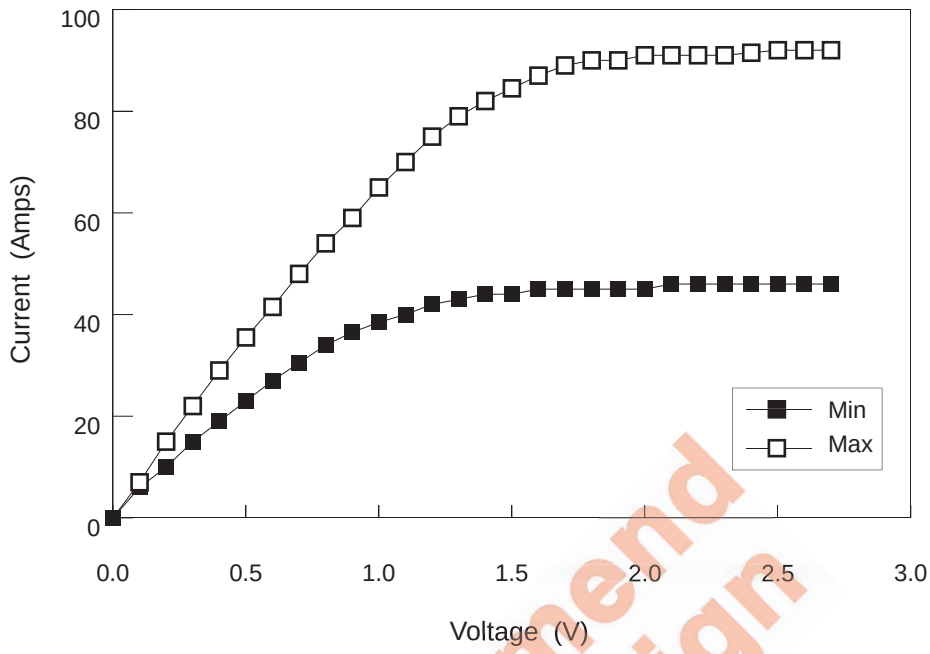


Figure 1

• Pull-up

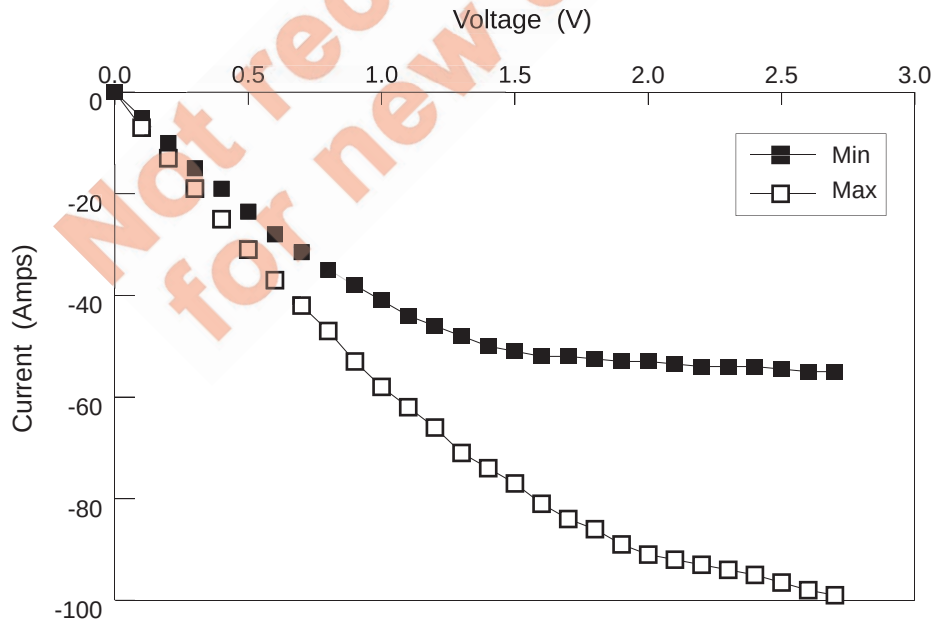


Figure 2

Not recommend for new design

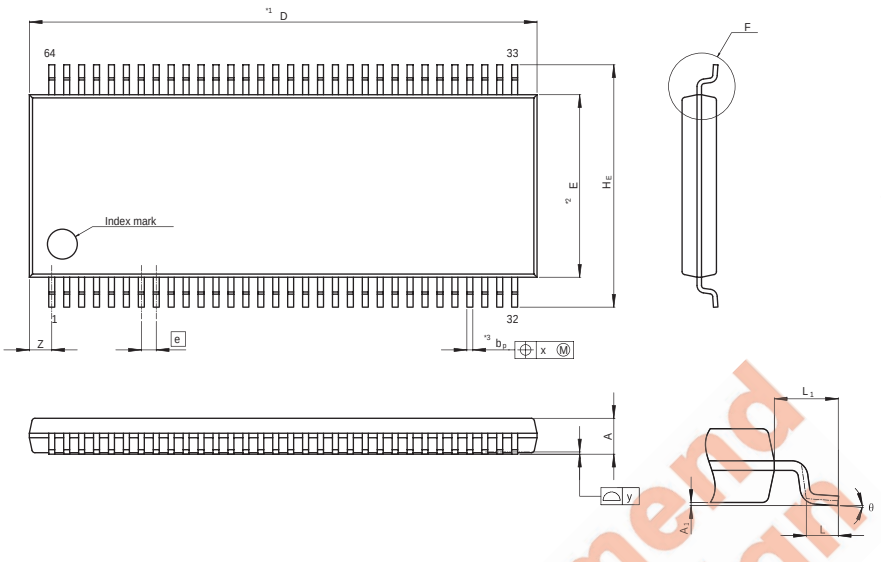
Curve Data

Voltage (V)	Pull-down		Pull-up	
	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Max	Min	Max
0.0	0	0	0	0
0.1	6	7	–5	–7
0.2	10	15	–10	–13
0.3	15	22	–15	–19
0.4	19	29	–19	–25
0.5	23	35.5	–23.5	–31
0.6	27	41.5	–28	–37
0.7	30.5	48	–31.5	–42
0.8	34	54	–35	–47
0.9	36.5	59	–38	–53
1.0	38.5	65	–41	–58
1.1	40	70	–44	–62
1.2	42	75	–46	–66
1.3	43	79	–48	–71
1.4	44	82	–50	–74
1.5	44	84.5	–51	–77
1.6	45	87	–52	–81
1.7	45	89	–52	–84
1.8	45	90	–52.5	–86
1.9	45	90	–53	–89
2.0	45	91	–53	–91
2.1	46	91	–53.5	–92
2.2	46	91	–54	–93
2.3	46	91	–54	–94
2.4	46	91.5	–54	–95
2.5	46	92	–54.5	–96.5
2.6	46	92	–55	–98
2.7	46	92	–55	–99

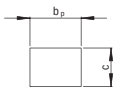
Not recommend for new design

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP64-6.1x17-0.50	PTSP0064KA-A	TTP-64DV	0.47g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	17.0	17.2
E	—	6.10	—
A_2	—	—	—
A_1	0.00	0.05	0.10
A	—	—	1.20
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	7.90	8.10	8.30
e	—	0.50	—
x	—	—	0.08
y	—	—	0.08
Z	—	—	0.90
L	0.4	0.5	0.6
L_1	—	1.0	—

Not recommend for new design

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!
1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials
1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

Not recommend for new design

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

© 2006. Renesas Technology Corp., All rights reserved. Printed in Japan.

Colophon .6.0