MITEL
SEMICONDUCTOR

VP16256

Programmable FIR Filter

Advance Information

Supersedes August 1997 version, DS4548 - 3.2

DS4548 - 4.0 August 1998

The VP16256 contains sixteen multiplier - accumulators, which can be multi cycled to provide from 16 to 128 stages of digital filtering. Input data and coefficients are both represented by 16-bit two's complement numbers with coefficients converted internally to 12 bits and the results being accumulated up to 32 bits.

In 16-tap mode the device samples data at the system clock rate of up to 40MHz. If a lower sample rate is acceptable then the number of stages can be increased in powers of two up to a maximum of 128. Each time the number of stages is doubled, the sample clock rate must be halved with respect to the system clock. With 128 stages the sample clock is therefore one eighth of the system clock.

In all speed modes devices can be cascaded to provide filters of any length, only limited by the possibility of accumulator overflow. The 32-bit results are passed between cascaded devices without any intermediate scaling and subsequent loss of precision.

The device can be configured as either one long filter or two separate filters with half the number of taps in each. Both networks can have independent inputs and outputs.

Both single and cascaded devices can be operated in decimate-by-two mode. The output rate is then half the input rate, but twice the number of stages are possible at a given sample rate. A single device with a 40MHz clock would then, for example, provide a 128-stage low pass filter, with a 10MHz input rate and 5MHz output rate.

Coefficients are stored internally and can be down loaded from a host system or an EPROM. The latter requires no additional support, and is used in stand alone applications. A full set of coefficients is then automatically loaded at power on, or at the request of the system. A single EPROM can be used to provide coefficients for up to 16 devices.

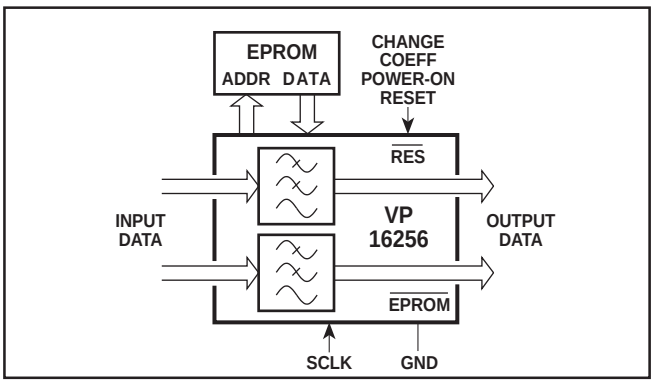


Fig. 1 A dual filter application

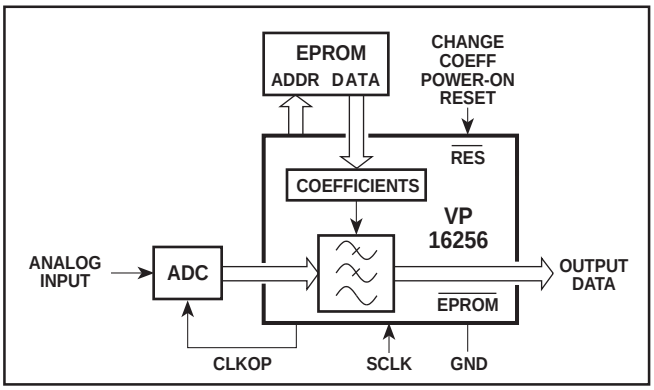
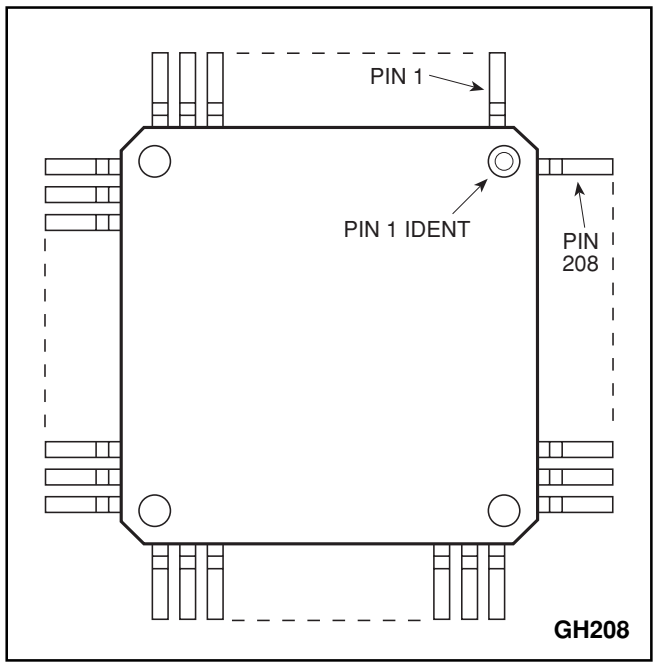


Fig. 2 Typical system application



Pin identification diagram (top view)
See Table 1 for pin descriptions and Table 2 for pinout

FEATURES

- Sixteen MACs in a Single Device
- Basic Mode is 16-Tap Filter at up to 40MHz Sample Rates
- Programmable to give up to 128 Taps with Sampling Rates Proportionally Reducing to 5MHz
- 16-bit Data and 32-bit Accumulators
- Can be configured as One Long Filter or Two Half-Length Filters
- Decimate-by-two Option will Double the Filter Length
- Coefficients supplied from a Host System or a local EPROM
- 208-Pin Plastic PowerQuad PQ2 Package

APPLICATIONS

- High Performance Commercial Digital Filters
- Matrix Multiplication
- Correlation
- High Performance Adaptive Filtering

ORDERING INFORMATION

VP16256-27/CG/GH1N 27MHz, Commercial plastic PowerQuad PQ2 package (GH208)
VP16256-40/CG/GH1N 40MHz, Commercial plastic PowerQuad PQ2 package (GH208)

Signal	Description
DA15:0	16-bit data input bus to Network A.
DB15:0	Delayed data output bus in the single filter mode. Connected to the data input bus of the next device in a cascaded chain. Input to Network B in the dual filter modes.
X31:0	Expansion input bus in the single filter mode. Connected to the previous filter output in a cascaded chain. The inputs are not used on a single device system or on the Termination device in a cascaded chain. The X bus provides the output from Network B in both dual modes.
F31:0	In single filter mode this bus holds the main device output. In dual mode it holds the output from Network A.
FEN	Filter enable. The first high present on an SCLK rising edge defines the first data sample. The control register and coefficient memory must be configured before FEN is enabled. The signal must stay active whilst valid data is being received and must be low if FRUN is high.
DFEN	Delayed filter enable. This output is connected to the Filter Enable input of the next device in a cascaded chain when moving towards the termination device and with multiple stand-alone EPROM-loaded configurations. It is used to coordinate the control logic within each device.
SWAP	Selects either the upper or lower set of coefficients for Bank Swap. A low selects the lower bank, a high the upper bank.
FRUN	In EPROM load mode, when high this signal allows continuous filter operations to occur without the need for the initial FEN edge. If the device is not a single, interface or master device then this pin must be tied low.
$\overline{\text{DCLR}}$	A low on this signal on the SCLK rising edge will clear all the internal accumulators. $\overline{\text{DCLR}}$ need only remain low for a single cycle, signal BUSY will indicate when the internal clearing is complete. After a clear the device must be re-synchronised to the data stream using FEN. It is recommended that FEN is taken low at the same time as clear. FEN may then be taken high to synchronise the data stream once BUSY has returned low.
C15:0	16-bit coefficient input bus. In the Byte mode of operation, C15:8 have alternative uses as explained in the text.
A7:0	Coefficient address bus. In the EPROM mode A7:0 are address outputs for an EPROM. In the remote host mode they are inputs from the host. A7 is not used when coefficients are loaded as 16-bit words.
CCS	This pin is similar in operation to A7:0 and provides a higher order address bit. When low the coefficients are loaded, when high the control register is loaded.
$\overline{\text{WEN}}$	In the remote mode this pin is an input which when low enables the load operation. In the EPROM mode it is an output which provides the write enable for other slave devices.
$\overline{\text{CS}}$	This pin is always an input and must also be low for the internal write operation to occur.
$\overline{\text{BYTE}}$	When this pin is tied low, coefficients are loaded as two 8-bit bytes. When the pin is high they are loaded as 16-bit words. In the EPROM mode this pin is ignored.
$\overline{\text{EPROM}}$	When this pin is tied low coefficients are loaded as bytes from an external EPROM. The device outputs an address on A7:0. When the pin is high coefficients must be loaded from a remote master. They can then be transferred individually rather than as a complete set.
SCLK	The main system clock; all operations are synchronous with this clock. The clock rate must be either 1, 2, 4, or 8 times the required data sampling rate. The factor used depends on the required filter length.
CLKOP	This output, when used to enable SCLK, can provide a data sampling clock. It has the effect of dividing the SCLK rate by 1, 2, 4 or 8 depending on the filter mode selected.
$\overline{\text{OEN}}$	Tri-state enable for the F bus. When high the outputs will be high impedance. $\overline{\text{OEN}}$ is registered onto the device and does not therefore take effect until the first SCLK rising edge
BUSY	A high on this signal indicates that the device is completing internal operations and is not yet able to accept new data. The signal is used during automatic EPROM loading, reset and accumulator clearing.
$\overline{\text{RES}}$	When this pin is low the control logic and accumulators are reset. In the EPROM mode it will initiate a load sequence when it goes high.

NOTES
1. Unused buses (e.g. X31:0 when the device is configured in single or termination mode) can be set to any value. They should however be maintained at a valid logic level to avoid an increase in power consumption.
2. To ensure correct input voltage thresholds are maintained all the V_{DD} and GND pins must be connected to adequate power and ground planes.

Table 1 Pin descriptions

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{DD}	43	F28	85	GND	127	A5	169	GND
2	F0	44	F29	86	C2	128	A6	170	X7
3	F1	45	GND	87	V_{DD}	129	GND	171	X8
4	GND	46	F30	88	C3	130	A7	172	V_{DD}
5	F2	47	F31	89	C4	131	DB0	173	X9
6	F3	48	V_{DD}	90	C5	132	V_{DD}	174	GND
7	V_{DD}	49	FEN	91	C6	133	DB1	175	X10
8	F4	50	DFEN	92	V_{DD}	134	GND	176	X11
9	F5	51	$\overline{\text{DCLR}}$	93	C7	135	DB2	177	X12
10	GND	52	GND	94	GND	136	DB3	178	V_{DD}
11	F6	53	SWAP	95	C8	137	DB4	179	X13
12	F7	54	GND	96	C9	138	V_{DD}	180	X14
13	V_{DD}	55	$\overline{\text{OEN}}$	97	C10	139	DB5	181	GND
14	F8	56	CLKOP	98	GND	140	GND	182	X15
15	GND	57	V_{DD}	99	C11	141	DB6	183	X16
16	F9	58	DA0	100	C12	142	DB7	184	X17
17	F10	59	V_{DD}	101	C13	143	V_{DD}	185	V_{DD}
18	V_{DD}	60	DA1	102	V_{DD}	144	DB8	186	X18
19	F11	61	GND	103	C14	145	V_{DD}	187	GND
20	F12	62	DA2	104	V_{DD}	146	DB9	188	X19
21	GND	63	V_{DD}	105	C15	147	DB10	189	X20
22	F13	64	DA3	106	GND	148	GND	190	X21
23	F14	65	DA4	107	GND	149	DB11	191	V_{DD}
24	F15	66	V_{DD}	108	$\overline{\text{WEN}}$	150	DB12	192	X22
25	V_{DD}	67	DA5	109	CCS	151	V_{DD}	193	GND
26	F16	68	GND	110	$\overline{\text{CS}}$	152	DB13	194	X23
27	F17	69	DA6	111	V_{DD}	153	DB14	195	X24
28	GND	70	DA7	112	$\overline{\text{RES}}$	154	GND	196	X25
29	F18	71	DA8	113	GND	155	DB15	197	X26
30	F19	72	DA9	114	SCLK	156	V_{DD}	198	GND
31	V_{DD}	73	V_{DD}	115	GND	157	GND	199	X27
32	F20	74	DA10	116	V_{DD}	158	BUSY	200	V_{DD}
33	F21	75	GND	117	$\overline{\text{BYTE}}$	159	X0	201	X28
34	F22	76	DA11	118	$\overline{\text{EPROM}}$	160	V_{DD}	202	X29
35	F23	77	DA12	119	A0	161	X1	203	X30
36	V_{DD}	78	DA13	120	V_{DD}	162	GND	204	GND
37	F24	79	DA14	121	A1	163	X2	205	X31
38	F25	80	V_{DD}	122	GND	164	V_{DD}	206	V_{DD}
39	GND	81	DA15	123	A2	165	X3	207	FRUN
40	F26	82	GND	124	A3	166	X4	208	GND
41	V_{DD}	83	C0	125	A4	167	X5		
42	F27	84	C1	126	V_{DD}	168	X6		

Table 2 VP16256 pinout (208-pin Power PQFP - GH208)

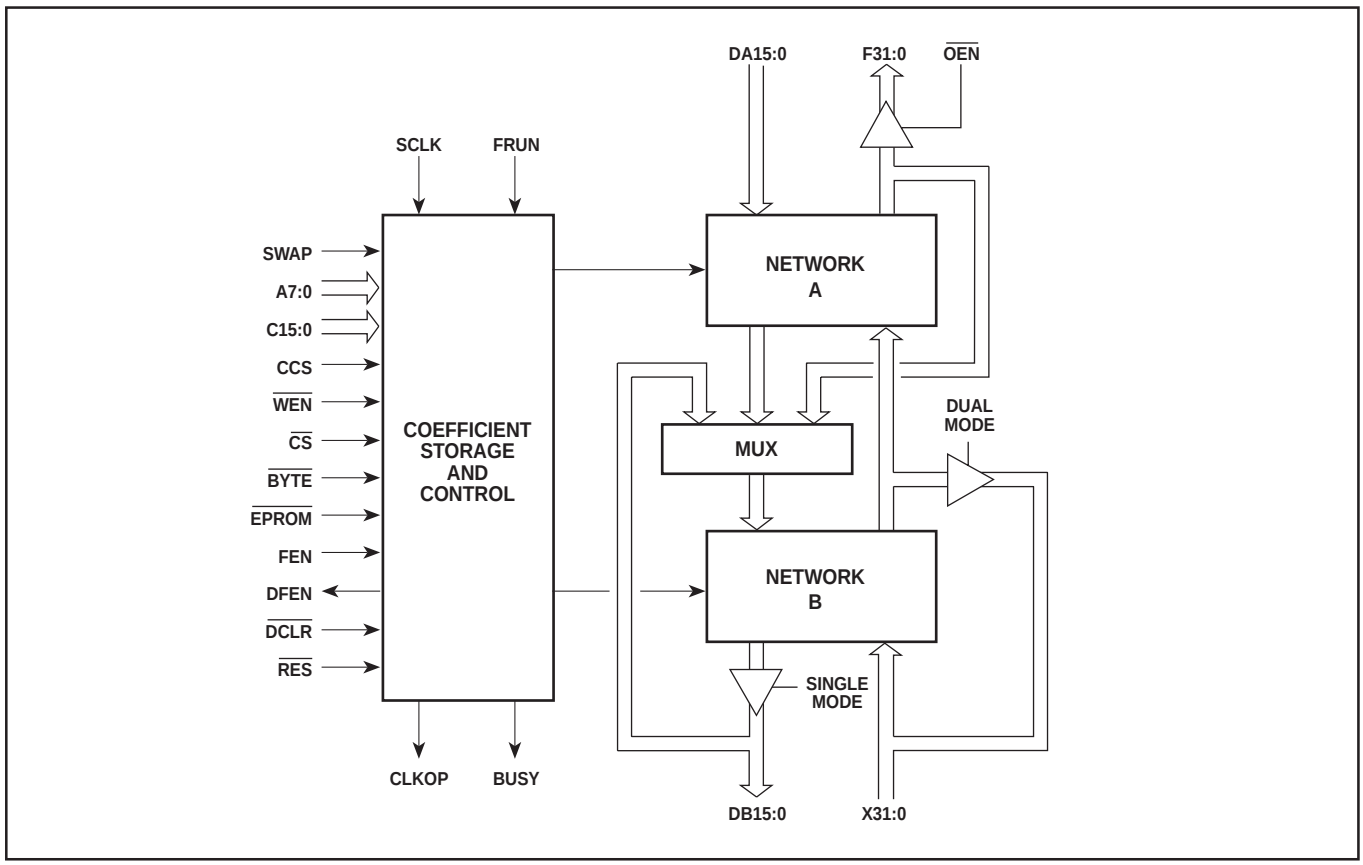


Fig. 3 Block Diagram

OPERATIONAL OVERVIEW

The VP16256 is an application specific FIR filter for use in high performance digital signal processing systems. Sampling rates can be up to 40MHz. The device provides the filter function without any software development, and the options are simply selected by loading a control register. The device can be user configured as either a single filter, or as two separate filters. The latter can provide two independent filters for the in-phase and quadrature channels after IQ splitting, or can provide two filters in cascade for greater stop band rejection.

The device operates from a system clock, with rates up to 40MHz. This clock must be 1, 2, 4, or 8 times the required sampling frequency, with the higher multiplication rates producing longer filter networks at the expense of lower sampling rates. Devices can be connected in cascade to produce longer filter lengths. This can be accomplished without the need for any additional external data delays, and all the single device options remain available.

Continuous inputs are accepted, and continuous results produced after the internal pipeline delay. Connection can be made directly to an A-D converter. The filter operation can be synchronised to a Filter Enable signal (FEN) whose positive going edge marks the first data sample. The internal multiplier accumulator array can be cleared with a dedicated input. This is necessary if erroneous results obtained during the normal data 'flush through' are not permissible in the system.

Coefficients can be loaded from a host system using a conventional peripheral interface and separate data bus. Alternatively, they can be loaded as a complete set from a byte wide EPROM. The device produces addresses for the EPROM and a BUSY output indicates that the transfer is occurring. Up to sixteen devices can have their coefficients supplied from a single EPROM. These devices need not necessarily be part of the same filter network.

Each of the filter networks shown in Fig. 3 contains eight systolic multiplier accumulator stages; an example with four stages is shown in Fig. 4. Input data flows through the delay lines and is presented for multiplication with the required coefficient. This is added to either the last result from this accumulator or the result from the previous accumulator. The filter results progress along the adders at the data sample rate. If the sample rate equals SCLK divided by four, for example, then the accumulated result is passed onto the next stage every fourth cycle. The structure described is highly efficient when used to calculate filtered results from continuous input data.

A comprehensive digital filter design program is available for PC compatible machines. This will optimise the filter coefficients for the filter type required and number of taps available at the selected sample rate within the VP16256 device. An EPROM file can be automatically generated in Motorola S-record format.

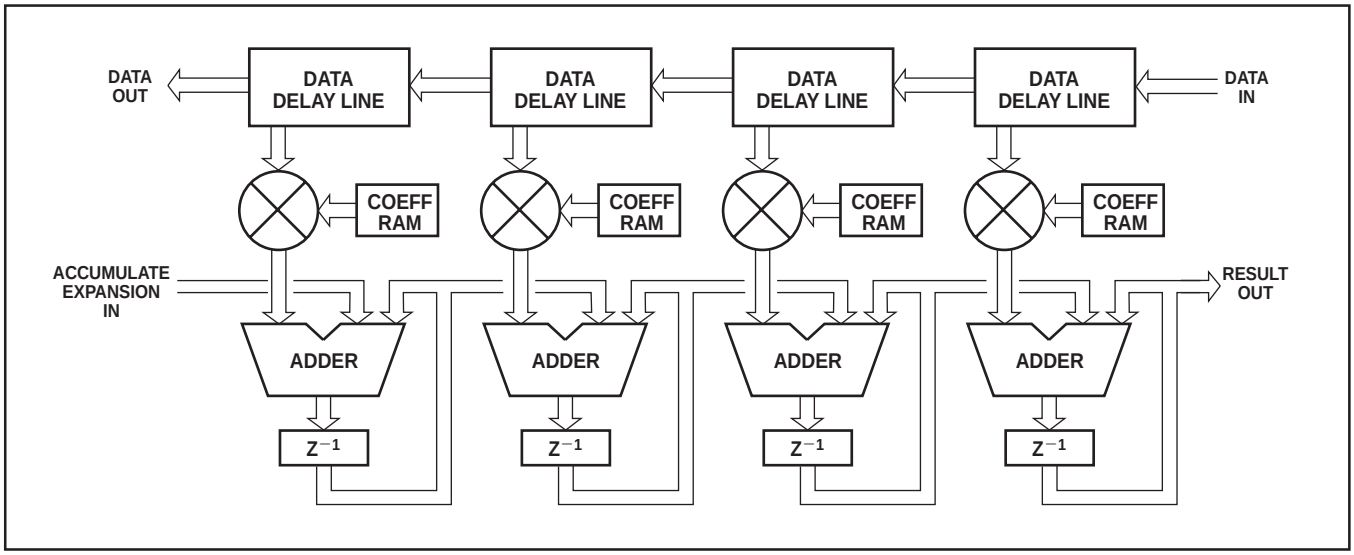


Fig. 4 Filter network diagram

SINGLE FILTER OPTIONS

When operating as a single filter the device accepts data on the 16-bit DA bus at the selected sample rate, see Figs. 5 and 6. Results are presented on the 32-bit F bus, which may be tristated using the $\overline{OEN}$ input. Signal $\overline{OEN}$ is registered onto the device and does not therefore take effect until the first SCLK rising edge. Devices may be cascaded this allows filters with more taps than available from a single device. To accomplish this two further buses are utilised. The DB bus presents the input data to the next device in cascade after the appropriate delay, while, partial results are accepted on the X bus.

Single filter mode is selected by setting control register bit 15 to a one. The required filter length is then selected using control register bits 14 and 13 as summarised in Table 3. The options define the number of times each multiplier accumulator is used per sample clock period. This can be once, twice, four times, or eight times.

In addition a normal/decimate bit (CR12) allows the filter length to be doubled at any sample rate. This is possible when the filter coefficients are selected to produce a low pass filter, since the filtered output would then not contain the higher frequency components present in the input. The Nyquist criterion, specifying that the sampling rate must be at least double the highest frequency component, can still then be satisfied even though the sampling rate has been halved.

CR 14	CR 13	CR 12	Input Rate	Output Rate	Filter Length	Setup Latency
0	0	0	SCLK	SCLK	16 Taps	16
0	0	1	SCLK	SCLK/2	32 Taps	17
0	1	0	SCLK/2	SCLK/2	32 Taps	16
0	1	1	SCLK/2	SCLK/4	64 Taps	18
1	0	0	SCLK/4	SCLK/4	64 Taps	20
1	0	1	SCLK/4	SCLK/8	128 Taps	24
1	1	0	SCLK/8	SCLK/8	128 Taps	24

Table 3 Single Filter options

The system clock latency for a single device is shown in Table 3. This is defined as the delay from a particular data sample being available on the input pins to the first result including that input appearing on the output pins. It does not include the delay needed to gather N samples, for an N tap filter, before a mathematically correct result is obtained.

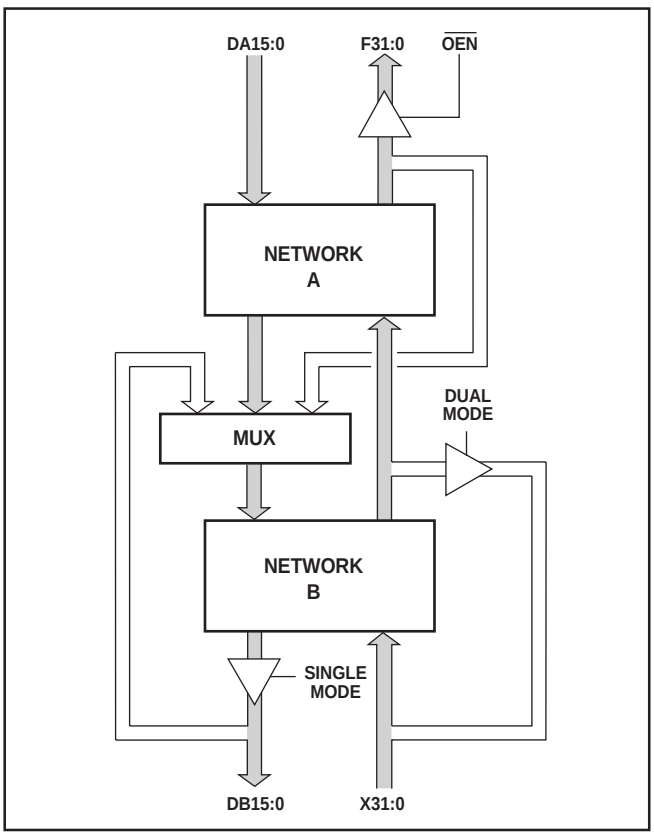
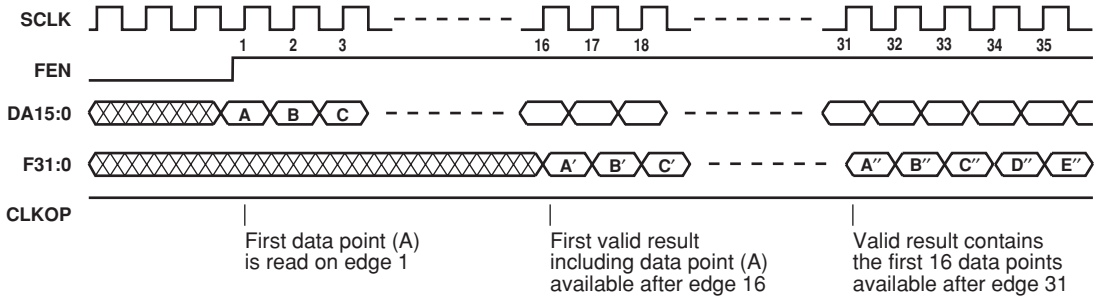
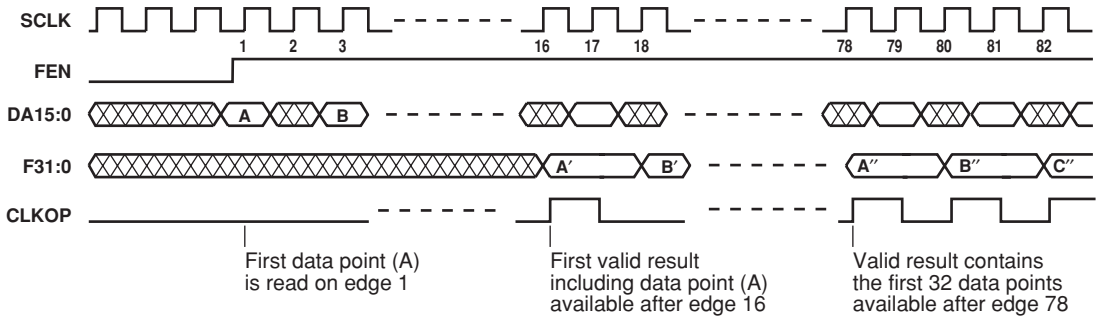


Fig. 5 Single Filter bus utilisation

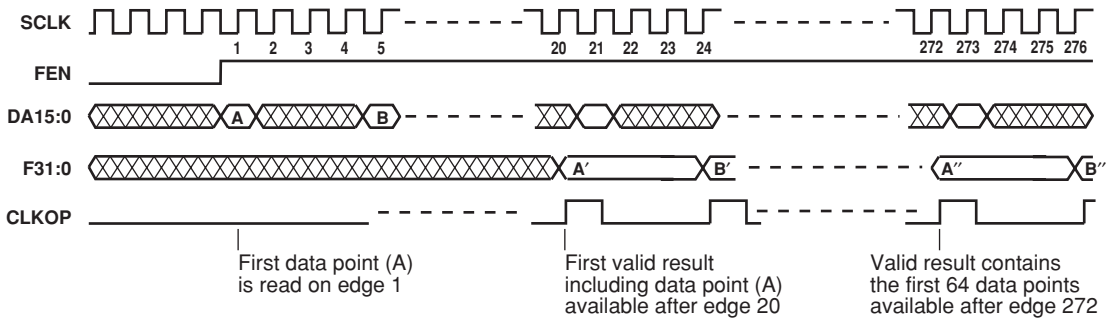
SPEED MODE 0 (Data input and output at f_{SCLK}) CR14:13 = 00, CR12 = 0. CLKOP held high.



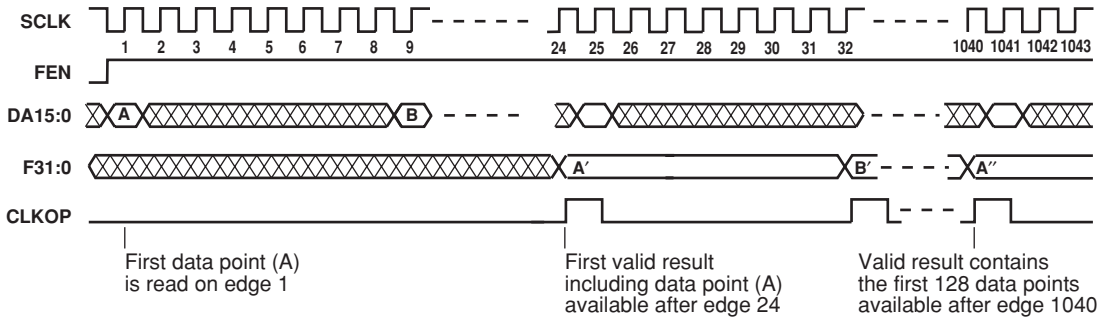
SPEED MODE 1 (Data input and output at half f_{SCLK}) CR14:13 = 01, CR12 = 0



SPEED MODE 2 (Data input and output at a quarter f_{SCLK}) CR14:13 = 10, CR12 = 0



SPEED MODE 3 (Data input and output at an eighth f_{SCLK}) CR14:13 = 11, CR12 = 0



SPEED MODE 1 Decimating (Data input at half f_{SCLK} and output at a quarter f_{SCLK}) CR14:13 = 01, CR12 = 1.

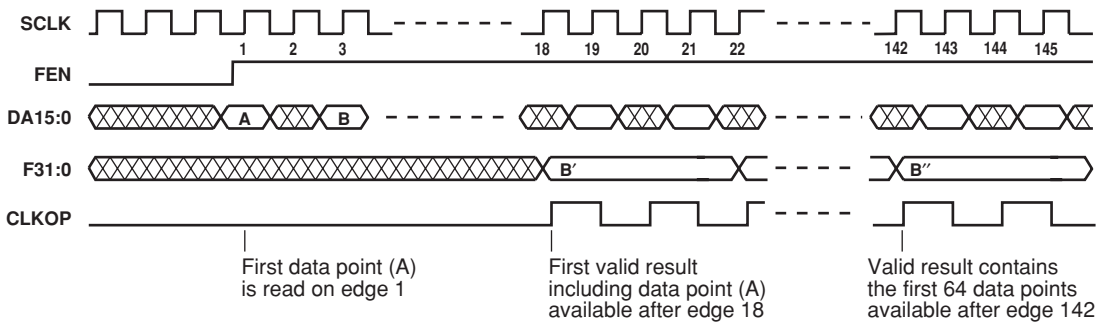


Fig. 6 Single Filter timing diagrams

DUAL INDEPENDENT FILTER OPTIONS

When operating as two independent filters the device accepts 16 bit data on both the DA and DB buses at the selected sample rate, see Fig. 7. Results are available from both the F and X buses. The F bus may be tristated using the $\overline{OEN}$ input. Signal $\overline{OEN}$ is registered onto the device and does not therefore take effect until the first SCLK rising edge

Each filter must be configured in the same manner, and multiple device expansion is not possible due to the pin re-organization. The latter requirement can, of course, still be satisfied by several devices configured as single filters.

Dual independent filter mode is selected by setting control register bits 15 and 4 to a zero. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. As in single filter mode normal or decimate-by-two operation can be selected using control register bit 12.

CR 14 13 12	Input Rate	Output Rate	Filter Length	Setup Latency	
				Ind	Cas
0 0 0	SCLK	SCLK	8 Taps	16	27
0 0 1	SCLK	SCLK/2	16 Taps	17	-
0 1 0	SCLK/2	SCLK/2	16 Taps	16	28
0 1 1	SCLK/2	SCLK/4	32 Taps	18	-
1 0 0	SCLK/4	SCLK/4	32 Taps	20	36
1 0 1	SCLK/4	SCLK/8	64 Taps	24	-
1 1 0	SCLK/8	SCLK/8	64 Taps	24	40

Table 4. Dual Filter options

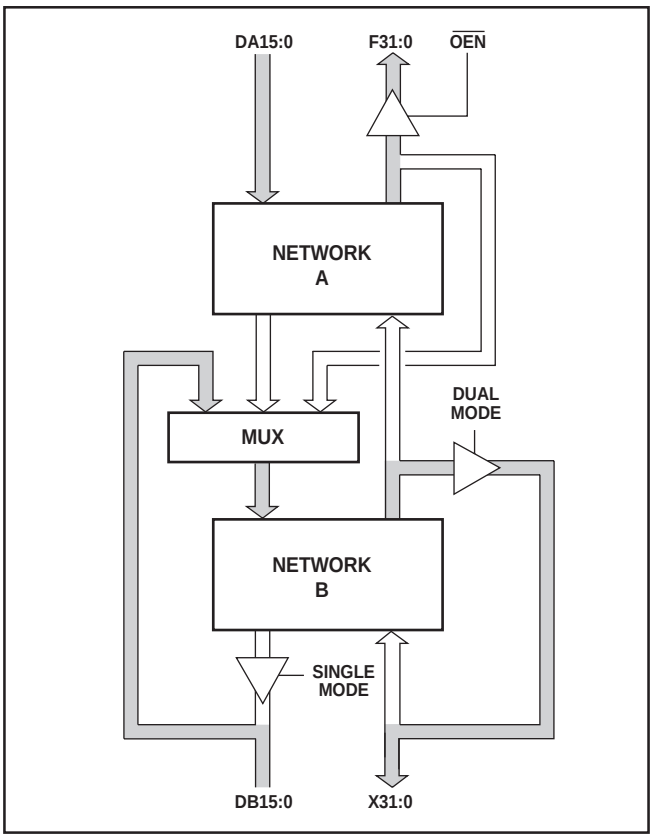


Fig. 7 Dual independent filter bus utilisation

DUAL CASCADED FILTER OPTIONS

When operating as two cascaded filters the device accepts 16 bit data on the DA bus at the selected sample rate. Results are presented on the 32-bit X bus, see Fig. 8. Each filter must be configured in the same manner. Multiple device expansion is not possible in this mode.

Dual cascaded filter mode is selected by setting control register bit 15 to a zero and bit 4 to a one. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. The decimate-by-two option is not available in this mode.

The data for the second filter network is extracted as the middle 16 bits from the first networks accumulated result. For successful operation the first filter network must have unity gain. See the section on filter accuracy for more details.

The cascade option is used to increase the stop band rejection in a practical filter application. Theoretically, increasing the number of taps in an FIR filter will increase the stop band rejection, but this assumes floating point calculations with no accuracy limitations. In practice, with fixed point arithmetic, better performance is achieved with two smaller filters in series.

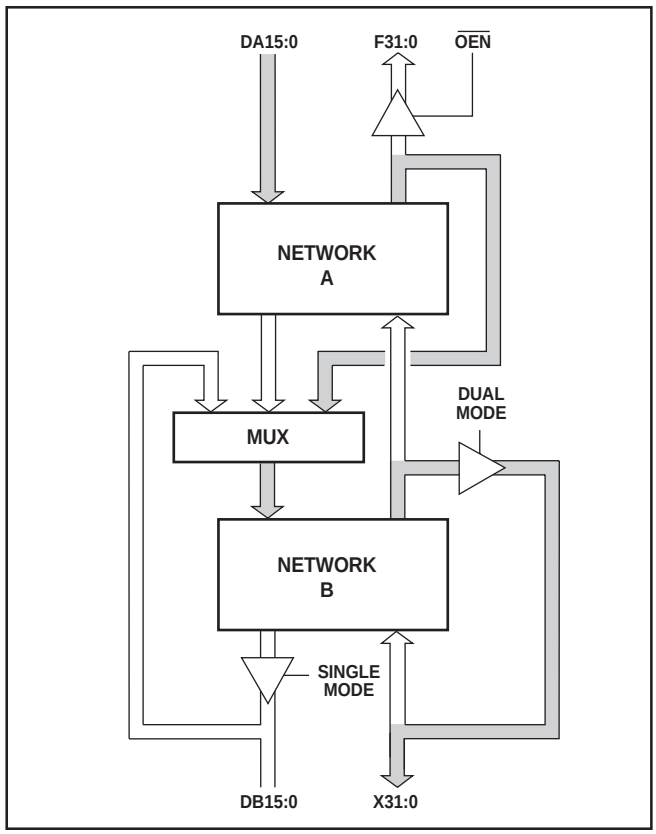


Fig. 8 Dual cascaded filter bus utilisation

FILTER ACCURACY

Input data and coefficients are both represented by 16-bit two's complement numbers. The coefficients are converted to twelve bits by rounding towards zero. This is achieved as follows. If the coefficient is positive then the least significant 4 bits are discarded. If the coefficient is negative then the logical 'OR' of the least significant 4 bits are added to the remainder of the word. Twelve bit coefficients can be used directly provided the least significant four bits are set to zero.

The FIR filter results are calculated using a multiplier accumulator structure as shown in Fig. 9. The truncation and word growth allowed for in the data path are explained in Fig. 10. The 16-bit data and 12-bit coefficient inputs (each with one sign bit before the binary point), are presented to the multiplier. This produces a 28-bit result with two bits before the binary point. Producing the full 28-bit result ensures that if both the data and coefficients are set to logic 1 a valid result is generated. Prior to entering the accumulator the least significant 4 bits of the multiplier result are truncated and the resulting 24 bits sign extended to 32 bits. The final accumulator result is 32 bits with 10 bits before the binary point. Thus 9 bits of word growth are allowed within the accumulator. All accumulator bits are made available on the output pins.

In cascade mode the middle 16 bits from the network A accumulator are fed round to the network B data inputs, see Fig. 10.

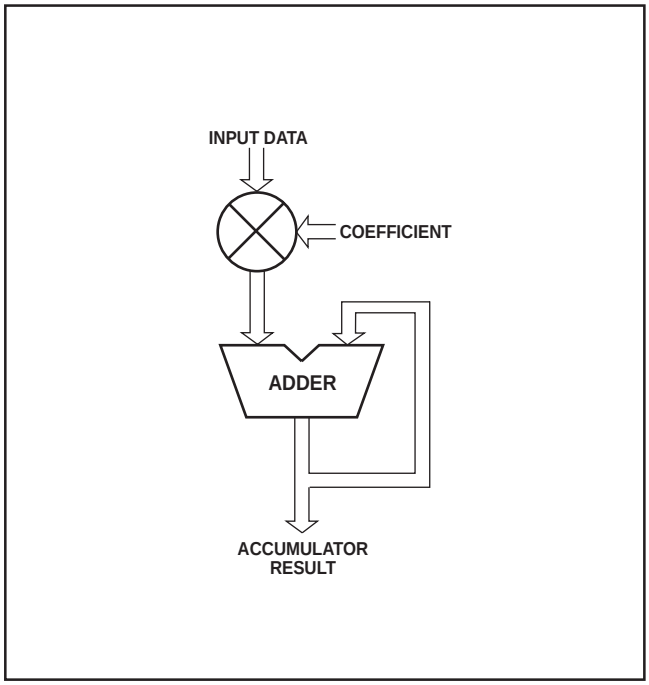


Fig. 9 Multiplier Accumulator

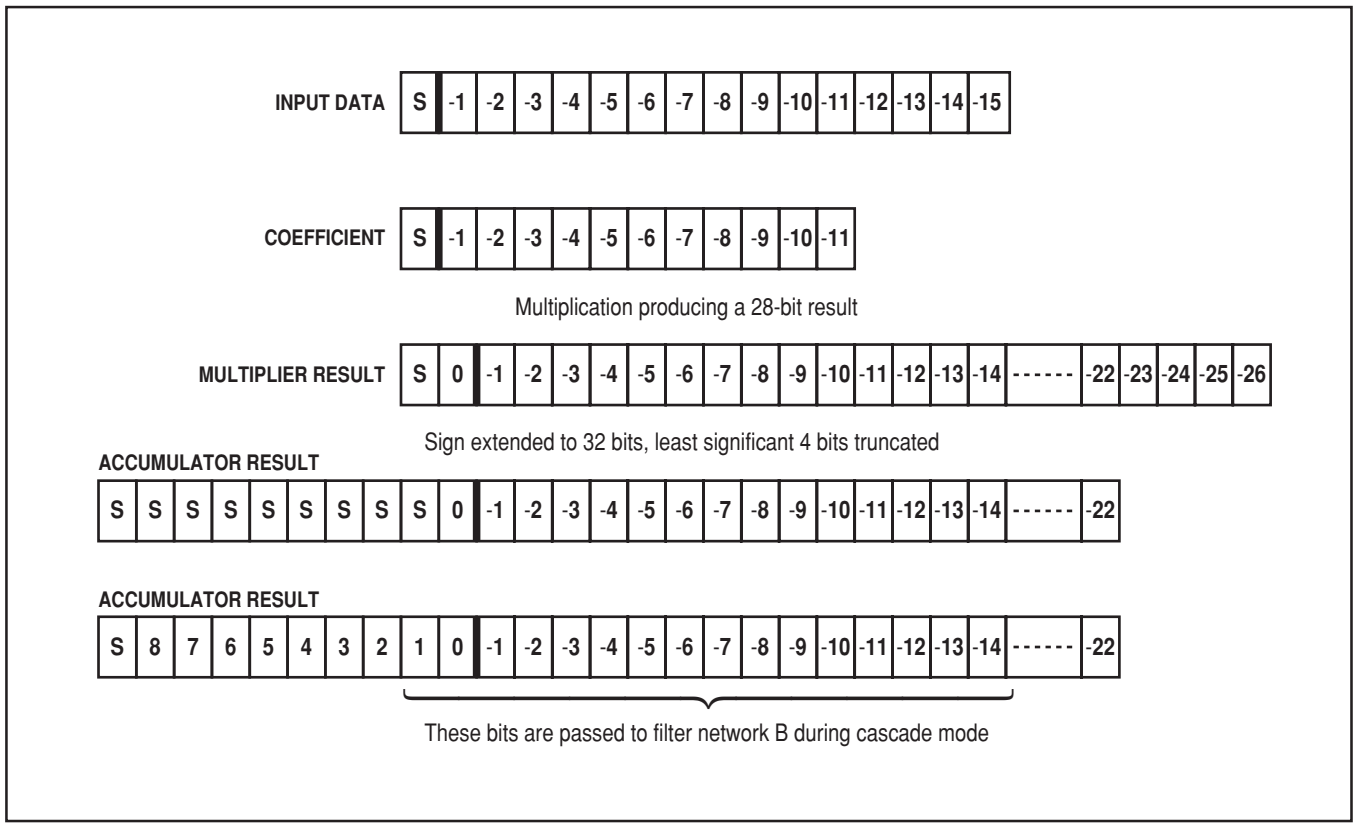


Fig. 10 Filter accuracy

CASCADING DEVICES

When the filter requirements are beyond the capabilities of a single device, it is possible to connect several devices in cascade increasing the number of taps available at the required sample rate. Within each device all filter length, decimate, and bank swap options are still possible, but each device in the chain must be similarly programmed and configured as a single filter.

The number of devices which can be cascaded is only limited by the possibility of overflow in the 32-bit intermediate accumulations. If more than sixteen devices are cascaded in auto EPROM load mode, then an additional EPROM will be needed.

In modes where the data sample rate does not equal the clock rate. Then the cascade arrangement shown in Fig. 11 is used. Delayed data is passed from device to device in one direction, while intermediate results flow in the opposite direction. The interface device both accepts the input data and produces the final result. It is not necessary for each device to know its exact position in the chain, but the device which receives the input data and produces the final result must be identified, as must the device which terminates the chain. The former is known as the Interface device and the latter as the Termination device, all others are Intermediate devices. Control Register bits CR11:10 are used to define these positions as shown in Table 6.

The control logic in each of the devices must be synchronised with respect to the Interface device. This is achieved by connecting the Delayed Filter Enable output (DFEN) to the Filter Enable input (FEN) of the next device in the chain. The Interface device, itself, needs a FEN signal produced by the system, unless in EPROM mode, where FRUN may be pulled high. Even when the latter is true, the FEN connection must be made between the remaining devices in the chain. By effectively extending the filter length, the cascade latency is therefore the same as for the single device in the same mode. Once the pipeline is initially flushed the latency is as given in Table 3.

When devices are cascaded such that the data sample rate equals the clock rate, (Control register bits 14:13 = 00), then a different cascade configuration must be used. This is shown in Fig. 12. The number of devices that can be cascaded is, again, only limited by the 32-bit accumulators.

In this mode the delayed data is passed from device to device in the same direction as the intermediate results. The device which accepts the input data is now at the opposite end of the chain to the device which produces the final result. The control logic in each of the devices must be synchronised this is achieved by connecting all the device FEN inputs to the global FEN. The cascade latency for the complete filter is built up from the 12 delays from the termination device, 8 delays from the interface device and additional intermediate devices each adding 4 delays.

AVAILABLE OPTIONS

No more than 128 coefficients can be stored internally. This limits the filter length / decimate / bank swap options to those which do not require more than that number of coefficients. Thus when a filter with 128 taps is to be implemented in a single device, it is not possible to decimate or bank swap. When a filter with 64 taps is implemented, decimate or bank swap are possible, but not both. With all other filter lengths, all decimate and bank swap configurations are possible.

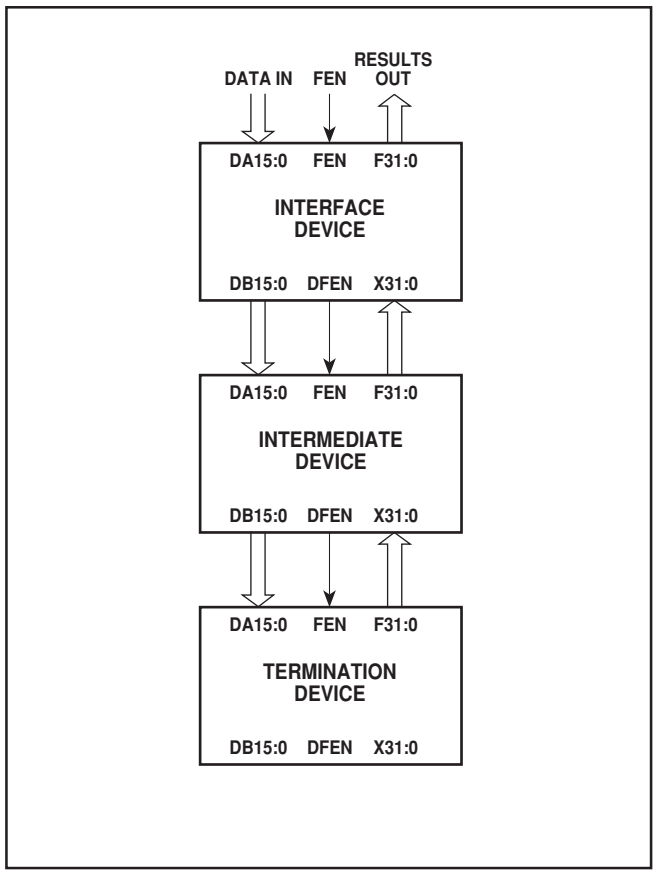


Fig. 11 Three-device cascaded system

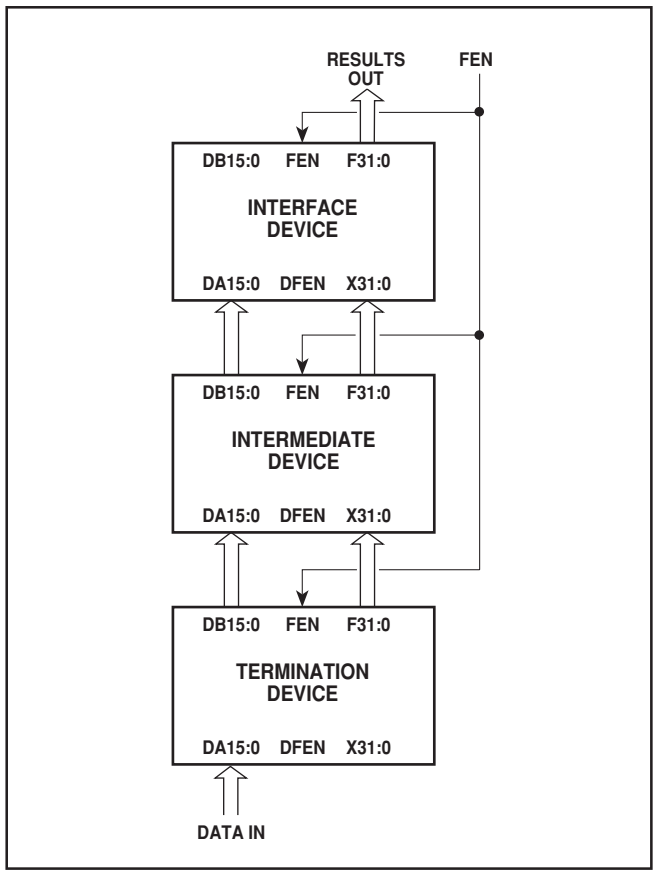


Fig. 12 Full speed cascaded system

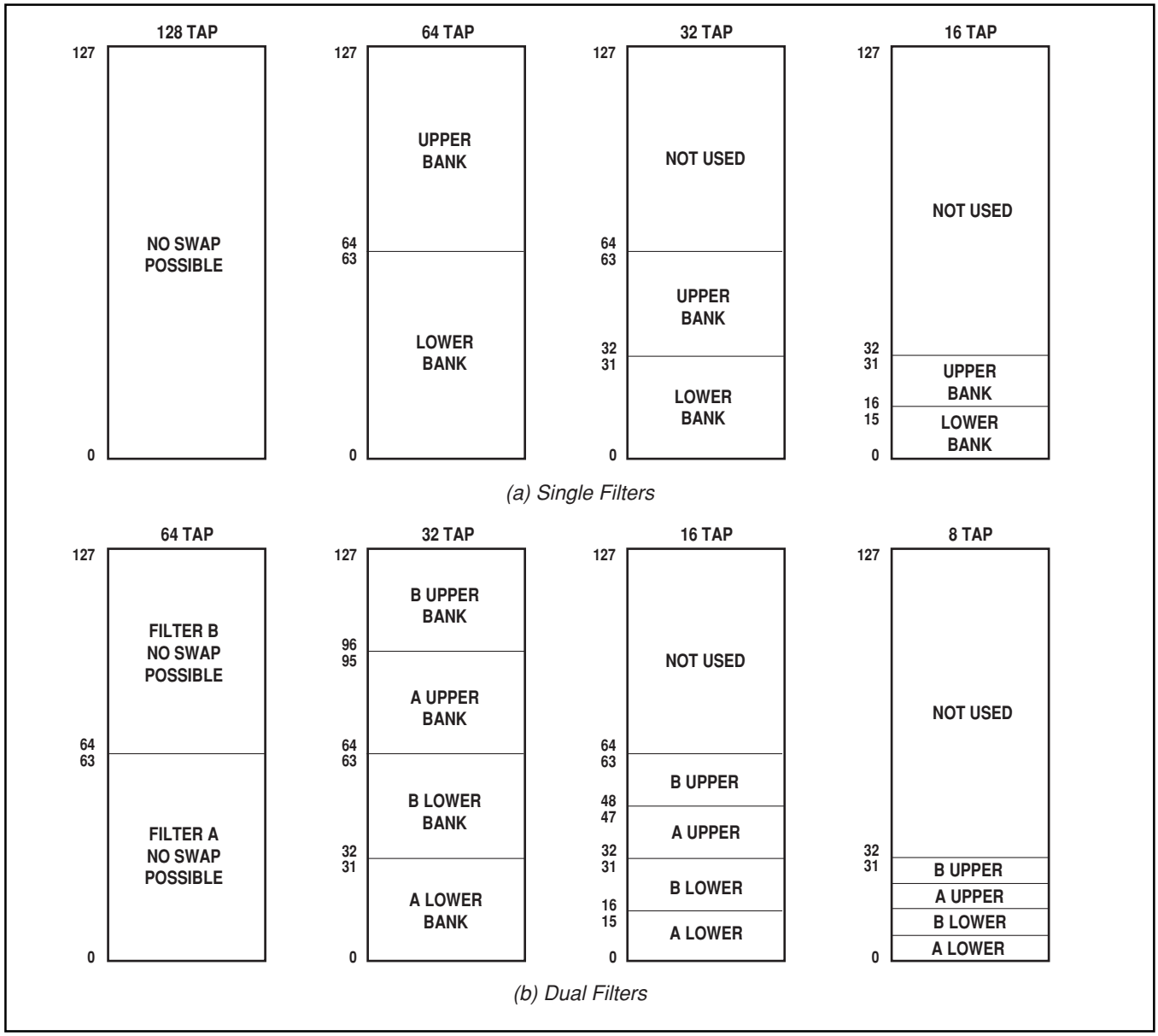


Fig. 13 Coefficient memory map

FILTER CONTROL

Two control modes are available selected by input signal FRUN. In EPROM load mode, when FRUN is tied high the device will commence operation once the coefficients have been loaded. The CLKOP signal indicates when new input data is required and that new results are available, see Fig. 6. In both EPROM and remote master load modes, when FRUN is tied low filter operation will not commence until a high has been detected on signal FEN. This mode allows synchronisation to an existing data stream. FEN should be taken high when the first valid data sample is available so that both are read into the device on the next SCLK rising edge.Proper device operation requires FEN to be low during control register and coefficient loading both in EPROM mode and Remote Master mode. After loading coefficients, filter operation is determined by FRUN and FEN as described above.

During device reset $\overline{\text{RES}}$ must be held low for a minimum of 16 SCLK cycles. After a reset the control register returns to its default state of $8C80_{HEX}$. This places the device into the following mode :

- Single filter
- Sample rate equal to the clock rate
- Non-decimating
- A single device (Not in a cascade chain)
- Bank swap selected by bit in the control register

COEFFICIENT BANK SWAP

A Bank Swap feature is provided which allows all coefficients to be simultaneously replaced with a different set. A bit in the Control Register (CR7) allows the swap to be controlled by either input signal SWAP or Control Register bit (CR6). The latter is useful if the device is controlled by a microprocessor, when driving a separate pin would entail additional address decoding logic and an external latch.

If SWAP or bit CR6 is low, the coefficients used will be those loaded into the lower banks illustrated in Fig. 13. When the SWAP or CR6 is high, the upper banks are used.

The actual swap will occur when the next sampling clock active going transition occurs. This can be up to seven system clocks later than the swap transition, and is filter length dependent. The first valid filtered output will then occur after the pipeline latencies given in Tables 3 and 4.

By setting a bit in the Control Register it is possible to bank

swap on every data sampling clock. This function does not depend on the status of SWAP or bit, and the lower bank will be initially selected after FEN goes active. The option can be used to implement filters with complex coefficients.

LOADING COEFFICIENTS

When the device is to operate in a stand alone application then the coefficients can be down loaded as a complete set from a previously programmed EPROM. Alternatively if the system contains a microprocessor they can be individually transferred from a remote master under software control. In any mode the system clock must be present and stable during the transfer, and the addressing scheme is such that the least significant address specifies the coefficient applied to the first multiplier seen by incoming data.

The addresses used during the load operation are those illustrated in Fig. 13. The Control Register is loaded when CCS is high. In byte mode address A0 is used to select the portion of control register loaded, otherwise the address bits are redundant. When an $\overline{\text{EPROM}}$ is used to provide coefficients, this redundancy causes the number of locations needed for any device to be double that for the coefficients alone.

AUTO EPROM LOAD

When EPROM is tied low, the VP16256 assumes the role of a master device in the system and controls the loading of coefficients from an external EPROM, see Fig.15. A load sequence commences when the $\overline{\text{RES}}$ input goes high, and will continue until every coefficient has been loaded. BUSY goes high to indicate that a load sequence is occurring and the filter output is invalid. The device will not commence a filter operation until the FEN edge is received after BUSY has gone low. This requirement can be avoided if FRUN is tied high.

The address bus pins become outputs on the Master device, and produce a new address every four system clock periods. This four clock interval, minus output delays and the data set up time, defines the available EPROM access time.

The coefficients are always loaded as bytes. The state of the $\overline{\text{BYTE}}$ pin on the master device is ignored. This arrangement also allows the eight most significant coefficient bus pins (C15:8) to be used for other purposes as described later. Since the 16-bit coefficients are loaded in two bytes the A0 pin specifies the required byte. The maximum number of stored coefficients is 128, eight address outputs are therefore provided for the EPROM. These eight outputs from the Master must also drive the address inputs on the slave devices.

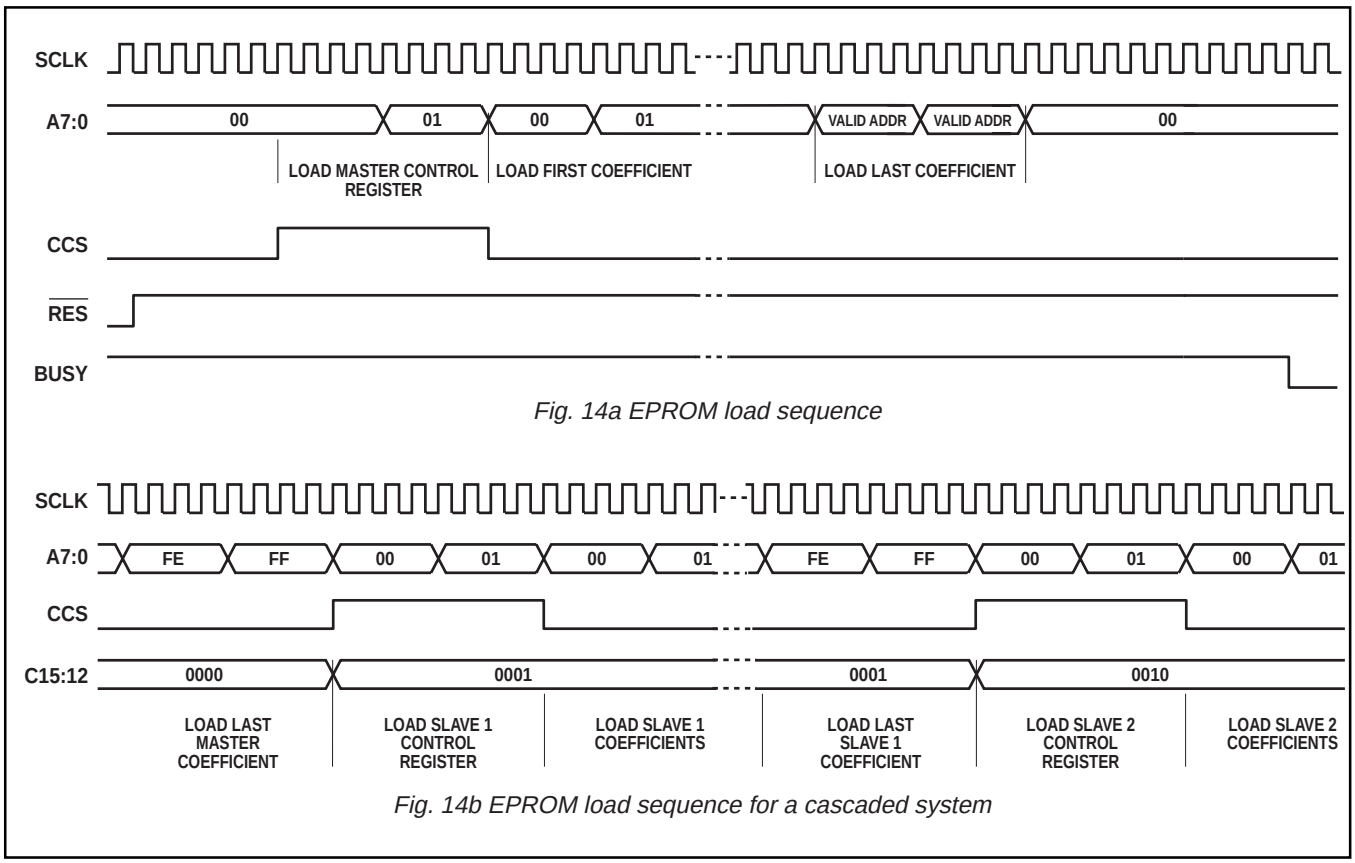


Fig. 14a EPROM load sequence

Fig. 14b EPROM load sequence for a cascaded system

Fig. 14 EPROM load sequence timing diagrams

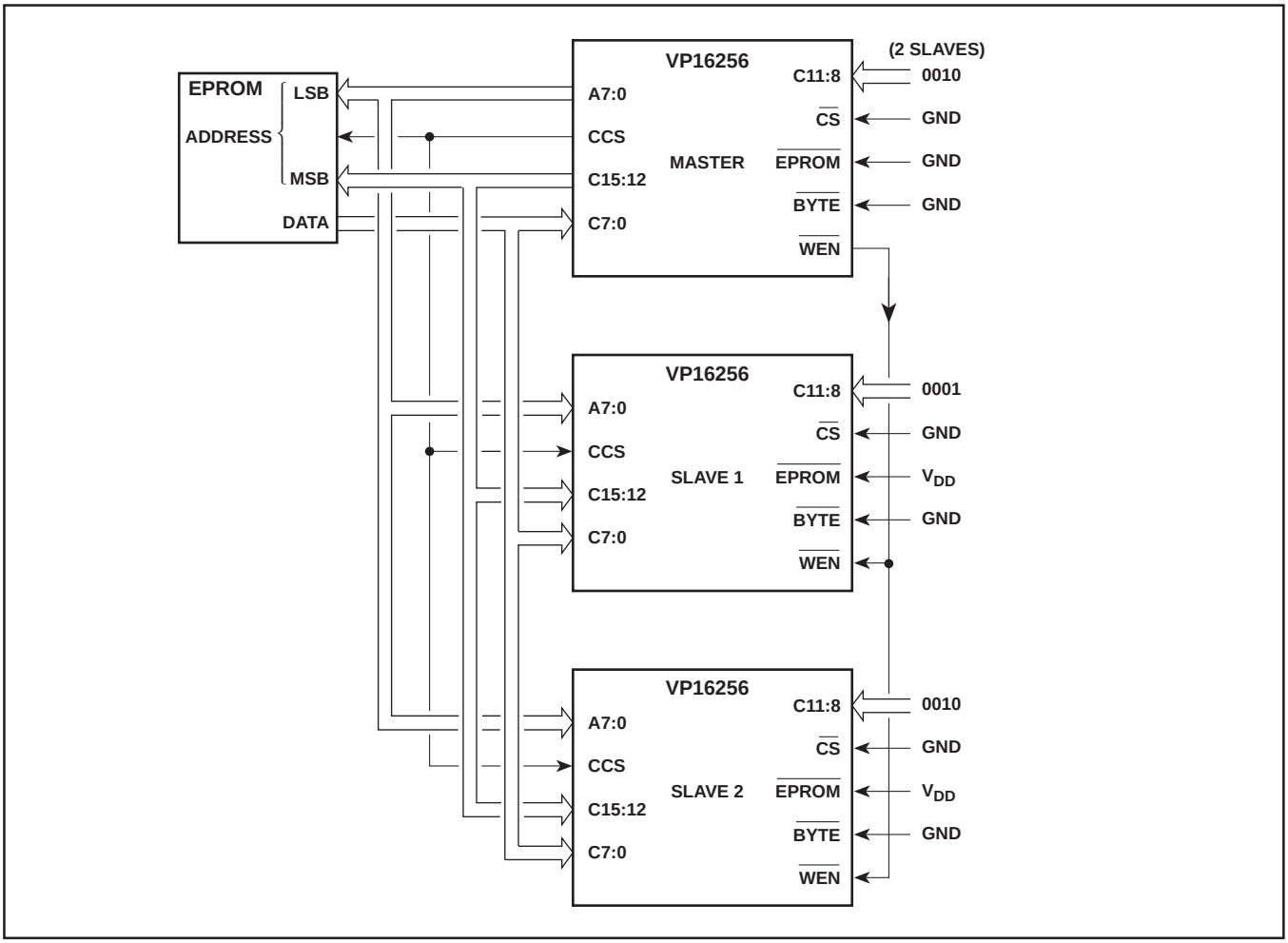


Fig. 15 Three device auto EPROM load

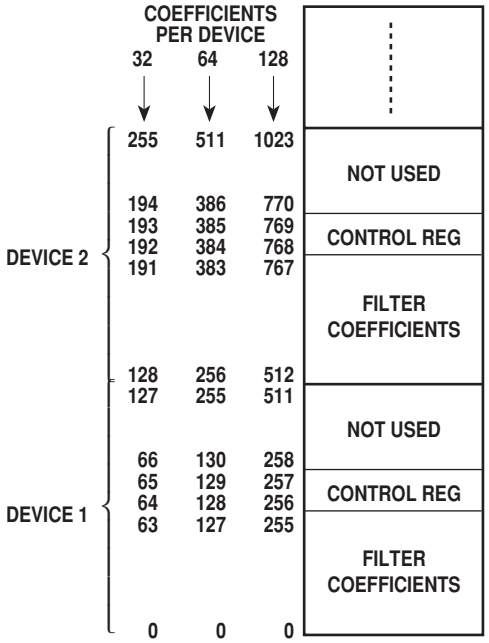
When the filter length is less than the maximum, the VP16256 will only transfer the correct number of coefficients, and one or more significant address bits will remain low. Sufficient coefficients are always loaded to allow for a possible Bank Swap to occur, and the EPROM allocation must allow for this even if the feature is not to be used. Table 5 shows the number of coefficients loaded for each of the modes.

If several devices are cascaded, only one device assumes the role of the Master by having its $\overline{\text{EPROM}}$ pin grounded. It produces a $\overline{\text{WEN}}$ signal for the other devices, plus four higher order address outputs on C15:12, see Fig. 14. The extra address bits on C15:12 define separate areas of EPROM, containing coefficients for up to fifteen additional devices. The least significant block of memory must always be allocated to the Master device. The additional devices need not in practice be all part of the same cascaded chain, but can consist of several independent filters. They must, however, all have their $\overline{\text{BYTE}}$ pins tied low. FRUN can still be used to start these independent filters after all the devices have been loaded. In this case, however, each slave FEN pin should be driven by DFEN from the master device.

When one EPROM is supplying information for several devices, some means of selectively enabling each additional device must be provided. This is achieved by using the C11:8 pins on the slave devices as binary coded inputs to define one to fifteen extra devices. These coded inputs always correspond to the block address used for the segment of EPROM allocated to that device. Code 'all zeros' must not be used since the Master device has implied use of the bottom segment. This is necessary since the C11:8 pins are alternatively used on the Master device to define the number of devices supported by the EPROM.

In addition to providing the most significant addresses to the EPROM, the C15:12 address outputs from the master device must also drive the C15:12 inputs on the slave devices. These C15:12 inputs are internally compared to the C11:8 inputs to decide if that device is currently to be loaded. This approach avoids the need for external decoders and makes the $\overline{\text{CS}}$ input redundant. This input, however, must be tied low on every device in an EPROM supported system.

The Control Coefficient pin (CCS) is used to define when the control register is to be loaded. It becomes an output on the Master device which provides an EPROM address bit next in significance above A7:0, and also drives the CCS inputs on the slave devices. This output is high for the first two EPROM transfers in order to access the control information, and then remains low whilst the coefficients are loaded. This control information is thus not stored adjacent to the coefficients within the EPROM, and in fact the EPROM must provide twice the storage necessary to contain the coefficients alone. All but two of the bytes in the additional half are redundant. See Fig.16 for the EPROM memory map.



Control Register 14 13 12	Number of Coefficients Loaded
0 0 0	32
0 0 1	64
0 1 0	64
0 1 1	128
1 0 0	128
1 0 1	128
1 1 0	128
1 1 1	Invalid Mode

Table 5. Number of coefficients loaded

NOTE:
The EPROM memory map assumes that, for the 32 and 64 coefficient per device options, the unused address pins are unconnected. If all address pins are connected as shown in Fig. 15 then the 128 coefficients per device memory map column should be used. Only those coefficients required will be read, hence the upper portions of the coefficient address space will be ignored.

Fig. 16 EPROM Memory Map

USING A REMOTE MASTER

When a remote master is used to load coefficients, $\overline{\text{EPROM}}$ must be tied high and a conventional peripheral interface is then provided. It is not possible, however, to read coefficients already stored. The master supplies an address and data bus, and writes to the VP16256 occur under the control of synchronous $\overline{\text{CS}}$ and $\overline{\text{WEN}}$ inputs. The Coefficient Control Register pin (CCS) must be driven by a master address line higher in significance than A7:0. Both the $\overline{\text{WEN}}$ and $\overline{\text{CS}}$ signals must be low for the load operation to occur. When loading the control register the $\overline{\text{CS}}$ signal must be held low for a further 2 cycles, see Fig. 19. Since the internal write operation is actually performed with the system clock, it is necessary for the clock to be present during the transfer.

The $\overline{\text{BYTE}}$ input defines whether coefficients are loaded as a single 16 bit word or two 8-bit bytes. The latter saves on connections to the remote master. Address bits A7:0 are used in byte mode. 16-bit word mode uses bits A6:0, A7 being redundant. ~~When~~ writing in byte mode the least significant byte (A0 = 0) must be written first followed by the most significant byte (A0 = 1).

In byte mode the internal comparison between C15:12 and C11:8 is made, regardless of the state of $\overline{\text{EPROM}}$. For this reason pins C15:8 should all be tied low when a remote master is used with byte transfers. This ensures that the internal comparison gives equality and allows the load operation to occur.

The address and coefficient buses plus the $\overline{\text{WEN}}$ and $\overline{\text{CS}}$ signals must all meet the specified set up and hold times with respect to the system clock, see Fig 19 and Switching Characteristics. This synchronous interface is optimum for the majority of high end applications, when individual coefficients must be updated at sample clock rates. However, if the coefficients are to be loaded under software control from a general purpose microprocessor, the processor's $\overline{\text{WRITE STROBE}}$ will probably be asynchronous with the SCLK clock used by the VP16256. In this case external synchronising logic is needed, as shown in Fig.17.

Fig. 18 shows the recommended loading sequence and filter operation initiation. The simplest technique is to reset the device prior to loading a set of coefficients. Coefficients may be loaded once BUSY returns low or 22 cycles after $\overline{\text{RES}}$ is taken high.

When loading a device from a remote master the control register must be loaded first followed by the filter coefficients. Fig. 18 shows the required loading sequence, two examples are given one for byte mode the other for word mode. A gap of at least one cycle must be left after loading the control register before loading the first coefficient.

Filter operations are started by presenting the first data word at the same time as raising signal FEN; FRUN should always be low.

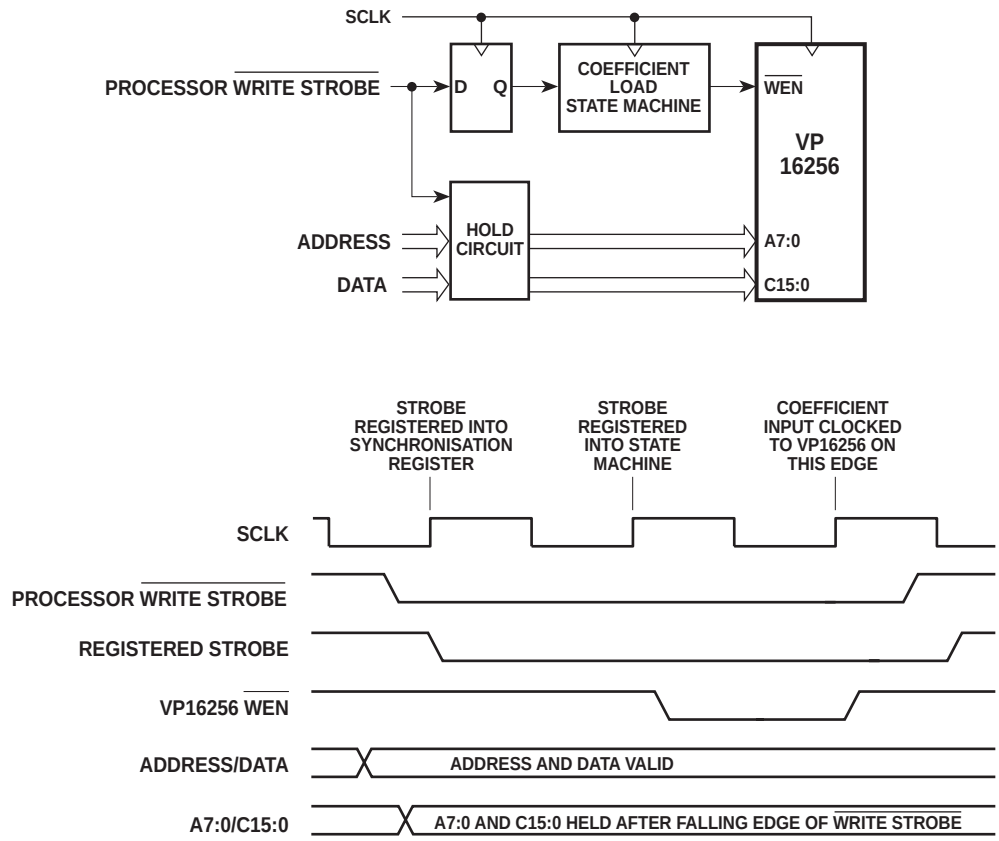


Fig. 17 Remote Master synchronisation

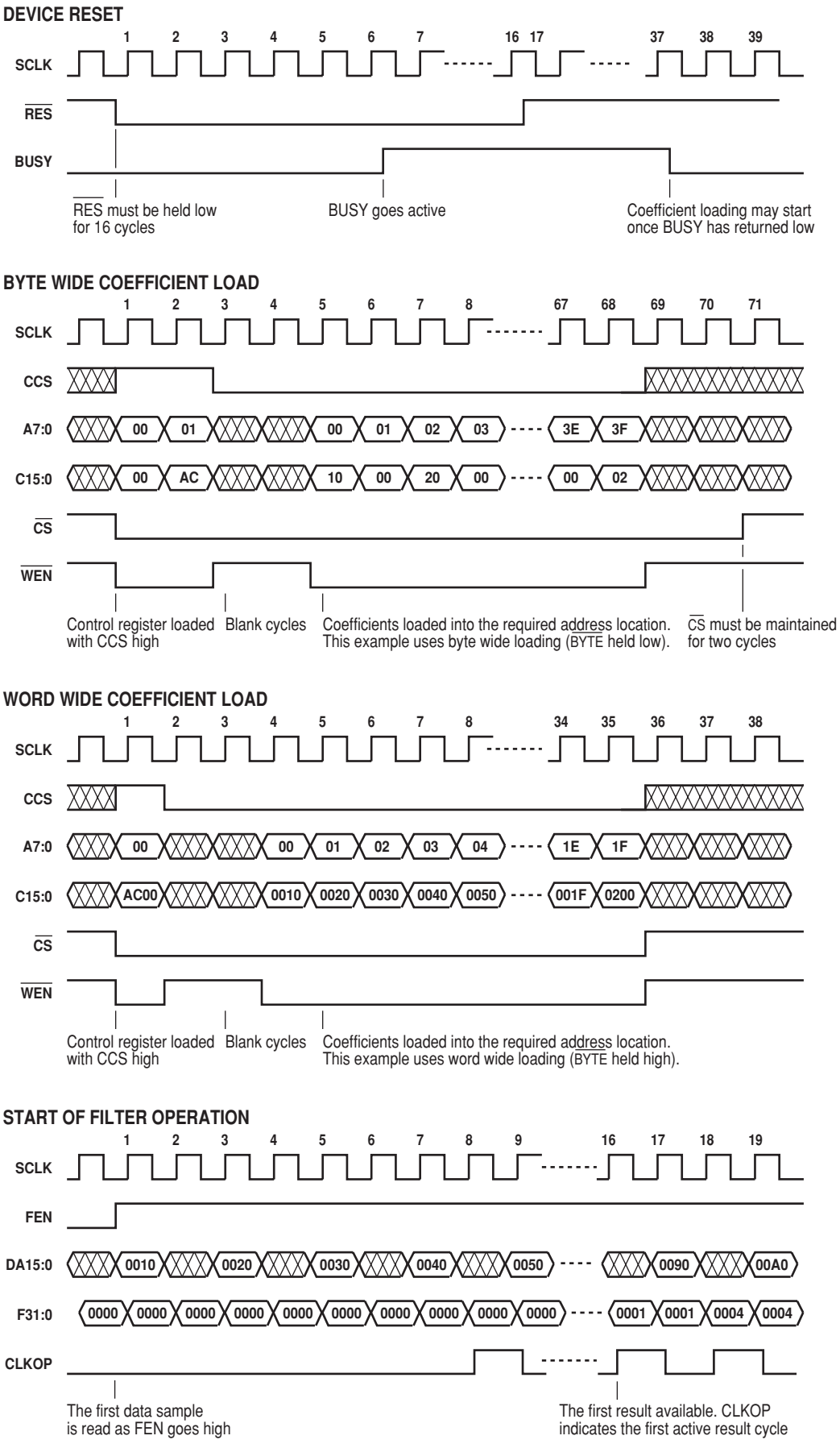


Fig. 18 Device startup timing diagrams

CONTROL REGISTER

The internal operation of the VP16256 is controlled by the status of a 16-bit control register. In the dual filter modes both networks are controlled by the same register. The significance of the various bits are shown in Table 6. Tables 7 and 8 define the control register bit interdependence for the filter and bank swapping modes.

Bits	Decode	Function
15	0	Dual filter mode
15	1	Single filter mode
14:13	00	Sample rate is the system clock
14:13	01	Sample rate is half the system clock
14:13	10	Sample rate is quarter the system clock
14:13	11	Sample rate is eighth the system clock
12	0	Output rate equals the input rate
12	1	Decimate-by-two
11:10	00	Intermediate device
11:10	01	Interface device
11:10	10	Termination device
11:10	11	Single device
9:8	00	These bits MUST be at logical zero
7	0	Bank swap is controlled by input pin
7	1	Bank swap is controlled by Bit 6
6	0	Lower bank if bit 7 is set
6	1	Upper bank if bit 7 is set
5	0	Normal Bank Swap
5	1	Bank swap on every sample clock
4	0	Two independent filters
4	1	Two filters in cascade
3:0		These bits MUST be at logical zero

Table 6 Control register bit allocation

The control register is double buffered. This allows the writing of a new control word without affecting the current operation of the device. To activate the new control register after it has been written to the device the bank swap signal must be toggled. After a reset the active control register is loaded directly and bank swap need not be used.

Control Register Bits		Function
15	4	
0	0	Two independent filters
0	1	Two filters in cascade
1	X	Single Filter

Table 7 Control register filter mode bits

Control Register Bits			Function
7	6	5	
0	X	0	Control by input pin
1	0	0	Lower bank selected
1	1	0	Upper bank selected
X	X	1	Swap on every sample clock

Table 8 Control register bank swap bits

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{DD}	−0·5V to +7·0V
Input voltage V_{IN}	−0·5V to V_{DD} +0·5V
Output voltage V_{OUT}	−0·5V to V_{DD} +0·5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	−65°C to+150°C
Ambient temperature with power applied T_{AMB}	0°C to+70°C
Junction temperature with power applied T_J	120°C
Package power dissipation	2500mW
Thermal resistance, junction-to-case θ_{JC}	1·0 °C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation should not be exceeded for more than1 second, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.
5. The θ_{JC} data assumes that heat is extracted from the bottom of the package via the integral heat sink.
6. The metal 'heat slug' in the base of the package is connected to the substrate, which is at V_{DD} potential.

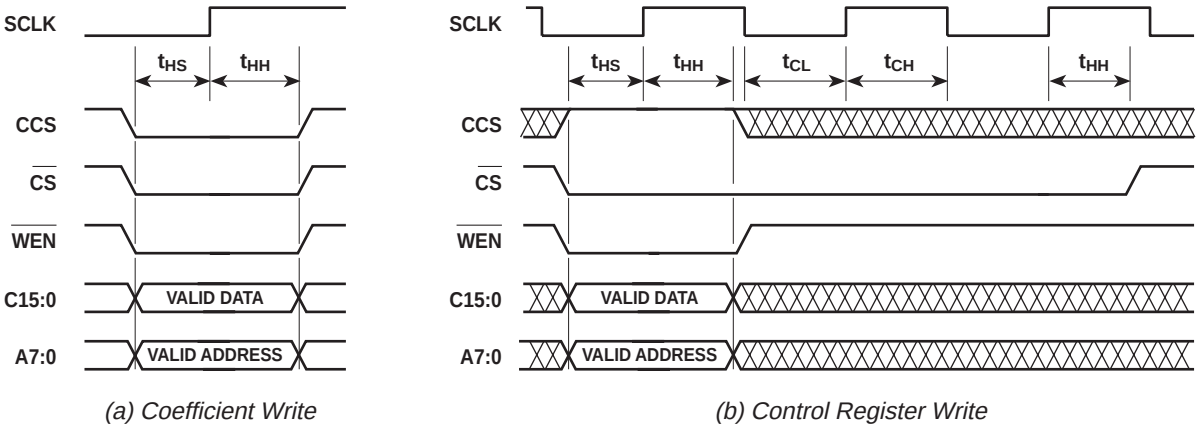


Fig. 19 Remote Master setup and hold timings

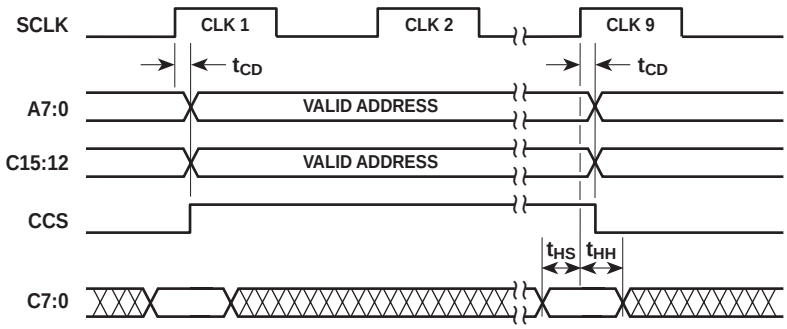


Fig. 20 EPROM load timings

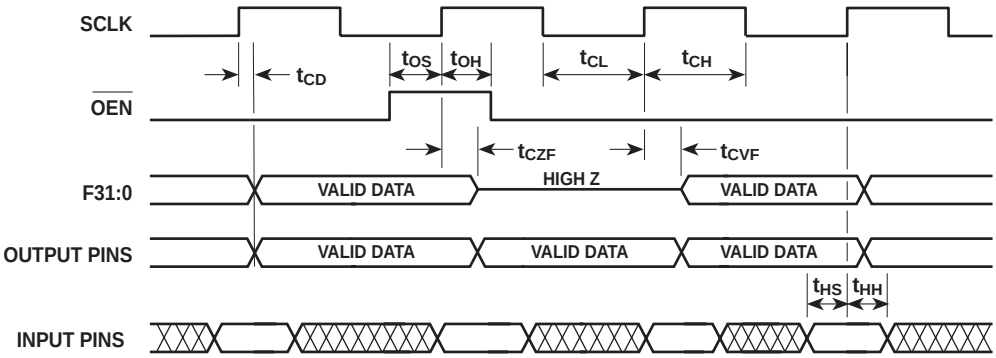


Fig. 21 Operating timings

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions, unless otherwise stated:

T_{AMB} = 0°C to +70°C, T_J = +120°C, V_{DD} = +5V±10%, GND = 0V

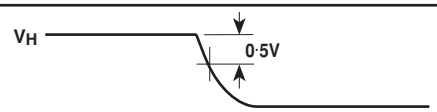
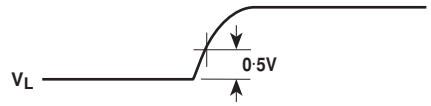
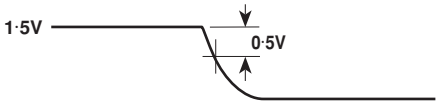
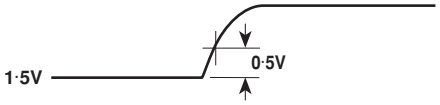
Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2·4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0·4	V	I_{OH} = 4mA
Input high voltage (CMOS)	V_{IH}	3·5		-	V	SCLK input only
Input low voltage (CMOS)	V_{IL}	-		1·0	V	SCLK input only
Input high voltage (TTL)	V_{IH}	2·0		-	V	All other inputs
Input low voltage (TTL)	V_{IL}	-		0·8	V	All other inputs
Input leakage current	I_{IN}	−10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	−50		+50	µA	GND < V_{OUT} < V_{DD}
Output short circuit current	I_{OS}	10		300	mA	V_{DD} = +5·5V

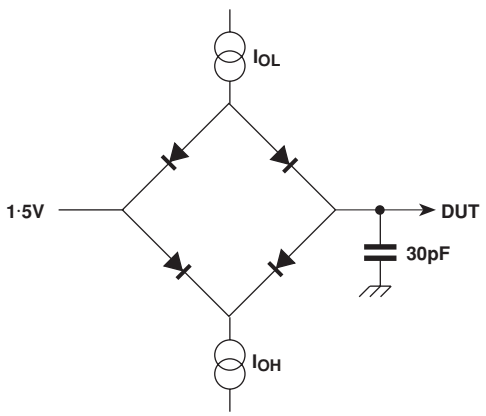
Switching Characteristics (see Figs. 19, 20 and 21)

Characteristic	Symbol	VP16256-27			VP16256-40			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Input signal setup to clock rising edge	t_{HS}	8		-	7		-	ns	
Input signal hold after clock rising edge	t_{HH}	0		-	0		-	ns	
$\overline{OEN}$ set up to clock rising edge	t_{OS}	20		-	20		-	ns	
$\overline{OEN}$ hold after clock rising edge	t_{OH}	4		-	4		-	ns	
Clock rising edge to output signal valid	t_{CD}	5		18	5		17	ns	30pF
Clock frequency	f_{SCLK}	-		27	-		40	MHz	
Clock high time	t_{CH}	14		-	10		-	ns	
Clock low time	t_{CL}	14		-	10		-	ns	
Clock to data valid F bus from high impedance	t_{CVF}	-		35	-		23	ns	See Fig. 22
Clock to data high impedance F bus	t_{CZF}	-		35	-		23	ns	See Fig. 22
V_{DD} current	I_{DD}		290	325		395	450	mA	See Note 1

NOTE 1. V_{DD} = +5·5V, outputs unloaded, clock frequency = Max.

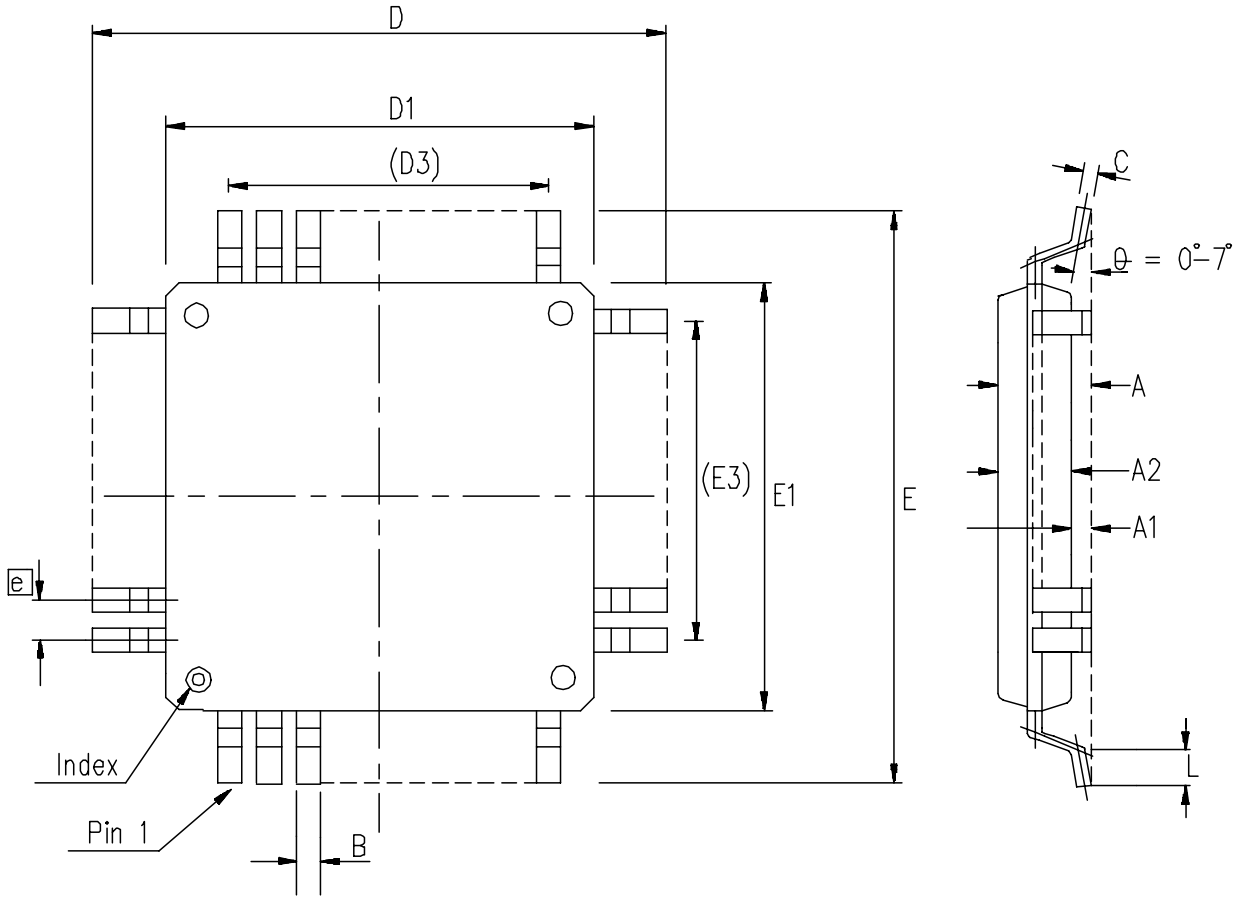
Test	Waveform measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to output low	
Delay from output high impedance to output high	

V_H is the voltage reached when the output is driven high
VL is the voltage reached when the output is driven low



Three state delay measurement load

Fig. 22 Three state delay measurement



	Min mm	Max mm	Min Inches	Max Inches
A	3.68	4.07	0.145	0.160
A1	0.25	0.43	0.010	0.017
A2	3.39	3.59	0.133	0.141
D	30.35	30.85	1.195	1.215
D1	27.90	28.10	1.098	1.106
D3	25.50 REF		1.004 REF	
E	30.35	30.85	1.195	1.215
E1	27.90	28.10	1.098	1.106
E3	25.50 REF		1.004 REF	
L	0.78	1.03	0.031	0.041
e	0.50 BSC		0.0197 BSC	
B	0.16	0.27	0.006	0.011
C	0.13	0.20	0.005	0.008
N	208		208	

NOTES: –
1. Controlling dimensions are in MM.
2. Maximum allowable die thickness to be assembled in this pkg. family is 0.51(0.020") millimeters.

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ISSUE	1				
ACN	179334				
DATE	26.JUN.95				
APPROVED					

MITEL SEMICONDUCTOR

Title:
208 Lead PowerQuad (II)
Outline drawing (B+2.6mm) (GH)

Drawing Number
GPD00098



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