# DS92LV090A 9 Channel Bus LVDS Transceiver

**Check for Samples: DS92LV090A**

## FEATURES

- **Bus LVDS Signaling**
- **3.2 Nanosecond Propagation Delay Max**
- **Chip to Chip Skew ±800ps**
- **Low Power CMOS Design**
- **High Signaling Rate Capability (Above 100 Mbps)**
- **0.1V to 2.3V Common Mode Range for $V_{ID}$ = 200mV**
- **±100 mV Receiver Sensitivity**
- **Supports Open and Terminated Failsafe on Port Pins**
- **3.3V Operation**
- **Glitch Free Power Up/Down (Driver & Receiver Disabled)**
- **Light Bus Loading (5 pF Typical) per Bus LVDS Load**
- **Designed for Double Termination Applications**
- **Balanced Output Impedance**
- **Product Offered in 64 Pin LQFP Package**
- **High Impedance Bus Pins on Power off ($V_{CC}$ = 0V)**
- **Driver Channel to Channel Skew (Same Device) 230ps Typical**
- **Receiver Channel to Channel Skew (Same Device) 370ps Typical**

## DESCRIPTION

The DS92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is less than ±100 mV over a ±1V common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels. (See Applications Information Section for more details.)

## Simplified Functional Diagram

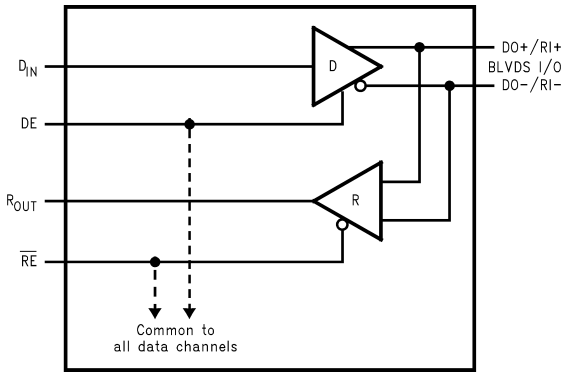



**Figure 1.**

## Connection Diagram

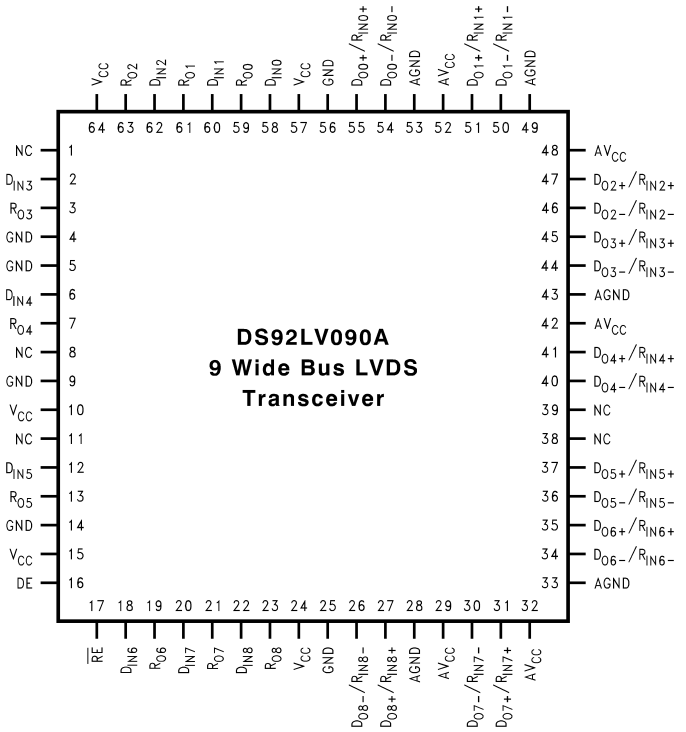



**Figure 2. Top View**
**Package Number PM0064**

### PIN DESCRIPTIONS

| Pin Name | Pin # | Input/Output | Descriptions |
|---|---|---|---|
| DO+/RI+ | 27, 31, 35, 37, 41, 45, 47, 51, 55 | I/O | True Bus LVDS Driver Outputs and Receiver Inputs. |
| DO−/RI− | 26, 30, 34, 36, 40, 44, 46, 50, 54 | I/O | Complimentary Bus LVDS Driver Outputs and Receiver Inputs. |
| $D_{IN}$ | 2, 6, 12, 18, 20, 22, 58, 60, 62 | I | TTL Driver Input. |
| RO | 3, 7, 13, 19, 21, 23, 59, 61, 63 | O | TTL Receiver Output. |
| $\overline{RE}$ | 17 | I | Receiver Enable TTL Input (Active Low). |
| DE | 16 | I | Driver Enable TTL Input (Active High). |
| GND | 4, 5, 9, 14, 25, 56 | Power | Ground for digital circuitry (must connect to GND on PC board). These pins connected internally. |
| $V_{CC}$ | 10, 15, 24, 57, 64 | Power | $V_{CC}$ for digital circuitry (must connect to $V_{CC}$ on PC board). These pins connected internally. |
| AGND | 28, 33, 43, 49, 53 | Power | Ground for analog circuitry (must connect to GND on PC board). These pins connected internally. |
| $AV_{CC}$ | 29, 32, 42, 48, 52 | Power | Analog $V_{CC}$ (must connect to $V_{CC}$ on PC board). These pins connected internally. |
| NC | 1, 8, 11, 38, 39 | N/A | Leave open circuit, do not connect. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)(3)

| | | |
|---|---|---|
| Supply Voltage ($V_{CC}$) | | 4.0V |
| Enable Input Voltage (DE, $\overline{RE}$) | | −0.3V to ($V_{CC}$ +0.3V) |
| Driver Input Voltage ($D_{IN}$) | | −0.3V to ($V_{CC}$ +0.3V) |
| Receiver Output Voltage ($R_{OUT}$) | | −0.3V to ($V_{CC}$ +0.3V) |
| Bus Pin Voltage (DO/RI±) | | −0.3V to +3.9V |
| ESD (HBM 1.5 kΩ, 100 pF) | | >4.5 kV |
| Driver Short Circuit Duration | | momentary |
| Receiver Short Circuit Duration | | momentary |
| Maximum Package Power Dissipation at 25°C | LQFP | 1.74 W |
| | Derate LQFP Package | 13.9 mW/°C |
| | $\theta_{ja}$ | 71.7°C/W |
| | $\theta_{jc}$ | 10.9°C/W |
| Junction Temperature | | +150°C |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | | 260°C |

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except $V_{OD}$, $\Delta V_{OD}$ and $V_{ID}$.
(2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 3.0 | 3.6 | V |
| Receiver Input Voltage | 0.0 | 2.4 | V |
| Operating Free Air Temperature | −40 | +85 | °C |
| Maximum Input Edge Rate (20% to 80%) (1) | | | Δt/ΔV |
| Data | | 1.0 | ns/V |
| Control | | 3.0 | ns/V |

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, $Z_O$ = 50Ω, $t_r$, $t_f$ = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

## DC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (1)(2)

| Symbol | Parameter | Conditions | | Pin | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Output Differential Voltage | $R_L$ = 27Ω, Figure 3 | | DO+/RI+, DO−/RI− | 240 | 300 | 460 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | | | 27 | mV |
| $V_{OS}$ | Offset Voltage | | | | 1.1 | 1.3 | 1.5 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change | | | | | 5 | 10 | mV |
| $V_{OH}$ | Driver Output High Voltage (3) | $R_L$ = 27Ω | | | | 1.4 | 1.65 | V |
| $V_{OL}$ | Driver Output Low Voltage (3) | $R_L$ = 27Ω | | | 0.95 | 1.1 | | V |
| $I_{OSD}$ | Output Short Circuit Current (4) | $V_{OD}$ = 0V, DE = $V_{CC}$, Driver outputs shorted together | | | | \|36\| | \|65\| | mA |
| $V_{OH}$ | Voltage Output High (5) | $V_{ID}$ = +300 mV | $I_{OH}$ = −400 µA | $R_{OUT}$ | $V_{CC}$−0.2 | | | V |
| | | Inputs Open | | | $V_{CC}$−0.2 | | | V |
| | | Inputs Terminated, $R_L$ = 27Ω | | | $V_{CC}$−0.2 | | | V |
| $V_{OL}$ | Voltage Output Low | $I_{OL}$ = 2.0 mA, $V_{ID}$ = −300 mV | | | | 0.05 | 0.075 | V |
| $I_{OD}$ | Receiver Output Dynamic Current (4) | $V_{ID}$ = 300mV, $V_{OUT}$ = $V_{CC}$−1.0V | | | −110 | \|75\| | | mA |
| | | $V_{ID}$ = −300mV, $V_{OUT}$ = 1.0V | | | | \|75\| | 110 | mA |
| $V_{TH}$ | Input Threshold High | DE = 0V, $V_{CM}$ = 1.5V | | DO+/RI+, DO−/RI− | | | +100 | mV |
| $V_{TL}$ | Input Threshold Low | | | | −100 | | | mV |
| $V_{CMR}$ | Receiver Common Mode Range | | | | $\|V_{ID}\|/2$ | | 2.4 − $\|V_{ID}\|/2$ | V |
| $I_{IN}$ | Input Current | DE = 0V, $\overline{RE}$ = 2.4V, $V_{IN}$ = +2.4V or 0V | | | −20 | ±1 | +20 | µA |
| | | $V_{CC}$ = 0V, $V_{IN}$ = +2.4V or 0V | | | −20 | ±1 | +20 | µA |
| $V_{IH}$ | Minimum Input High Voltage | | | $D_{IN}$, DE, $\overline{RE}$ | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Maximum Input Low Voltage | | | | GND | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{CC}$ or 2.4V | | | −20 | ±10 | +20 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = GND or 0.4V | | | −20 | ±10 | +20 | µA |
| $V_{CL}$ | Input Diode Clamp Voltage | $I_{CLAMP}$ = −18 mA | | | −1.5 | −0.8 | | V |
| $I_{CCD}$ | Power Supply Current Drivers Enabled, Receivers Disabled | No Load, DE = $\overline{RE}$ = $V_{CC}$, DIN = $V_{CC}$ or GND | | $V_{CC}$ | | 55 | 80 | mA |
| $I_{CCR}$ | Power Supply Current Drivers Disabled, Receivers Enabled | DE = $\overline{RE}$ = 0V, $V_{ID}$ = ±300mV | | | | 73 | 80 | mA |
| $I_{CCZ}$ | Power Supply Current, Drivers and Receivers TRI-STATE | DE = 0V; $\overline{RE}$ = $V_{CC}$, DIN = $V_{CC}$ or GND | | | | 35 | 80 | mA |
| $I_{CC}$ | Power Supply Current, Drivers and Receivers Enabled | DE = $V_{CC}$; $\overline{RE}$ = 0V, DIN = $V_{CC}$ or GND, $R_L$ = 27Ω | | | | 170 | 210 | mA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{CC}$ = 0V or OPEN, $D_{IN}$, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED}$ = 3.6V (Port Pins) | | DO+/RI+, DO−/RI− | −20 | | +20 | µA |
| $C_{OUTPUT}$ | Capacitance @ Bus Pins | | | DO+/RI+, DO−/RI− | | 5 | | pF |
| $c_{OUTPUT}$ | Capacitance @ $R_{OUT}$ | | | $R_{OUT}$ | | 7 | | pF |

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except $V_{OD}$, $\Delta V_{OD}$ and $V_{ID}$.
(2) All typicals are given for $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise stated.
(3) The DS92LV090A functions within datasheet specification when a resistive load is applied to the driver outputs.
(4) Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.
(5) $V_{OH}$ failsafe terminated test performed with 27Ω connected between RI+ and RI− inputs. No external voltage is applied.

## AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DIFFERENTIAL DRIVER TIMING REQUIREMENTS** | | | | | | |
| $t_{PHLD}$ | Differential Prop. Delay High to Low (2) | $R_L$ = 27Ω, Figure 4, Figure 5, $C_L$ = 10 pF | 0.6 | 1.4 | 2.2 | ns |
| $t_{PLHD}$ | Differential Prop. Delay Low to High (2) | | 0.6 | 1.4 | 2.2 | ns |
| $t_{SKD1}$ | Differential Skew $\|t_{PHLD}–t_{PLHD}\|$ (3) | | | 80 | | ps |
| $t_{SKD2}$ | Chip to Chip Skew (4) | | | | 1.6 | ns |
| $t_{SKD3}$ | Channel to Channel Skew (5) | | | 0.25 | 0.45 | ns |
| $t_{TLH}$ | Transition Time Low to High | | | 0.6 | 1.2 | ns |
| $t_{THL}$ | Transition Time High to Low | | | 0.5 | 1.2 | ns |
| $t_{PHZ}$ | Disable Time High to Z | $R_L$ = 27Ω, Figure 6, Figure 7, $C_L$ = 10 pF | | 3 | 8 | ns |
| $t_{PLZ}$ | Disable Time Low to Z | | | 3 | 8 | ns |
| $t_{PZH}$ | Enable Time Z to High | | | 3 | 8 | ns |
| $t_{PZL}$ | Enable Time Z to Low | | | 3 | 8 | ns |
| **DIFFERENTIAL RECEIVER TIMING REQUIREMENTS** | | | | | | |
| $t_{PHLD}$ | Differential Prop. Delay High to Low (2) | Figure 8, Figure 9, $C_L$ = 35 pF | 1.6 | 2.4 | 3.2 | ns |
| $t_{PLHD}$ | Differential Prop Delay Low to High (2) | | 1.6 | 2.4 | 3.2 | ns |
| $t_{SDK1}$ | Differential Skew $\|t_{PHLD}–t_{PLHD}\|$ (3) | | | 80 | | ps |
| $t_{SDK2}$ | Chip to Chip Skew (4) | | | | 1.6 | ns |
| $t_{SDK3}$ | Channel to Channel Skew (5) | | | 0.35 | 0.60 | ns |
| $t_{TLH}$ | Transition Time Low to High | | | 1.5 | 2.5 | ns |
| $t_{THL}$ | Transition Time High to Low | | | 1.5 | 2.5 | ns |
| $t_{PHZ}$ | Disable Time High to Z | $R_L$ = 500Ω, Figure 10, Figure 11, $C_L$ = 35 pF | | 4.5 | 10 | ns |
| $t_{PLZ}$ | Disable Time Low to Z | | | 3.5 | 8 | ns |
| $t_{PZH}$ | Enable Time Z to High | | | 3.5 | 8 | ns |
| $t_{PZL}$ | Enable Time Z to Low | | | 3.5 | 8 | ns |

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, $Z_O$ = 50Ω, $t_r$, $t_f$ = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.
(2) Propagation delays are specified by design and characterization.
(3) $t_{SKD1}$ $|t_{PHLD}–t_{PLHD}|$ is the worse case skew between any channel and any device over recommended operation conditions.
(4) Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.
(5) Channel to Channel skew is the difference in driver output or receiver output propagation delay between any channels within a device, either edge.

## APPLICATIONS INFORMATION

General application guidelines and hints may be found in the following application notes: AN-808 (SNLA028), AN-903 (SNLA034), AN-971 (SNLA165), AN-977 (SNLA166), and AN-1108 (SNLA008).

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Two or three high frequency, multi-layer ceramic (MLC) surface mount (0.1 µF, 0.01 µF, 0.001 µF) in parallel should be used between each $V_{CC}$ and ground. The capacitors should be as close as possible to the $V_{CC}$ pin.
  - Multiple vias should be used to connect $V_{CC}$ and Ground planes to the pads of the by-pass capacitors.
  - In addition, randomly distributed by-pass capacitors should be used.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.
- Isolate TTL signals from Bus LVDS signals

MEDIA (CONNECTOR or BACKPLANE) SELECTION:

- Use controlled impedance media. The backplane and connectors should have a matched differential impedance.

**Table 1. Functional Table**

| MODE SELECTED | DE | $\overline{RE}$ |
|---|---|---|
| DRIVER MODE | H | H |
| RECEIVER MODE | L | L |
| TRI-STATE MODE | L | H |
| LOOP BACK MODE | H | L |

**Table 2. Transmitter Mode**

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| DE | $D_{IN}$ | DO+ | DO− |
| H | L | L | H |
| H | H | H | L |
| H | 0.8V< $D_{IN}$ <2.0V | X | X |
| L | X | Z | Z |

**Table 3. Receiver Mode(1)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{RE}$ | (RI+) – (RI−) | |
| L | L (< −100 mV) | L |
| L | H (> +100 mV) | H |
| L | −100 mV < $V_{ID}$ < +100 mV | X |
| H | X | Z |

(1) X = High or Low logic state
L = Low state
Z = High impedance state
H = High state

## Test Circuits and Timing Waveforms

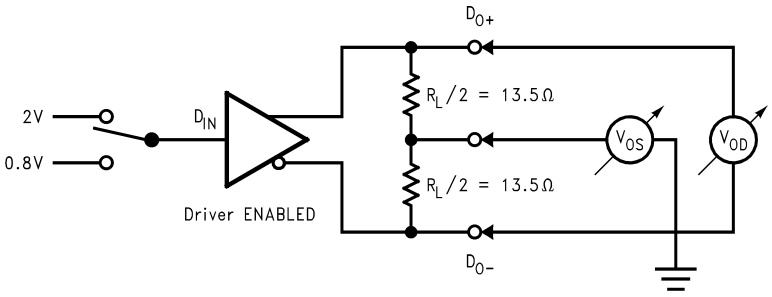



**Figure 3. Differential Driver DC Test Circuit**

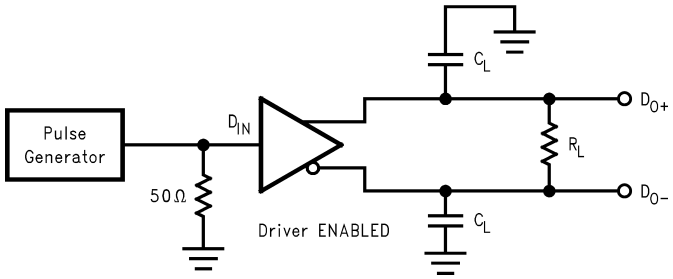



**Figure 4. Differential Driver Propagation Delay and Transition Time Test Circuit**

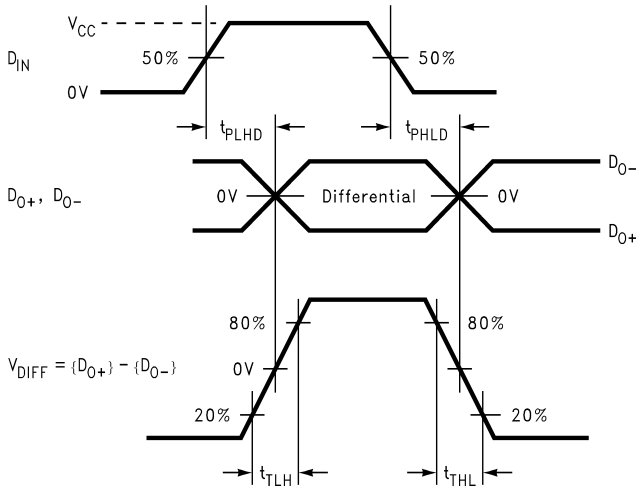



**Figure 5. Differential Driver Propagation Delay and Transition Time Waveforms**

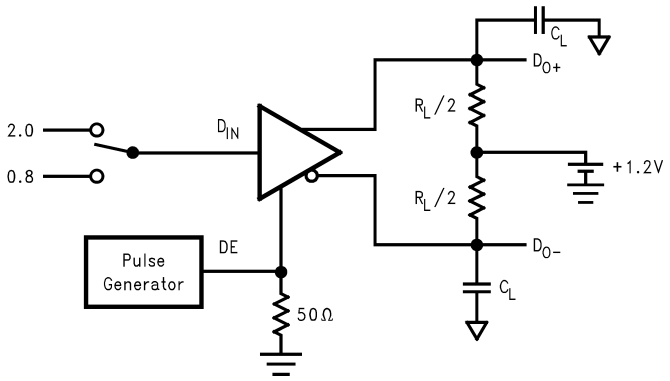



**Figure 6. Driver TRI-STATE Delay Test Circuit**

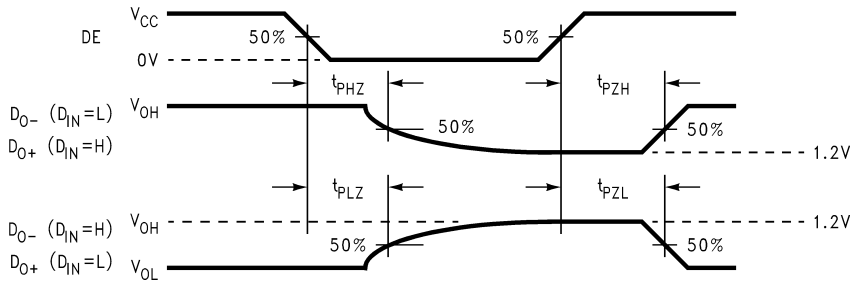



**Figure 7. Driver TRI-STATE Delay Waveforms**

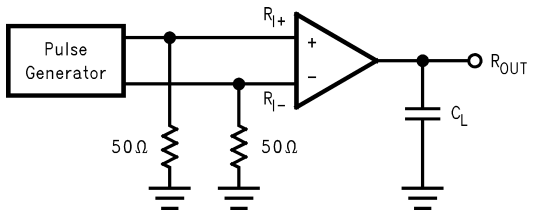



**Figure 8. Receiver Propagation Delay and Transition Time Test Circuit**

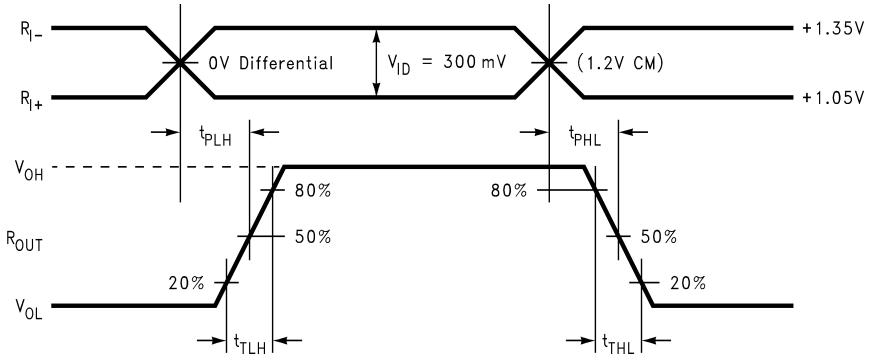



**Figure 9. Receiver Propagation Delay and Transition Time Waveforms**

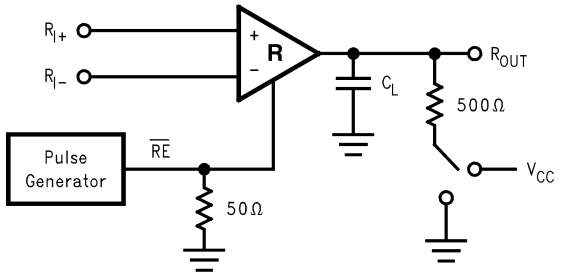



**Figure 10. Receiver TRI-STATE Delay Test Circuit**

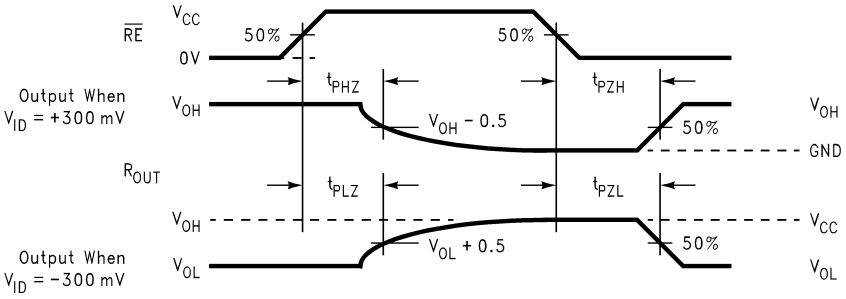



**Figure 11. Receiver TRI-STATE Delay Waveforms**

## Typical Bus Application Configurations

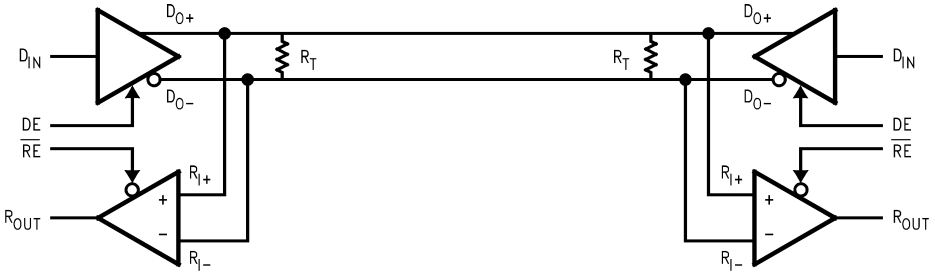


**Figure 12. Bi-Directional Half-Duplex Point-to-Point Applications**

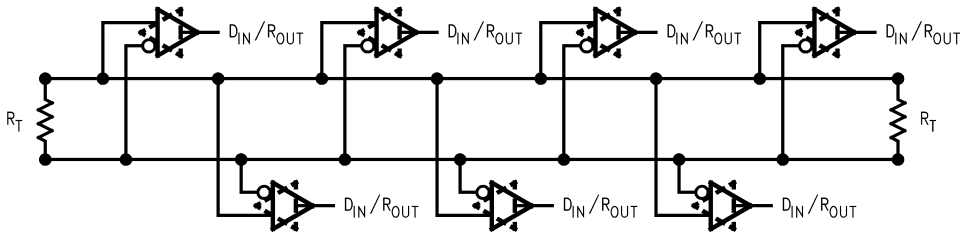


**Figure 13. Multi-Point Bus Applications**

## REVISION HISTORY

| Changes from Revision C (April 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 9 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS92LV090ATVEH/NOPB | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | DS92LV090A TVEH | Samples |
| DS92LV090ATVEHX/NOPB | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | DS92LV090A TVEH | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

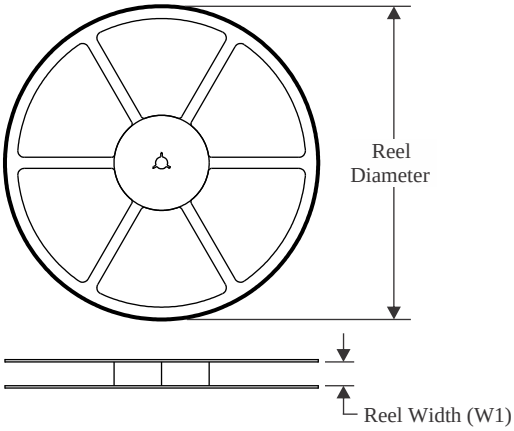
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

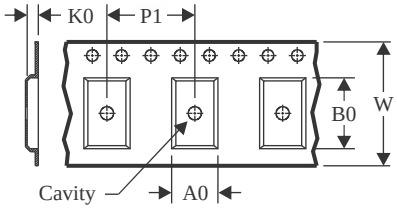
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

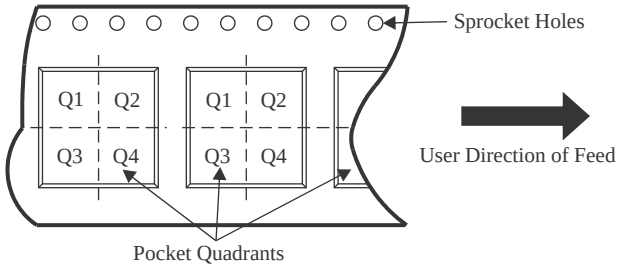



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

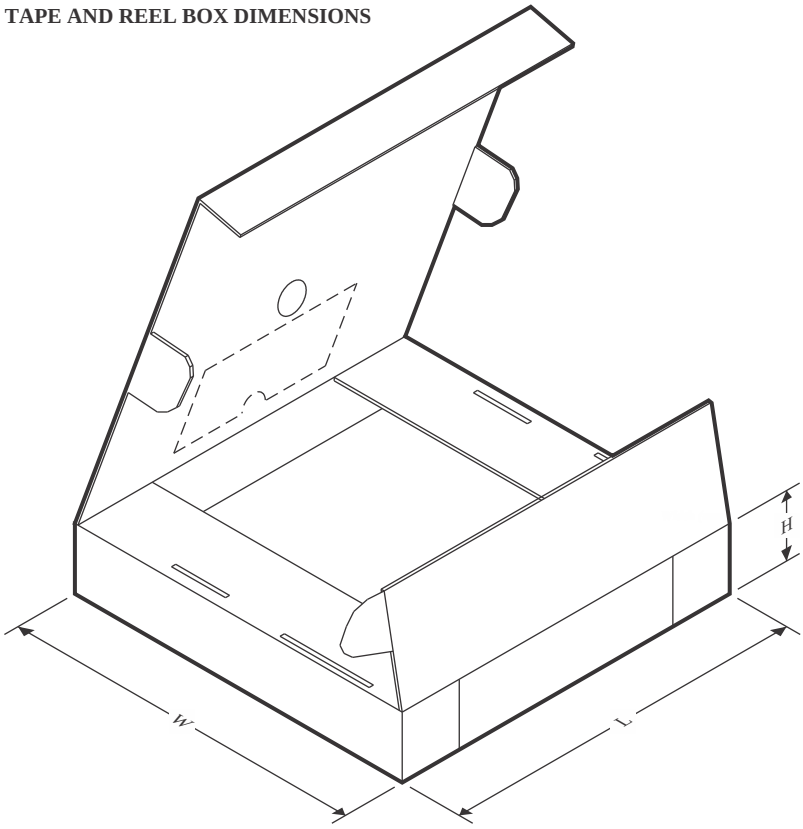
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS92LV090ATVEHX/ NOPB | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 12.35 | 12.35 | 2.2 | 16.0 | 24.0 | Q2 |

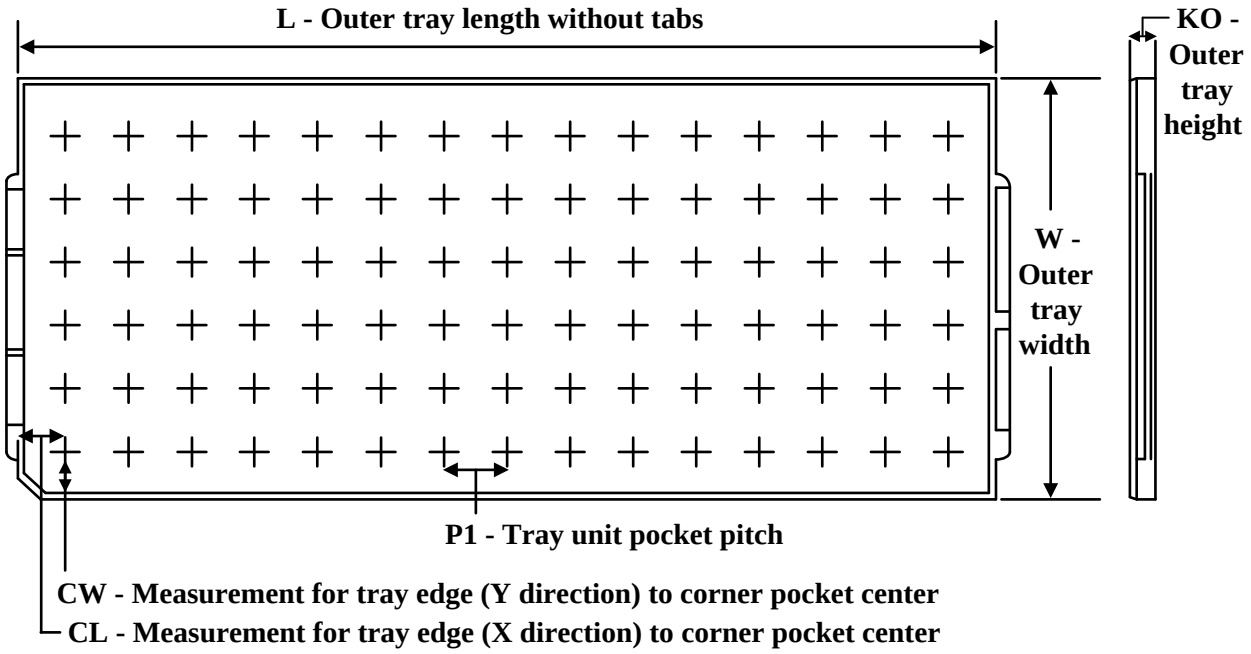
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS92LV090ATVEHX/ NOPB | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

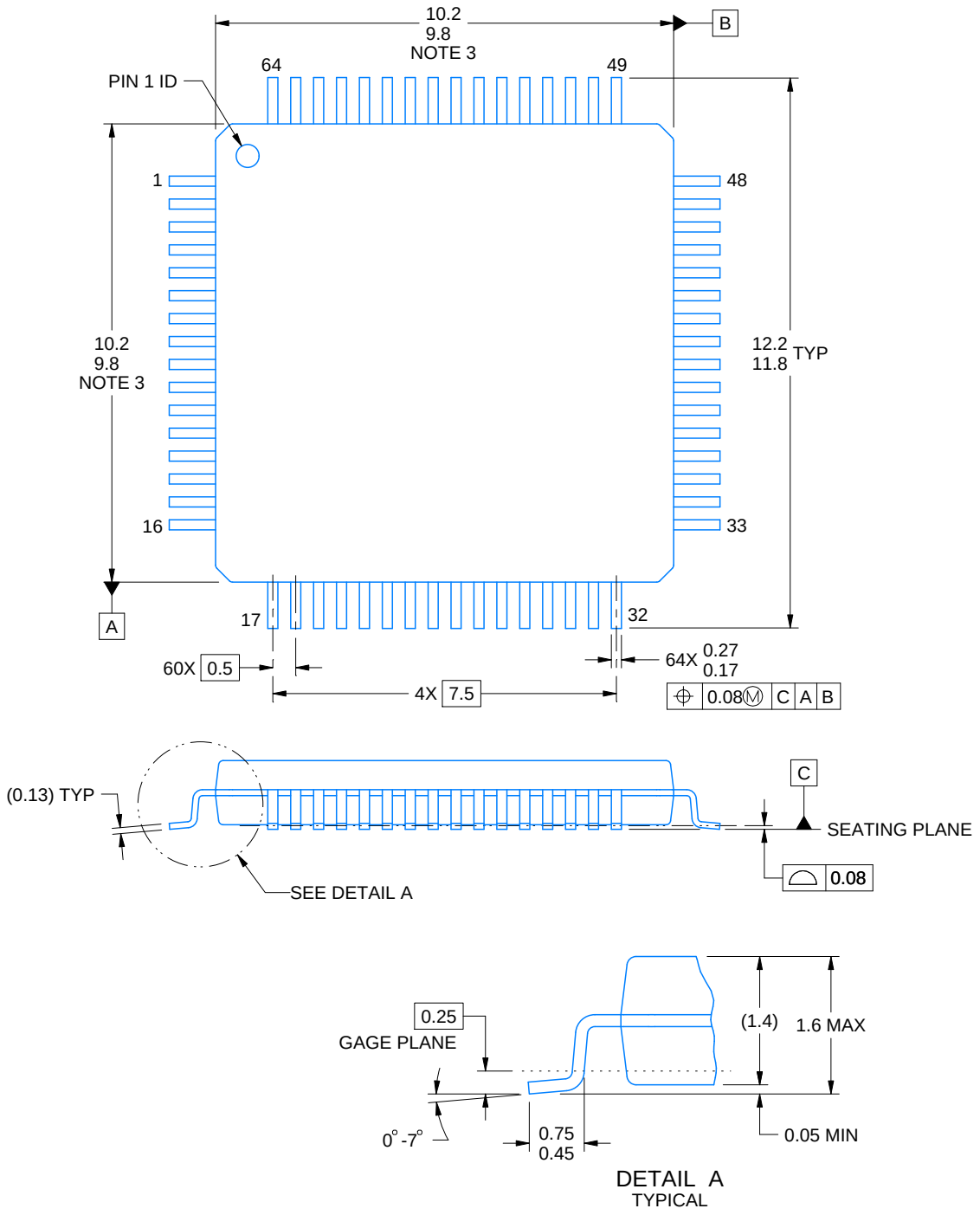
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS92LV090ATVEH/ NOPB | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 322.6 | 135.9 | 7620 | 15.2 | 13.1 | 13 |

# PACKAGE OUTLINE

## PM0064A

## LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

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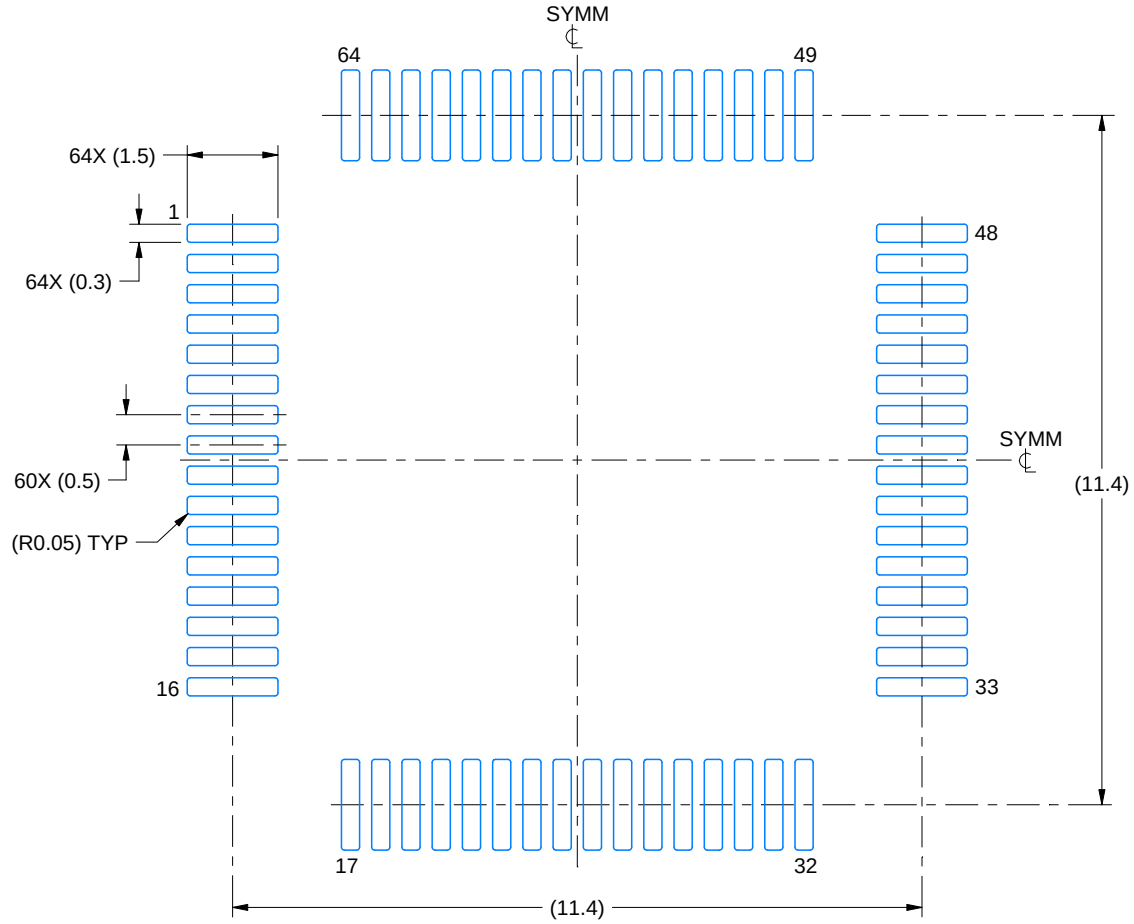
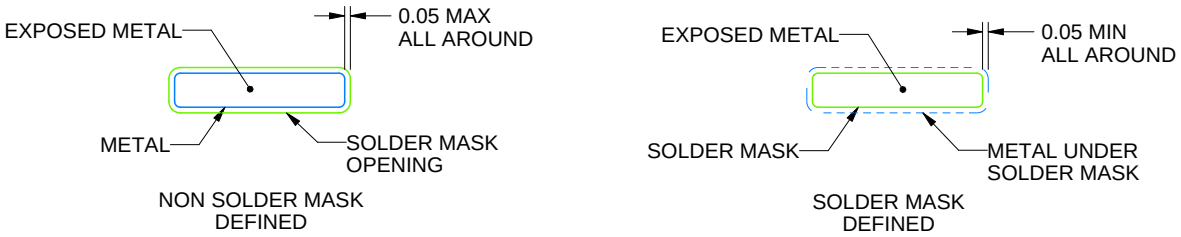
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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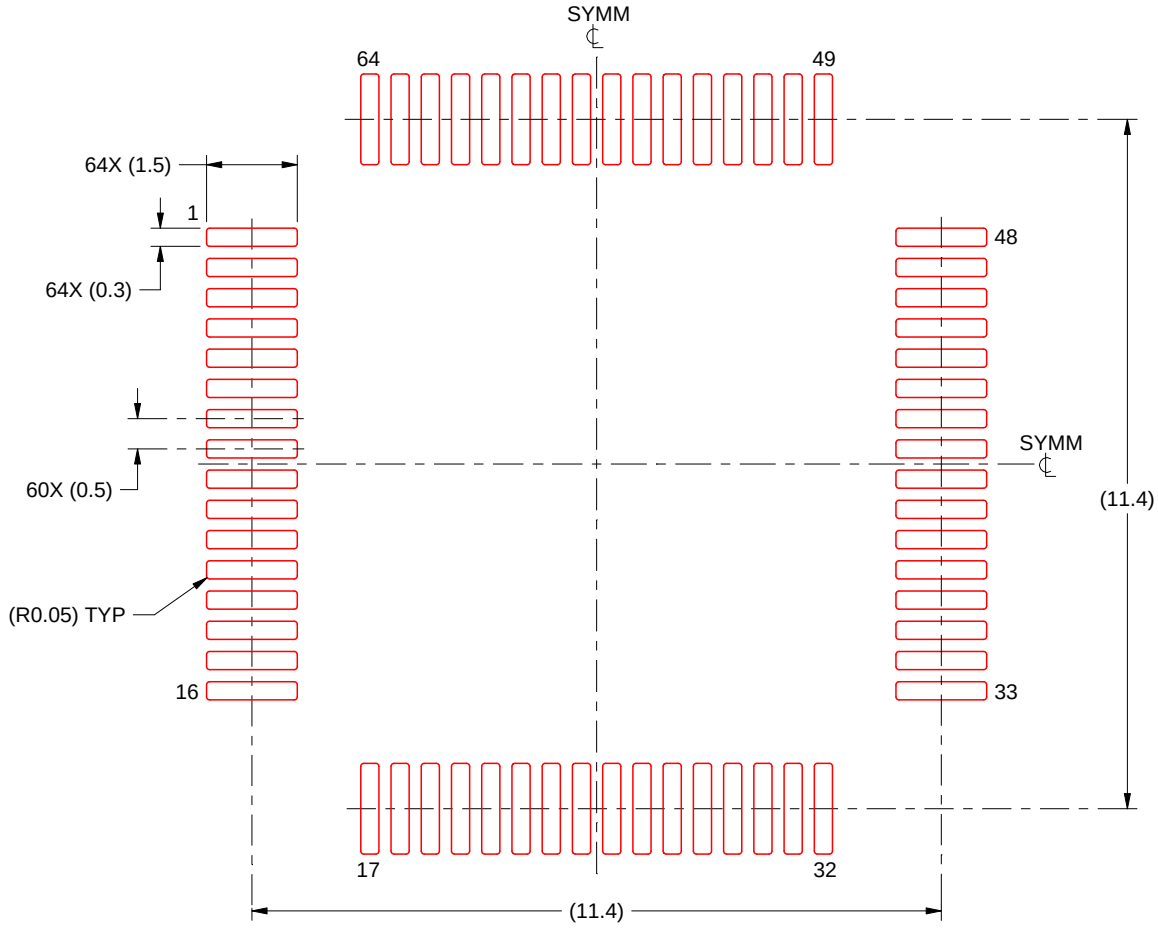
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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