DATA SHEET

SAA4955TJ
2.9-Mbit field memory

Product specification
Supersedes data of 1997 Sep 25
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Philips
Semiconductors



PHILIPS

2.9-Mbit field memory SAA4955TJ

FEATURES

- 2949264-bit field memory
- 245772 × 12-bit organization
- 3.3 V power supply
- Inputs fully TTL compatible when using an extra 5 V power supply
- High speed read and write operations
- FIFO operations:
  - full word continuous read and write
  - independent read and write pointers (asynchronous read and write access)
  - resettable read and write pointers
- Optional random access by block function (40 words per block) enabled during pointer reset operation
- Quasi static (internal self-refresh and clocking pauses of infinite length)
- Write mask function
- Cascade operation possible
- 16 Mbit CMOS DRAM process technology
- 40-pin SOJ Package.

GENERAL DESCRIPTION

The SAA4955TJ is a 2949264-bit field memory designed for advanced TV applications such as 100/120 Hz TV, PALplus, PIP and 3D comb filter. The maximum storage depth is 245772 words × 12 bits. A FIFO operation with full word continuous read and write could be used as a data delay, for example. A FIFO operation with asynchronous read and write could be used as a data rate multiplier. Here the data is written once, then read as many times as required without being overwritten by new data. In addition to the FIFO operations, a random block access mode is accessible during the pointer reset operation. When this mode is enabled, reading and/or writing may begin at, or proceed from, the start address of any of the 6144 blocks. Each block is 40 words in length. Two or more SAA4955TJs can be cascaded to provide greater storage depth or a longer delay, without the need for additional circuitry.

The SAA4955TJ contains separate 12-bit wide serial ports for reading and writing. The ports are controlled and clocked separately, so asynchronous read and write operations are supported. Independent read and write clock rates are possible. Addressing is controlled by read and write address pointers. Before a controlled write operation can begin, the write pointer must be set to zero or to the beginning of a valid address block. Likewise, the read pointer must be set to zero or to the beginning of a valid address block before a controlled read operation can begin.

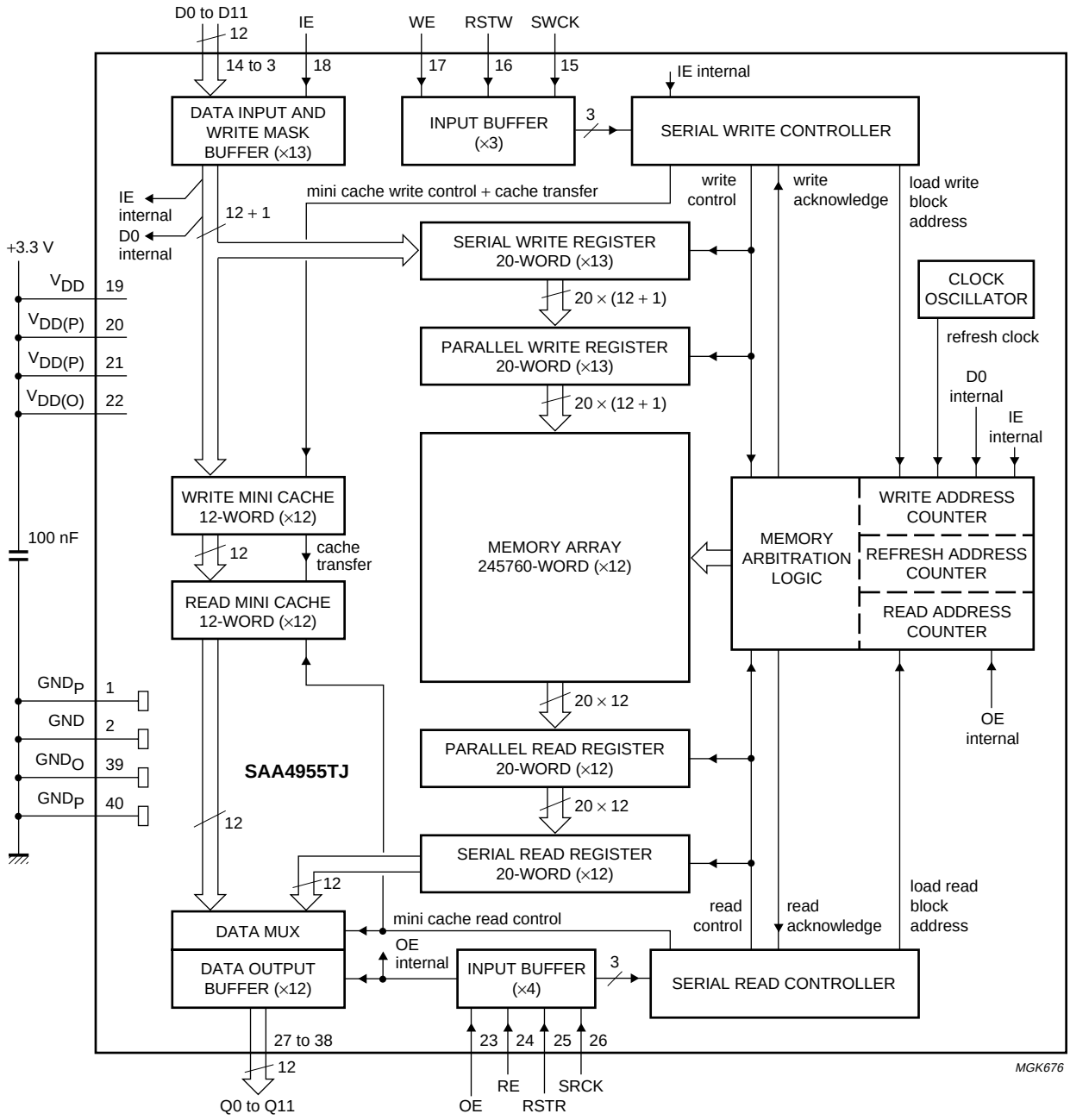
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$T_{cy(SWCK)}$	WRITE cycle time (SWCK)	see Fig.3	26	–	–	ns
$T_{cy(SRCK)}$	READ cycle time (SRCK)	see Fig.10	26	–	–	ns
t_{ACC}	READ access time after SRCK	see Fig.10	–	–	21	ns
V_{DD}, $V_{DD(O)}$	supply voltage (pins 19 and 22)		3.0	3.3	3.6	V
$V_{DD(P)}$	supply voltage (pins 20 and 21)		3.0	3.3	5.5	V
$I_{DD(tot)}$	total supply current ($I_{DD(tot)} = I_{DD} + I_{DD(O)} + I_{DD(P)}$)	minimum read/write cycle; outputs open	–	22	70	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4955TJ	SOJ40	plastic small outline package; 40 leads (J-bent); body width 10.16 mm	SOT449-1

BLOCK DIAGRAM



Pins 20 and 21 ($V_{DD(P)}$) should be connected to the supply voltage of the driving circuit that generates the input voltages. This could be, for instance, 5.5 V instead of 3.3 V. Pins 19 and 22 (V_{DD} and $V_{DD(O)}$) require a 3.3 V supply.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
GND_P	1	ground	ground for protection circuits
GND	2	ground	general purpose ground
D11	3	digital input	data input 11
D10	4	digital input	data input 10
D9	5	digital input	data input 9
D8	6	digital input	data input 8
D7	7	digital input	data input 7
D6	8	digital input	data input 6
D5	9	digital input	data input 5
D4	10	digital input	data input 4
D3	11	digital input	data input 3
D2	12	digital input	data input 2
D1	13	digital input	data input 1
D0	14	digital input	data input 0
SWCK	15	digital input	serial write clock
RSTW	16	digital input	write reset clock
WE	17	digital input	write enable
IE	18	digital input	input enable
V_{DD}	19	supply	+3.3 V general purpose supply voltage (see figure note in Fig.1)
$V_{DD(P)}$	20	supply	+3.3 to 5.5 V supply voltage for protection circuits (see figure note in Fig.1)
$V_{DD(P)}$	21	supply	+3.3 to 5.5 V supply voltage for protection circuits
$V_{DD(O)}$	22	supply	+3.3 V supply voltage for output circuits
OE	23	digital input	output enable
RE	24	digital input	read enable
RSTR	25	digital input	reset read
SRCK	26	digital input	serial read clock
Q0	27	digital output	data output 0
Q1	28	digital output	data output 1
Q2	29	digital output	data output 2
Q3	30	digital output	data output 3
Q4	31	digital output	data output 4
Q5	32	digital output	data output 5
Q6	33	digital output	data output 6
Q7	34	digital output	data output 7
Q8	35	digital output	data output 8
Q9	36	digital output	data output 9
Q10	37	digital output	data output 10
Q11	38	digital output	data output 11
GND_O	39	ground	ground for output circuits
GND_P	40	ground	ground for protection circuits

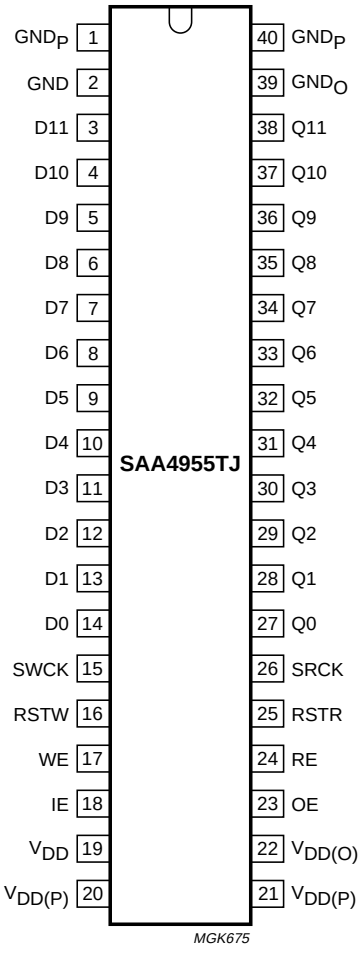


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Write operation

Write operations are controlled by the SWCK, RSTW, WE and IE signals. A write operation starts with a reset write address pointer (RSTW) operation, followed by a sequence SWCK clock cycles during which time WE and IE must be held HIGH. Write operations between two successive reset write operations must contain at least 40 SWCK write clock cycles while WE is HIGH. To transfer data temporarily stored in the serial write registers to the memory array, a reset write operation is required after the last write operation.

RESET WRITE: RSTW

The first positive transition of SWCK after RSTW goes from LOW to HIGH resets the write address pointer to the lowest address (−12 decimal), regardless of the state of WE (see Figs 3 and 4). RSTW set-up ($t_{su(RSTW)}$) and hold ($t_{h(RSTW)}$) times are referenced to the rising edge of SWCK (see Fig.3). The reset write operation may also be asynchronously related to the SWCK signal if WE is LOW.

RSTW needs to stay LOW for a single SWCK cycle before another reset write operation can take place. If RSTW is HIGH for 1024 SWCK write clock cycles while WE is HIGH, the SAA4955TJ will enter a built-in test mode and will not be in regular operation.

RANDOM WRITE BLOCK ACCESS MODE

The SAA4955TJ will enter random write block access mode if the following signal sequence is applied to control inputs IE and WE during the first four SWCK write clock cycles after a reset write (see Figs 5 and 6):

At the 1st and 2nd positive transitions of SWCK, IE must be LOW and WE must be HIGH

At the 3rd and 4th positive transitions of SWCK, IE must be HIGH and WE must be LOW

At the 5th positive transition of SWCK, the state of WE determines which input pin is used for the block address. If WE is LOW the Most Significant Bit (MSB) of the block address must be applied to the D0 input pin. If WE is HIGH, the Most Significant Bit (MSB) of the block address is applied to pin IE.

During the first four clock cycles, control signals WE and IE will function as defined for normal operation. The remaining 12 bits of the 13-bit write block address must be applied, in turn, to the selected input pin (D0 or IE) at the following 12 positive transitions of SWCK. The Least Significant Bit (LSB) of the write block address is applied at the 17th positive transition of SWCK. A write latency period of 18 additional SWCK clock cycles is required before write access to the new block address is possible. During this time, data is transferred from the serial write and parallel write registers into the memory array and the write pointer is set to the new block address.

Block address values between 0 and 6143 are valid. Values outside this range must be avoided because invalid block addresses can result in abnormal operation or a lock-up condition. Recovery from lock-up requires a standard reset write operation.

WE must remain LOW from the 3rd positive transition of SWCK to the 17th write latency SWCK clock cycle if the block address is applied to pin D0. If the block address is applied to pin IE, WE must be HIGH on the 5th positive transition of SWCK, may be HIGH or LOW on the 6th transition, and must be LOW from the 7th transition to the 17th write latency SWCK clock cycle.

At the 18th write latency SWCK clock cycle, IE and WE may be switched HIGH to prepare for writing new data at the next positive transition of SWCK. The complete write block access entry sequence is finished after the 18th write latency cycle.

The LOW-to-HIGH transition on RSTW required at the beginning of the sequence should not be repeated. Additional LOW-to-HIGH transitions on RSTW would disable write block address mode and reset the write pointer.

ADDRESS ORGANIZATION

Two different types of memory are used in the data address area: a mini cache for the first 12 data words after a reset write or a reset read, and a DRAM cell memory array with a 245760 word capacity. Each word is 12 bits long. The mini cache is needed to store data immediately after a reset operation since a latency period is required before read or write access to the memory array is possible. Latency periods are needed for read or write operations in random read or write block access modes because data is read from, or written to, the memory array. The data in the mini cache can only be accessed directly after a standard reset operation. It cannot be accessed in random read or write block access modes.

The address area reserved for the mini cache, accessible after a standard reset operation, is from decimal −12 to −1. The memory array starts at decimal 0 and ends at 245759. Decimal address 0 is identical to block address 0000H. Because a single block address is defined for every 40 words in the memory array, block address 0001H

corresponds to decimal address 40. The highest block address is 17FFH. This block has a decimal start address of 245720 and an end address 245759.

If a read or write reset operation is not performed, the next read or write pointer address after 245759 will be address 0 due to pointer wraparound. Note that reset read and reset write operations should occur in a single sequence. If one pointer wraps around while the other is reset, either 12 words will be lost or 12 words of undefined data will be read.

DATA INPUTS: D0 TO D11 AND WRITE CLOCK: SWCK

A positive transition on the SWCK write clock latches the data on inputs D0 to D11, provided WE was HIGH at the previous positive transition of SWCK. The data input set-up ($t_{su(D)}$) and hold ($t_{h(D)}$) times are referenced to the positive transition of SWCK (see Fig.4). The latched data will only be written into memory if IE was HIGH at the previous positive transition of SWCK.

WRITE ENABLE: WE

Pin WE is used to enable or disable a data write operation. The WE signal controls data inputs D0 to D11. In addition, the internal write address pointer is incremented if WE is HIGH at the positive transition of the SWCK write clock. WE set-up ($t_{su(WE)}$) and hold ($t_{h(WE)}$) times are referenced to the positive edge of SWCK (see Fig.7).

INPUT ENABLE: IE

Pin IE is used to enable or disable a data write operation from the D0 to D11 data inputs into memory. The latched data will only be written into memory if the IE and WE signals were HIGH during the previous positive transition of SWCK. A LOW level on IE will prevent the data being written into memory and existing data will not be overwritten (write mask function; see Fig.9). The IE set-up ($t_{su(IE)}$) and hold ($t_{h(IE)}$) times are referenced to the positive edge of SWCK (see Fig.8).

Read operation

Read operations are controlled by the SRCK, RSTR, RE and OE signals. A read operation starts with a reset read address pointer (RSTR) operation, followed by a sequence of SRCK clock cycles during which time RE and OE must be held HIGH. Read operations between two successive reset read operations must contain at least 20 SRCK read clock cycles while RE is HIGH.

RESET READ: RSTR

The first positive transition of SRCK after RSTR goes from LOW to HIGH resets the read address pointer to the lowest address (–12 decimal; see Figs 10 and 11). If RE is LOW, however, the reset read operation to the lowest address will be delayed until the first positive transition of SRCK after RE goes HIGH. RSTR set-up ($t_{su(RSTR)}$) and hold ($t_{h(RSTR)}$) times are referenced to the rising edge of SRCK (see Fig.10). The reset read operation may also be asynchronously related to the SRCK signal if RE is LOW.

RSTR needs to stay LOW for a single SRCK cycle before another reset read operation can take place.

RANDOM READ BLOCK ACCESS MODE

The SAA4955TJ will enter random read block access mode if the following signal sequence is applied to control inputs RE and OE during the first four SRCK read clock cycles after a reset read (see Fig.12):

At the 1st and 2nd positive transitions of SRCK, OE must be LOW and RE must be HIGH

At the 3rd and 4th positive transitions of SRCK, OE must be HIGH and RE must be LOW.

During this time, control signals RE and OE will function as defined for normal operation. The Most Significant Bit (MSB) of the block read address is applied to the OE input pin at the 5th positive transition of SRCK. The remaining 12 bits of the 13-bit read block address must be applied, in turn, to OE at the following 12 positive transitions of SRCK. The Least Significant Bit (LSB) of the block address is applied at the 17th positive transition of SRCK. A read latency period of 20 additional SRCK clock cycles is required before read access to the new block address is possible. During this period, data is transferred from the memory array to the serial read and parallel read registers and the read pointer is set to the new block address.

Block address values between 0 and 6143 are valid. Values outside this range must be avoided because invalid block addresses can result in abnormal operation or a lock-up condition. Recovery from lock-up requires a standard reset read operation.

The data output pins are not controlled by the OE pin and are forced into high impedance mode from the 3rd to the 17th positive transition of SRCK. OE should be held LOW during the read latency period. RE must remain LOW from the 3rd positive transition of SRCK to the 20th read latency SRCK clock cycle.

After the 20th read latency SRCK clock cycle, RE and OE may be switched HIGH to prepare for reading new data

from the new address block at the next positive transition of SRCK. The complete read block access entry sequence is finished after the 20th read latency cycle.

The LOW-to-HIGH transition on RSTR required at the beginning of the sequence should not be repeated. Additional LOW-to-HIGH transitions on RSTR would disable read block address mode and reset the read pointer.

DATA OUTPUTS: Q0 TO Q11 AND READ CLOCK: SRCK

The new data is shifted out of the data output registers on the rising edge of the SRCK read clock provided RE and OE are HIGH. Data output pins are low impedance if OE is HIGH. If OE is LOW, the data outputs are high impedance and the data output bus may be used by other devices. Data output hold ($t_{h(Q)}$) and access (t_{ACC}) times are referenced to the positive transition of SRCK. The output data becomes valid after access time interval t_{ACC} (see Fig.11).

Data output pins Q0 to Q11 are TTL compatible with the restriction that when the outputs are high impedance, they must not be forced higher than $V_{DD(O)}$ + 0.5 V or 5.0 V absolute. The output data has the same polarity as the incoming data at inputs D0 to D11.

READ ENABLE: RE

RE is used to increment the read pointer. Therefore, RE needs to be HIGH at the positive transition of SRCK. When RE is LOW, the read pointer is not incremented. RE set-up ($t_{su(RE)}$) and hold ($t_{h(RE)}$) times are referenced to the positive edge of SRCK (see Fig.13).

OUTPUT ENABLE: OE

OE is used to enable or disable data outputs Q0 to Q11. The data outputs are enabled (low impedance) if OE is HIGH. OE LOW disables the data output pins (high impedance). Incrementing of the read pointer does not depend on the status of OE. OE set-up ($t_{su(OE)}$) and hold ($t_{h(OE)}$) times are referenced to the positive edge of SRCK (see Fig.14).

Power-up and initialization

Reliable operation is not guaranteed until at least 100 μs after power-up, the time needed to stabilize V_{DD} within the recommended operating range. After the 100 μs power-up interval has elapsed, the following initialization sequence must be performed: a minimum of 12 dummy read operations (SRCK cycles) followed by a reset read operation (RSTR), and a minimum of 12 dummy write operations (SWCK) followed by a reset write operation (RSTW). Read and write initialization may be performed simultaneously.

If initialization starts earlier than the recommended 100 μs after power-up, the initialization sequence described above must be repeated, starting with an additional reset read operation and an additional reset write operation after the 100 μs start-up time.

Old and new data access

A minimum delay of 40 SWCK clock cycles is needed before newly written data can be read back from memory (see Fig.15). If a reset read operation (RSTR) occurs in a read cycle before a reset write operation (RSTW) in a write cycle accessing the same memory location, then old data will be read.

Old data will be read provided a data read cycle begins within 20 pointer positions of the start of a write cycle. This means that if a reset read operation begins within 20 SWCK clock cycles after a reset write operation, the internal buffering of the SAA4955TJ will ensure that old data will be read out (see Fig.16).

New data will be read if the read pointer is delayed by 40 pointer positions or more after the write pointer. Old data is still read out if the write pointer is less than or equal to 20 pointer positions ahead of the read pointer (internal buffering). A write pointer to read pointer delay of more than 20 but less than 40 pointer positions should be avoided. In this case, the old or the new data may be read, or a combination of both.

In random read and write block access modes, the minimum write-to-read new data delay of 40 SWCK clock cycles must be inserted for each block.

Memory arbitration logic and self-refresh

Since the data in the memory array is stored in DRAM cells, it needs to be refreshed periodically. Refresh is performed automatically under the control of internal memory arbitration logic which is clocked by a free running clock oscillator. The memory arbitration logic controls memory access for read, write and refresh operations. It uses the contents of the write, read and refresh address counters to access the memory array to load data from the parallel write register, store data in the parallel read register, or to refresh stored data. The values in these counters correspond to block addresses.

Cascade operation

If a longer delay is needed, the total storage depth can be increased beyond 2949264 bits by cascading several SAA4955TJs. For details see the interconnection and timing diagrams (Figs 17 and 18).

Test mode operation

The SAA4955TJ incorporates a test mode not intended for customer use. If WE and RSTW are held HIGH continuously for 1024 SWCK clock cycles, the SAA4955TJ will enter test mode. It will exit test mode if WE is LOW for a single SWCK cycle or if RSTW is LOW for 2 SWCK clock cycles.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}, $V_{DD(O)}$	supply voltages		–0.5	+5	V
$V_{DD(P)}$	supply voltage for protection circuits		–0.5	+5.5	V
V_I	input voltage	$V_{DD(P)}$ = 5 V	–0.5	+5.5	V
		$V_{DD} = V_{DD(O)} = V_{DD(P)}$ = 3.3 V	–0.5	+3.8	V
V_O	output voltage	$V_{DD(P)}$ = 5 V	–0.5	+5	V
		$V_{DD} = V_{DD(O)} = V_{DD(P)}$ = 3.3 V	–0.5	+3.8	V
$I_{DD(tot)}$	total supply current		–	200	mA
ΔV	voltage difference between GND, GND_O and GND_P		–0.5	+0.5	V
I_O	short circuit output current		–	50	mA
P_{tot}	total power dissipation		–	750	mW
T_{stg}	storage temperature		–20	+150	°C
T_j	junction temperature		0	125	°C
T_{amb}	ambient temperature		0	70	°C
V_{es}	electrostatic handling	note 1	–150	+200	V
		note 2	–2000	+2000	V

Notes

1. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (‘0 Ω’ is actually 0.75 μH + 10 Ω).
2. Human body model: equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

CHARACTERISTICS

V_{DD} = $V_{DD(O)}$ = $V_{DD(P)}$ = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; 3 ns input transition times; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}, $V_{DD(O)}$	supply voltages (pins 19 and 22)		3.0	3.3	3.6	V
$V_{DD(P)}$	supply voltage (pins 20 and 21)		3.0	3.3	5.5	V
$I_{DD(tot)}$	total supply current ($I_{DD(tot)}$ = I_{DD} + $I_{DD(O)}$ + $I_{DD(P)}$)	minimum write/read cycle; outputs open	–	22	70	mA
I_{DD}	operating supply current	minimum write/read cycle	–	20	60	mA
I_{DDstd}	stand-by supply current	after 1 RSTW/RSTR cycle; WE, RE and OE LOW	–	3	10	mA
$I_{DD(O)}$	supply current	minimum write/read cycle; outputs open	–	2	10	mA
$I_{DD(P)}$	supply current		–	0	1	mA
Inputs (pins 3 to 18 and 23 to 26)						
V_{IH}	HIGH-level input voltage		2.0	–	$V_{DD(P)}$ + 0.3	V
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
I_{LI}	input leakage current	V_I = 0 V to $V_{DD(P)}$	–10	–	+10	µA
C_i	input capacitance	f = 1 MHz; V_I = 0 V	–	–	7	pF
Outputs (pins 27 to 38)						
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.2 mA	–	–	0.4	V
I_{LO}	output leakage current	V_O = 0 V to $V_{DD(Q)}$; RE and OE LOW	–10	–	+10	µA
C_o	output capacitance	f = 1 MHz; V_O = 0 V	–	–	10	pF
Write cycle timing; note 2						
$T_{cy(SWCK)}$	SWCK cycle time	see Fig.3	26	–	–	ns
$t_{W(SWCKH)}$	SWCK HIGH pulse width	see Fig.3	7	–	–	ns
$t_{W(SWCKL)}$	SWCK LOW pulse width	see Fig.3	7	–	–	ns
$t_{su(D)}$	set-up time data inputs (D0 to D11)	see Fig.3	5	–	–	ns
$t_{h(D)}$	hold time data inputs (D0 to D11)	see Fig.3	3	–	–	ns
$t_{su(RSTW)}$	set-up time RSTW	see Fig.3	5	–	–	ns
$t_{h(RSTW)}$	hold time RSTW	see Fig.3	3	–	–	ns
$t_{su(WE)}$	set-up time WE	see Fig.7	5	–	–	ns
$t_{h(WE)}$	hold time WE	see Fig.7	3	–	–	ns
$t_{W(WEL)}$	WE LOW pulse width	see Fig.7	8	–	–	ns
$t_{su(IE)}$	set-up time IE	see Fig.8	5	–	–	ns
$t_{h(IE)}$	hold time IE	see Fig.8	3	–	–	ns
$t_{W(IEL)}$	IE LOW pulse width	see Fig.8	8	–	–	ns
t_t	transition time (rise and fall)	see Fig.3	–	3	30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Read cycle timing; note 3						
t_{ACC}	access time after SRCK	see Fig.10	–	–	21	ns
$t_{en(Q)}$	output enable time after SRCK	see Fig.14	–	–	21	ns
$t_{dis(Q)}$	output disable time after SRCK	note 4; see Fig.14	–	–	12	ns
$t_{h(Q)}$	output hold time after SRCK	see Fig.10	3	–	–	ns
$T_{cy(SRCK)}$	SRCK cycle time	see Fig.10	26	–	–	ns
$t_{W(SRCKH)}$	HIGH-level pulse width of SRCK	see Fig.10	7	–	–	ns
$t_{W(SRCKL)}$	LOW-level pulse width of SRCK	see Fig.10	7	–	–	ns
$t_{su(RSTR)}$	set-up time RSTR	see Fig.10	5	–	–	ns
$t_{h(RSTR)}$	hold time RSTR	see Fig.10	3	–	–	ns
$t_{su(RE)}$	set-up time RE	see Fig.13	5	–	–	ns
$t_{h(RE)}$	hold time RE	see Fig.13	3	–	–	ns
$t_{W(REL)}$	LOW-level pulse width of RE	see Fig.13	9	–	–	ns
$t_{su(OE)}$	set-up time OE	see Fig.14	5	–	–	ns
$t_{h(OE)}$	hold time OE	see Fig.14	3	–	–	ns
$t_{W(OEL)}$	LOW-level pulse width of OE	see Fig.14	9	–	–	ns
t_t	transition time (rise and fall)	see Fig.10	–	3	30	ns

Notes

1. Typical values are valid for T_{amb} = 25 °C, $V_{DD} = V_{DD(O)} = V_{DD(P)}$ = 3.3 V, all voltages referenced to GND. See Fig.1 for configuration.
2. The write cycle timing set-up and hold times are related to V_{IL} of the rising edge of SWCK. They are valid for the specified LOW- and HIGH-level input voltages (V_{IL} and V_{IH}).
3. The read cycle timing set-up and hold times are related to V_{IL} of the rising edge of SRCK. They are valid for the specified LOW- and HIGH-level input voltages (V_{IL} and V_{IH}). The load on each output is a 30 pF capacitor to ground in parallel with a 218 Ω resistor to 1.31 V.
4. Disable times specified are from the initiating edge until the output is no longer driven by the memory. Disable times are measured by observing the output waveforms. Low values of load resistor and capacitor have to be used to obtain a short time constant.

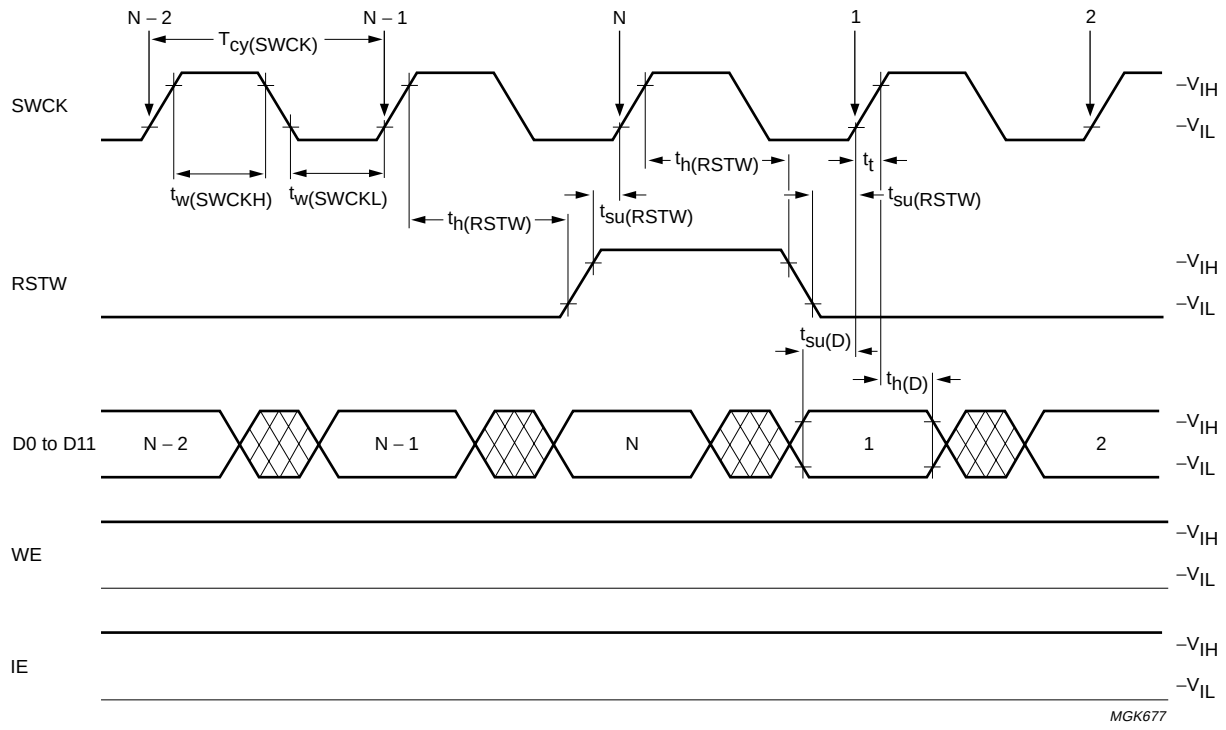


Fig.3 Write cycle timing diagram (reset write).

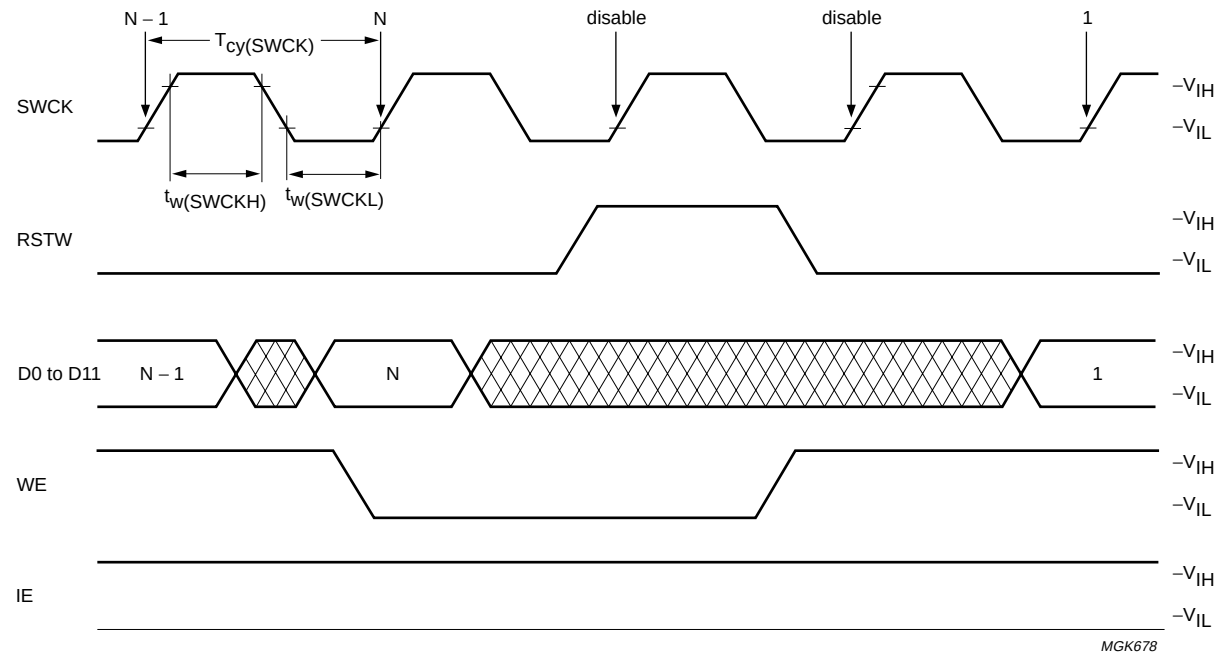


Fig.4 Write cycle timing diagram (reset write with WE LOW).

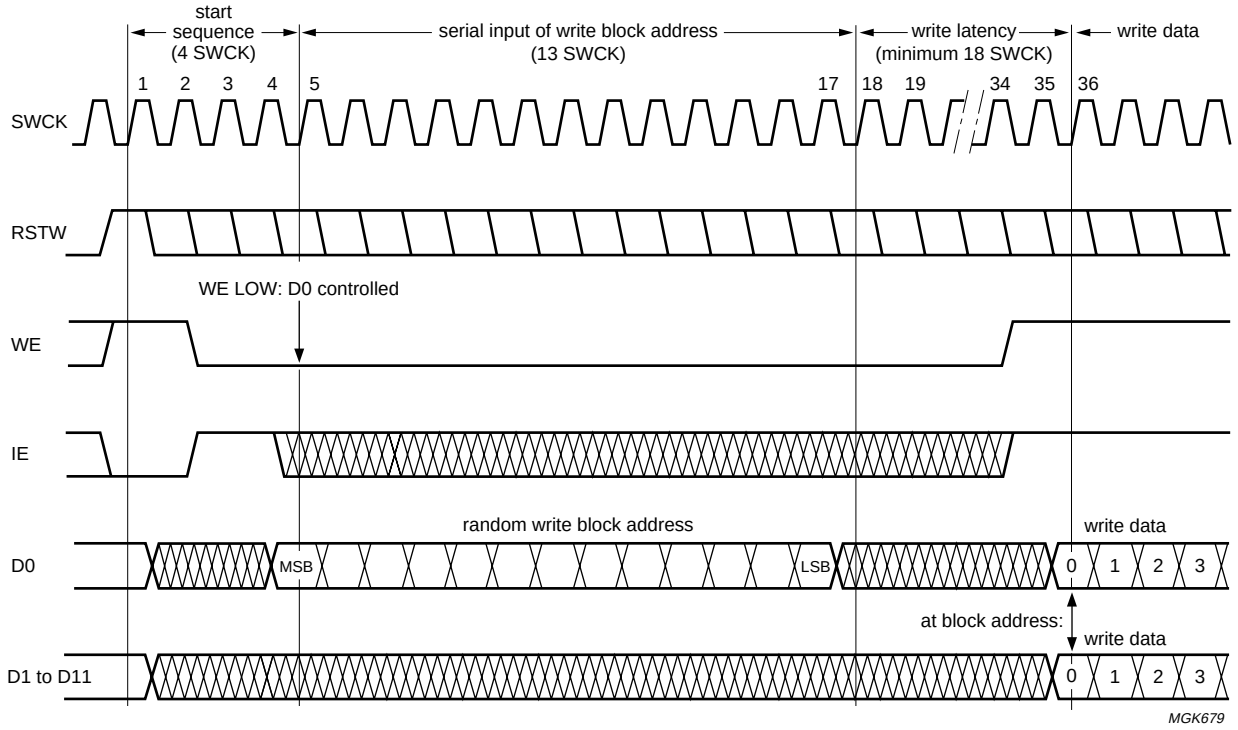


Fig.5 D0 controlled entry sequence of random write block access mode.

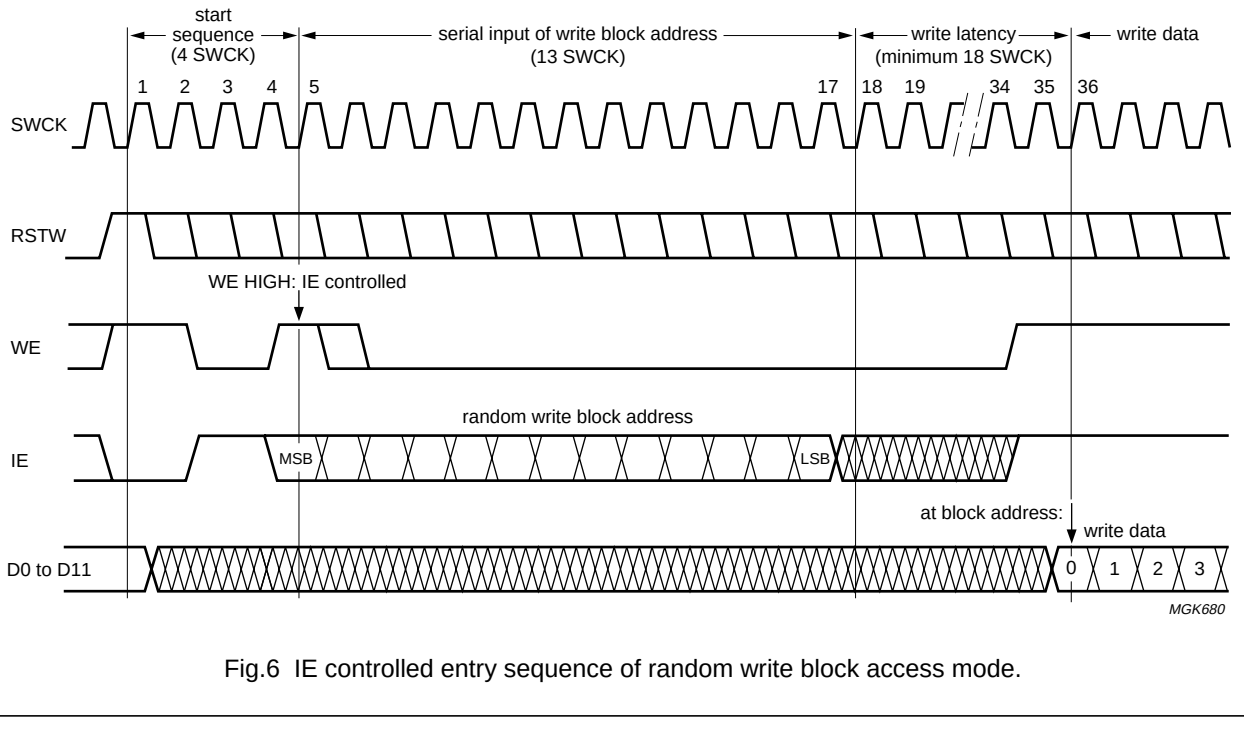


Fig.6 IE controlled entry sequence of random write block access mode.

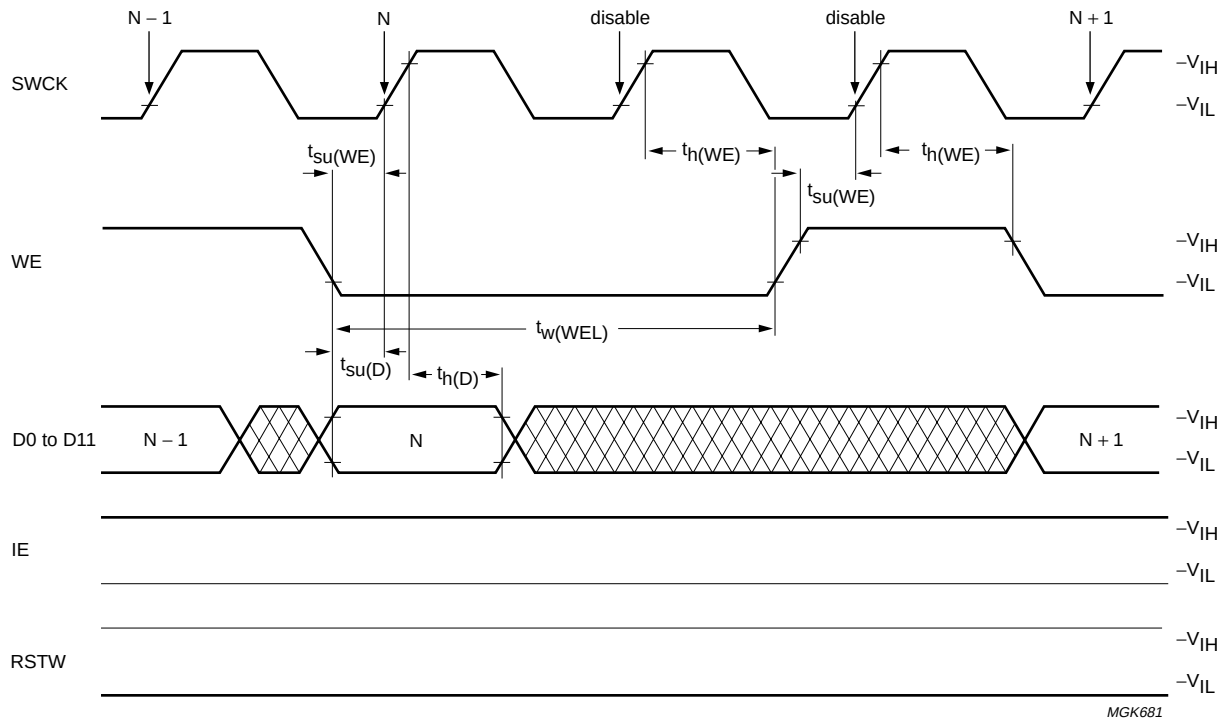


Fig.7 Write cycle timing diagram (write enable).

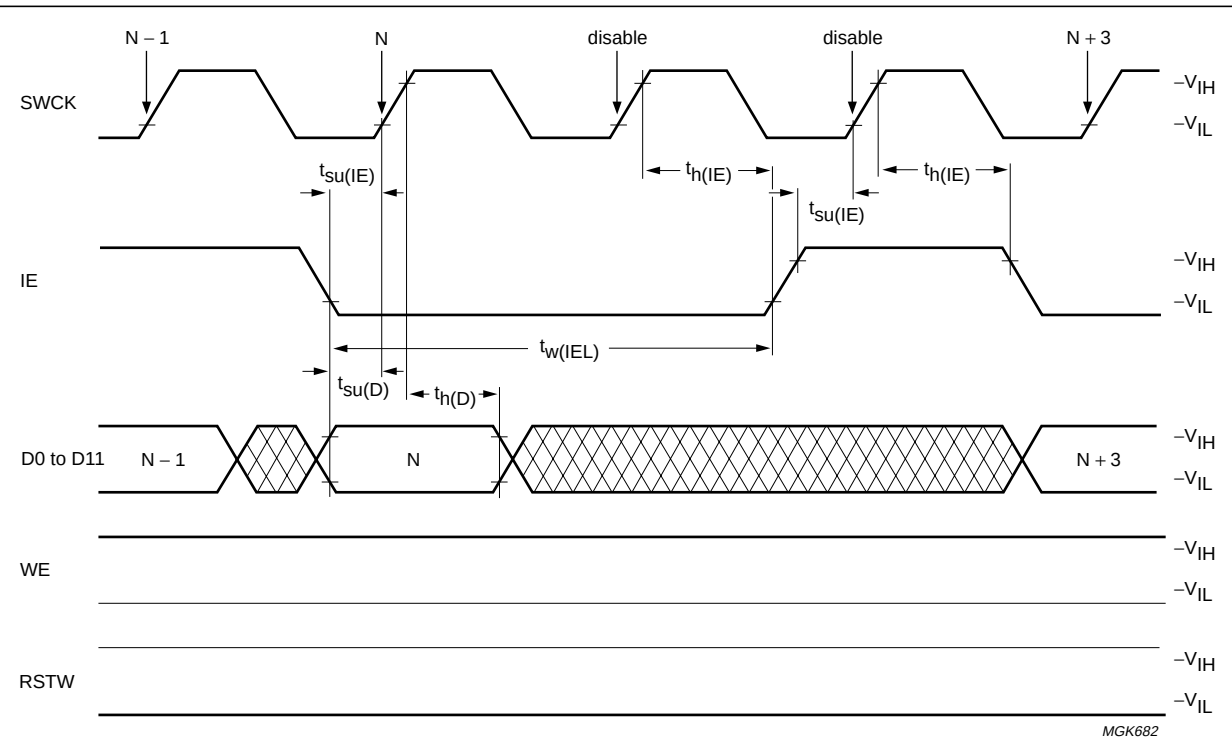


Fig.8 Write cycle timing diagram (input enable = write mask operation).

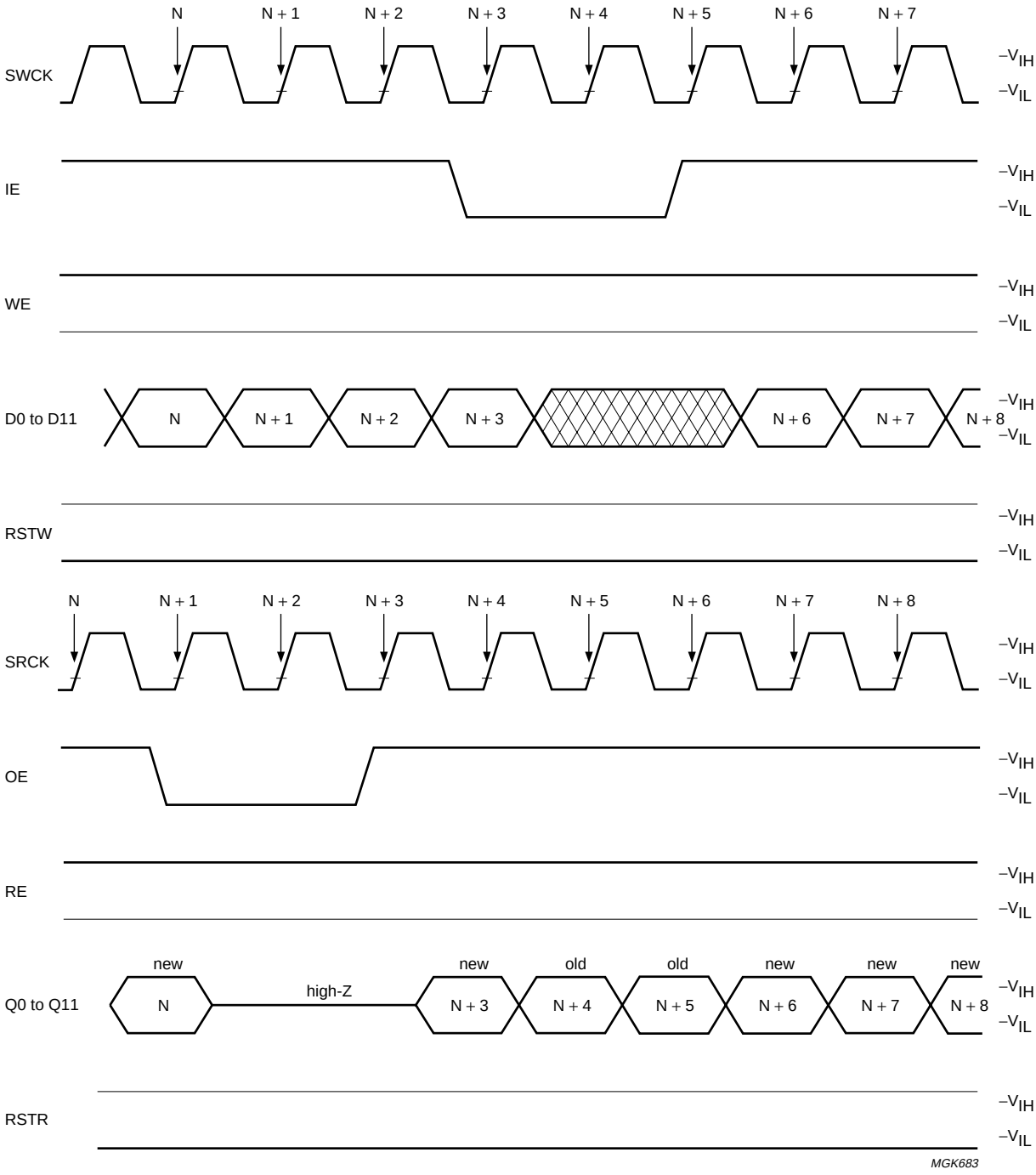


Fig.9 Write mask operation.

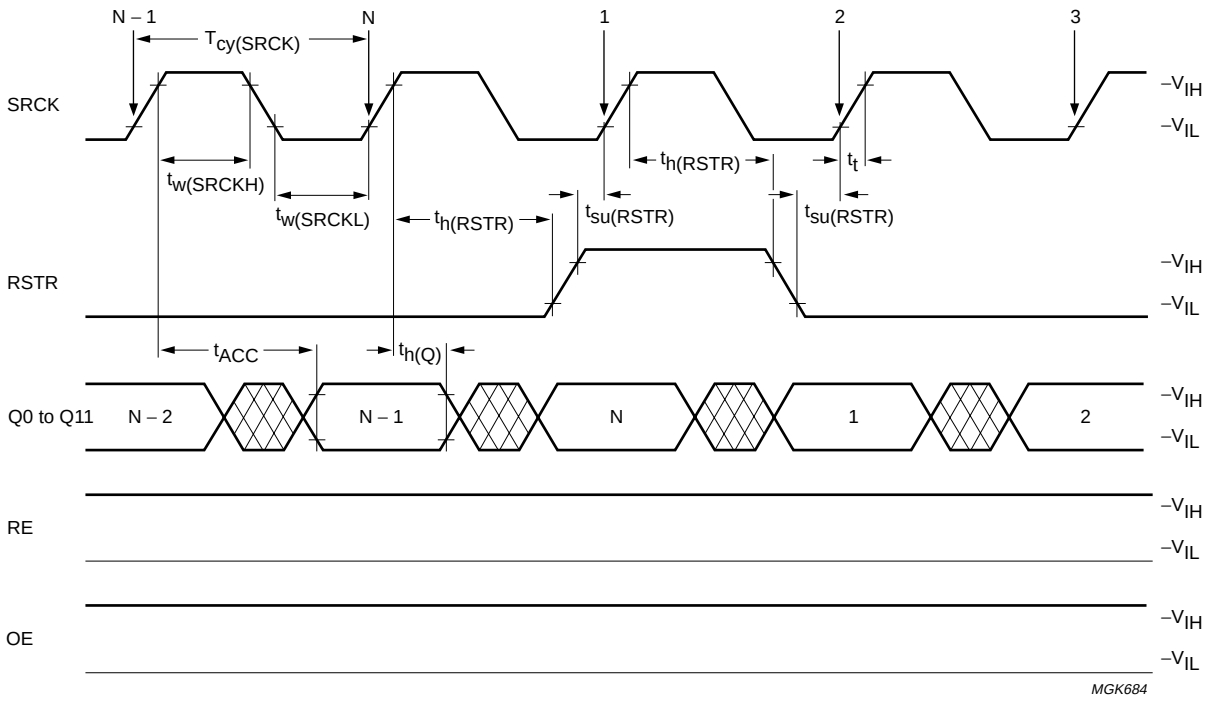


Fig.10 Read cycle timing diagram (reset read).

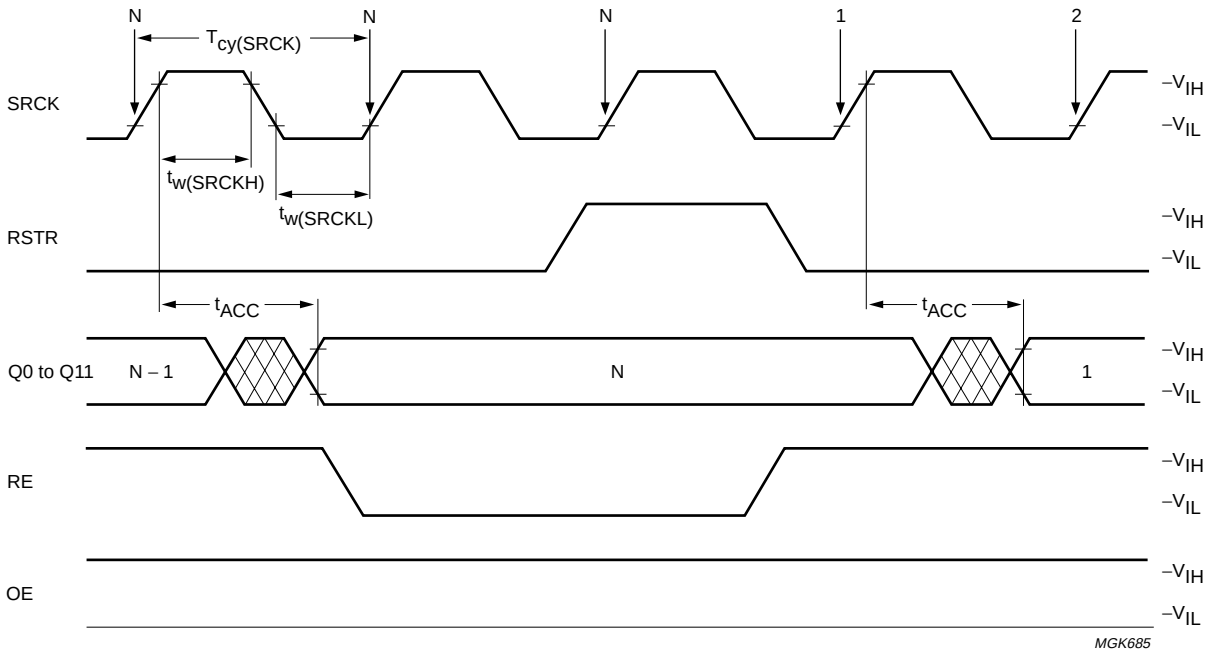


Fig.11 Read cycle timing diagram (reset read with RE LOW).

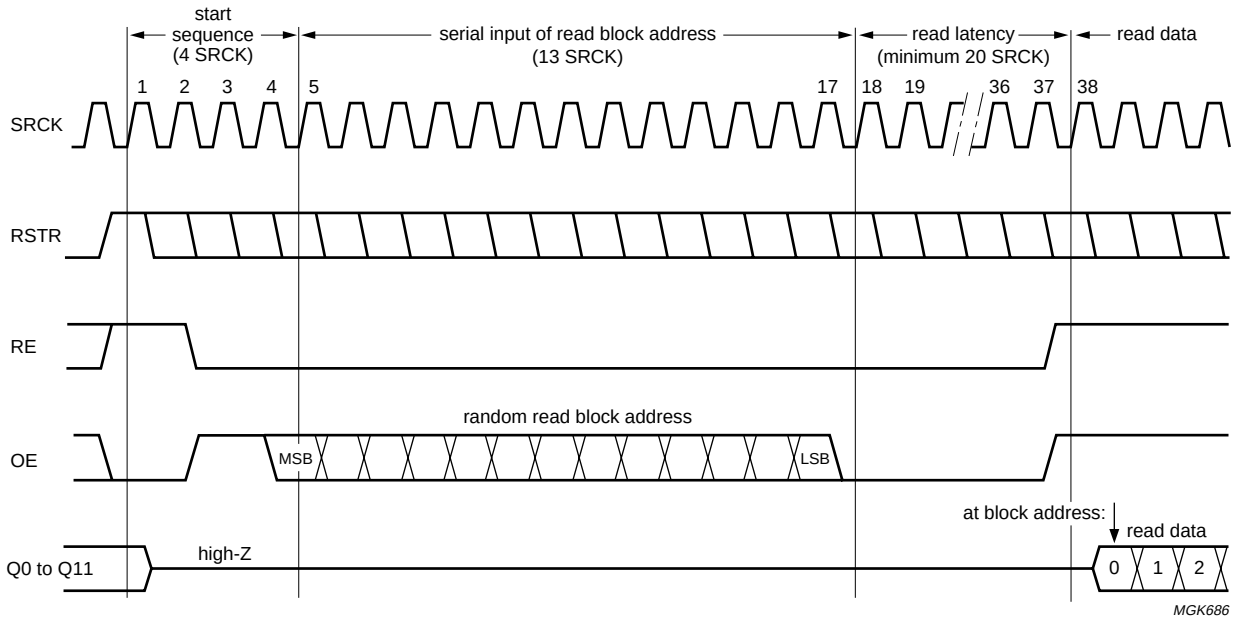


Fig.12 Entry sequence of random read block access mode.

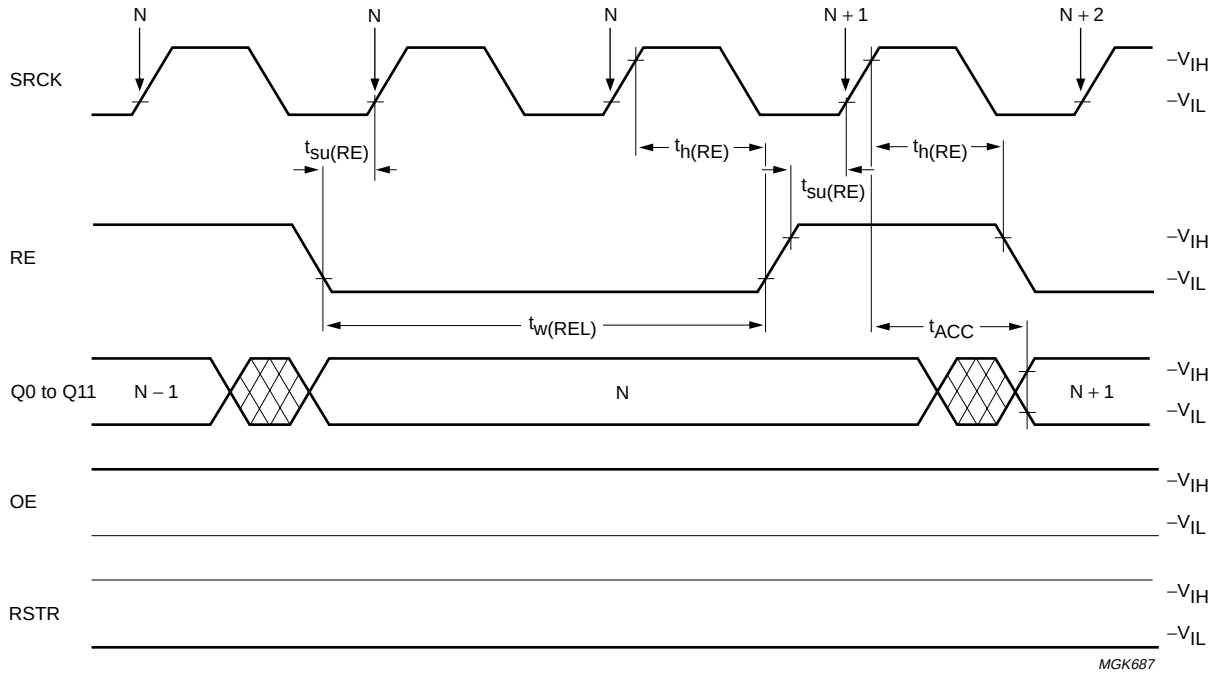


Fig.13 Read cycle timing diagram (read enable).

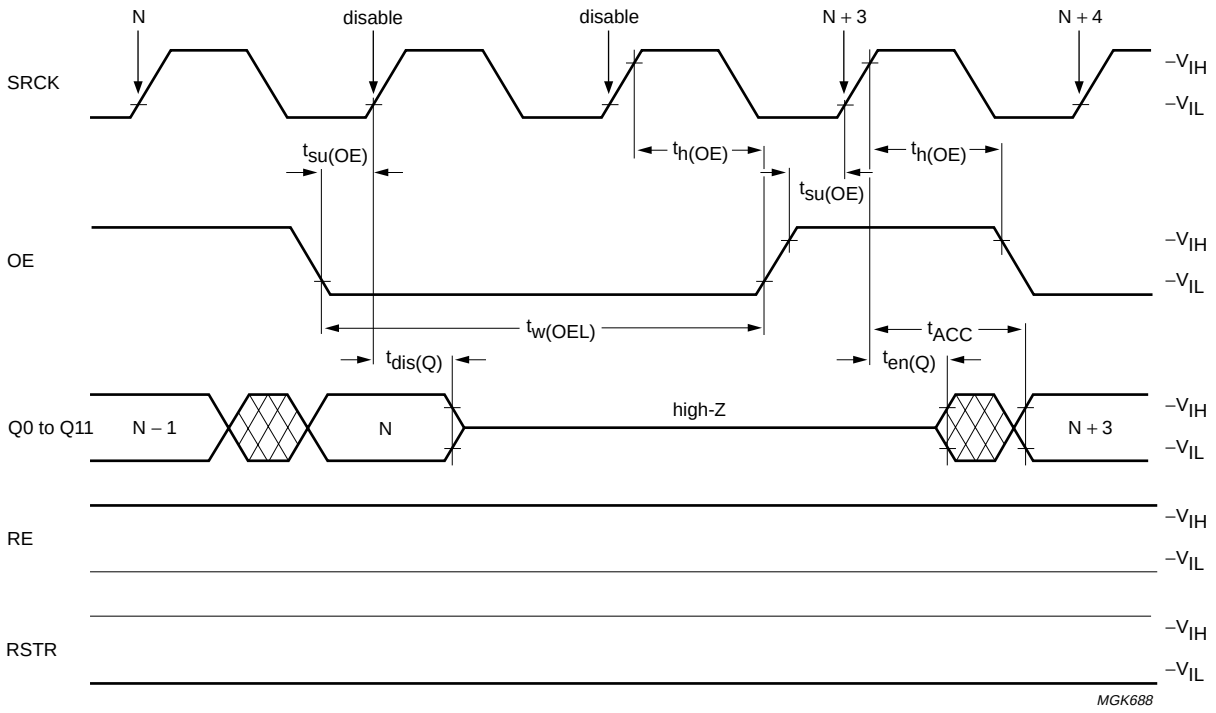


Fig.14 Read cycle timing diagram (output enable).

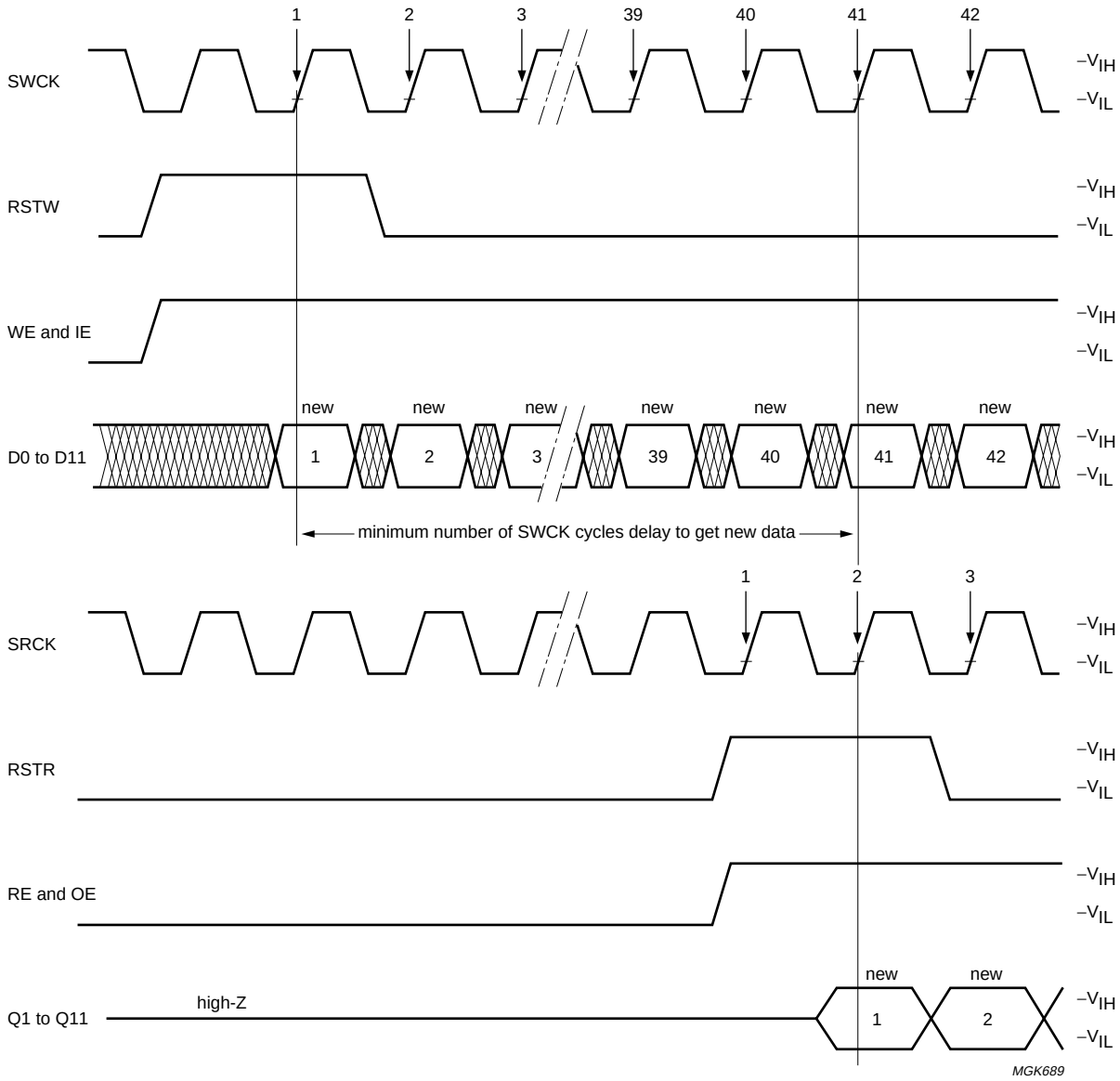


Fig.15 New data access.

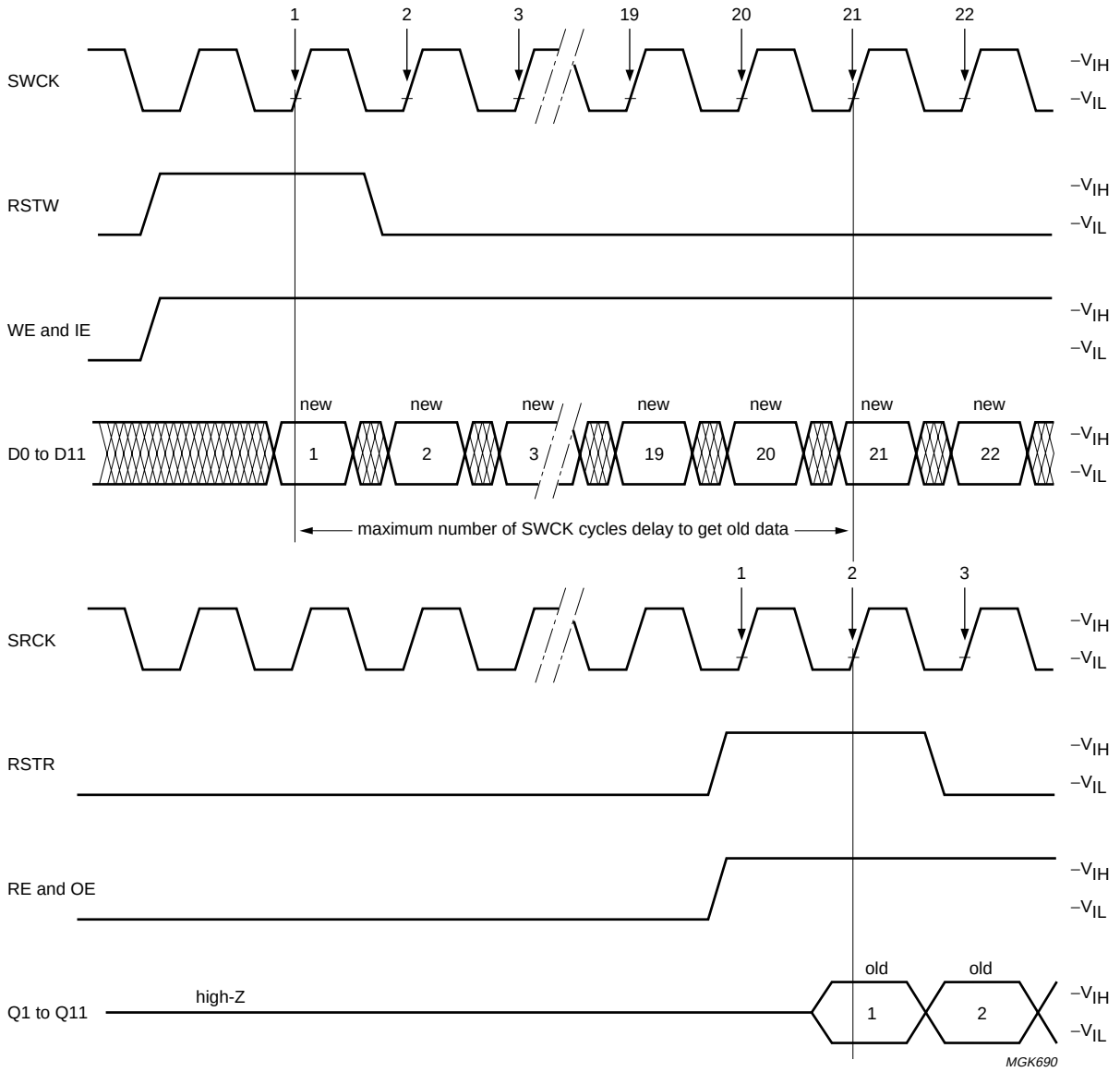


Fig.16 Old data access.

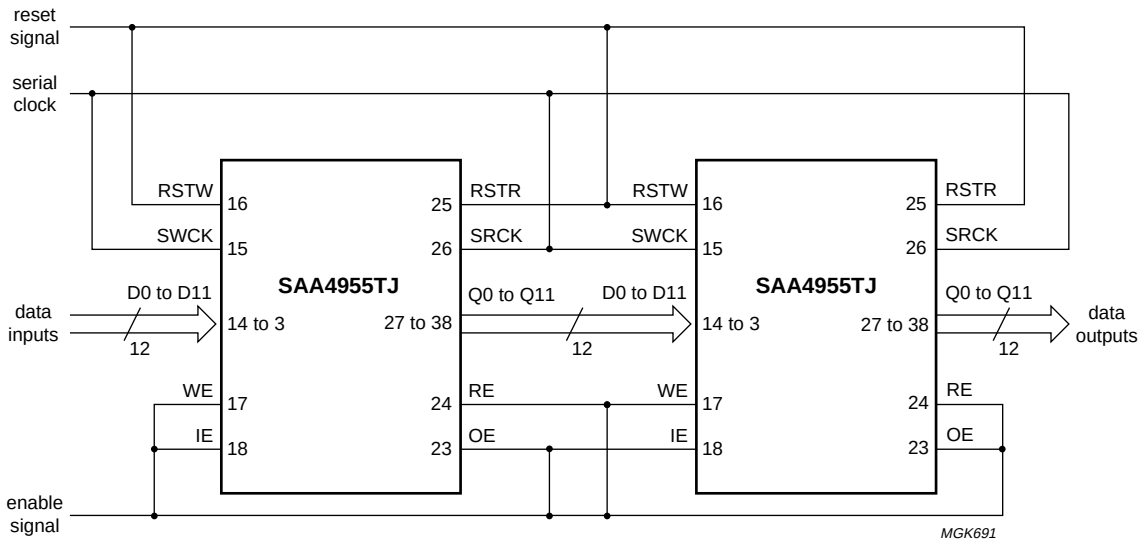


Fig.17 Cascade operation (signal connections).

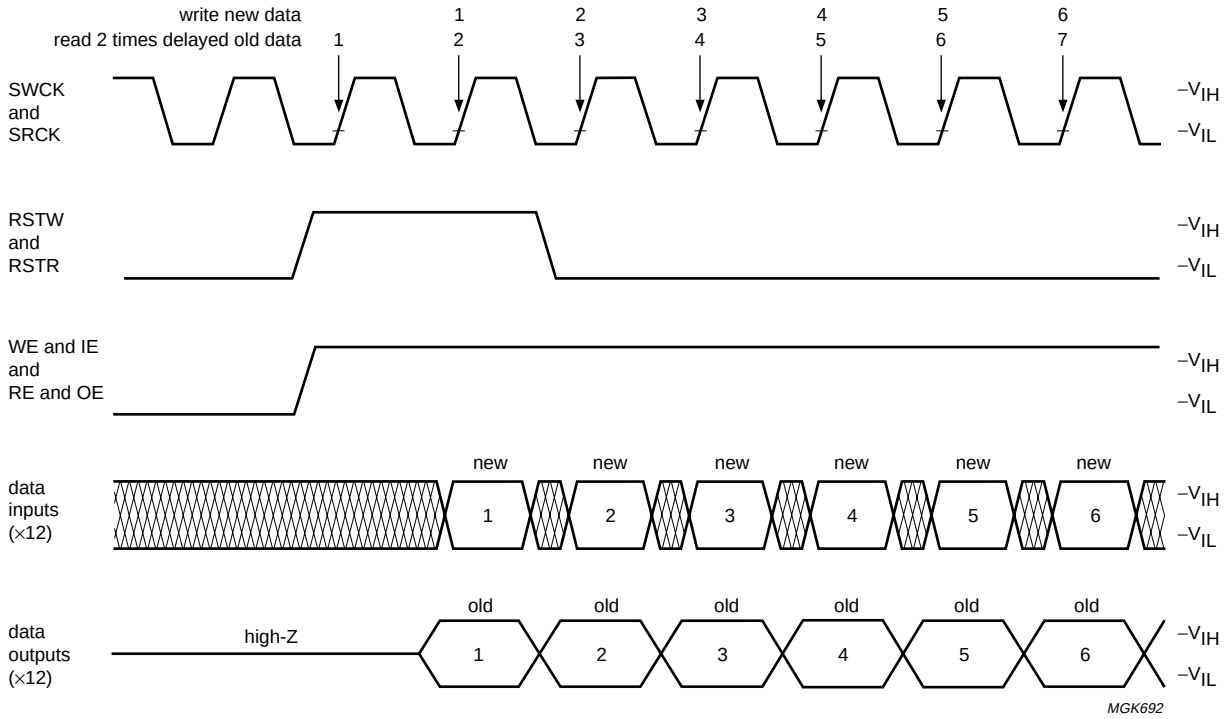
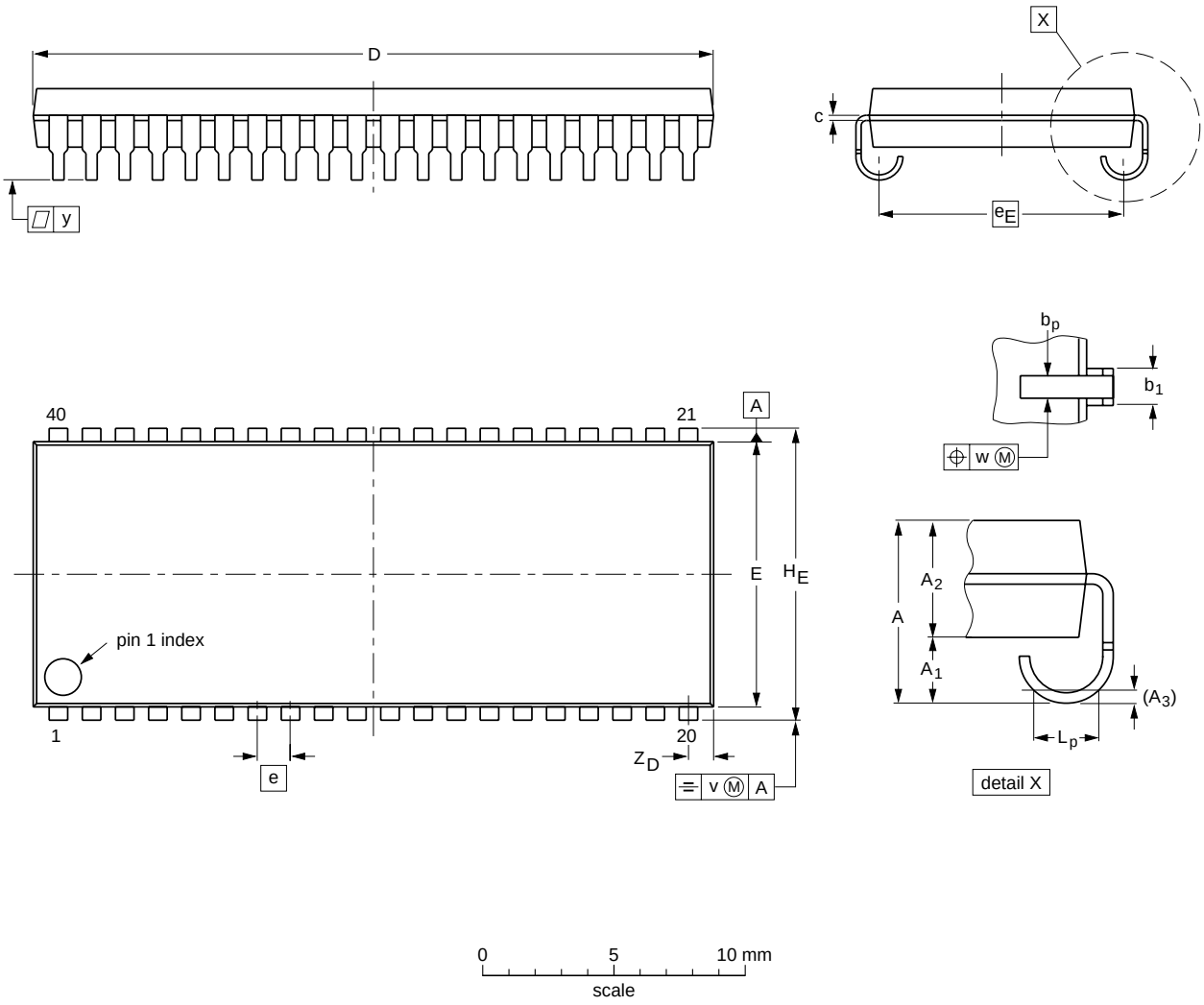


Fig.18 Cascade operation (timing waveforms).

PACKAGE OUTLINE

SOJ40: plastic small outline package; 40 leads (J-bent); body width 10.16 mm **SOT449-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_E	H_E	L_p	v	w	y	$Z_D^{(1)}$
mm	3.68	1.40 1.14	2.29 2.18	0.25	0.51 0.38	0.81 0.66	0.32 0.18	26.2 25.9	10.3 10.0	1.27	9.4	11.30 11.05	1.4 1.1	0.18	0.18	0.1	1.19 0.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT449-1		MS027				97-06-02

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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