2A Low-Dropout Regulator with Enable

DESCRIPTION

The EUP7966 is a high current, fast response voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 2 amps. It operates from two input voltages : VBIAS provides 5V voltage to drive the gate of the N-MOS power transistor, while VIN is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low VIN voltage. The EUP7966 features ultra low dropout, ideal for applications where VOUT is very close to VIN.

Additionally, the EUP7966 has an enable pin to further reduce power dissipation while shutdown. The EUP7966 provides excellent regulation over variations in line, load and temperature. The EUP7966 provides a power OK signal to indicate if the voltage level of VOUT reaches 92% of its rating value.
The EUP7966 is available in the power SOP-8 (FD) package. It is available with 1.2V, 1.5V, 1.8V and 2.5V internally preset outputs, that are also be able to programmed as low as 0.8V with ADJ pin configured with external resistors.

FEATURES

- Input Voltage as Low as 1.2V and VBIAS Voltage 5V
- ± 2% Output Voltage
- 300mV Dropout @ 2A, VOUT=1.2V
- Over Current and Over Temperature Protection
- Enable Pin
- Low Reverse Leakage (Output to Input)
- Power OK Output
- 1.2V, 1.5V, 1.8V and 2.5V Standard Voltages
  Available and Each also can be Adjustable by Connecting ADJ with External Resistors
- SOP-8 (FD) Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Motherboards
- Peripheral Cards
- Network cards
- Set Top Boxes
- Notebook Computers

Typical Application Circuit

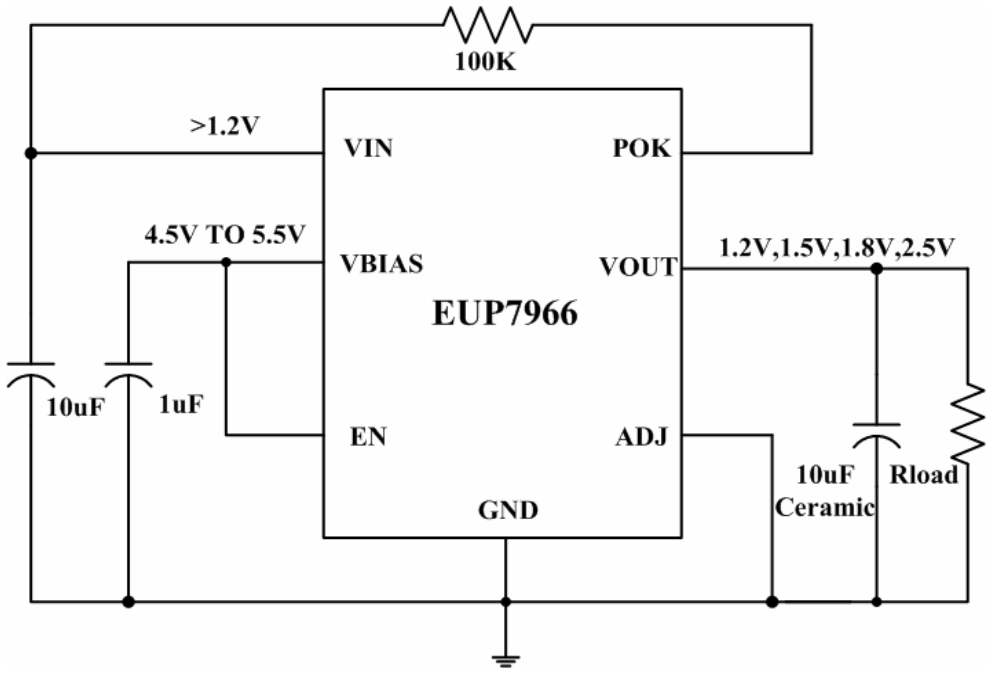


Figure 1. Fixed Output Voltage

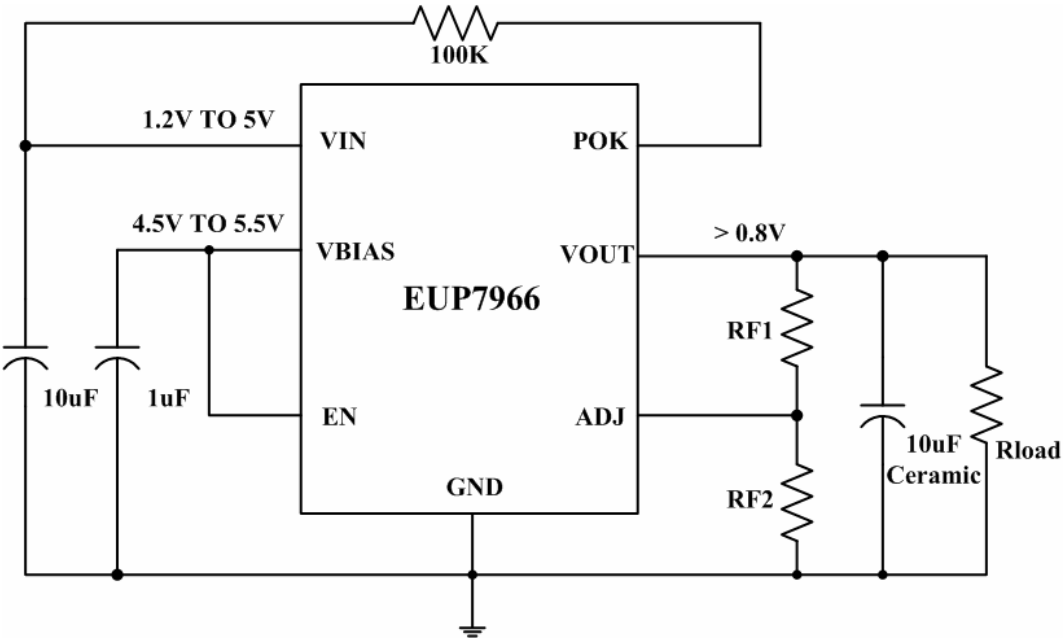


Figure 2. Adjustable Output Voltage

Block Diagram

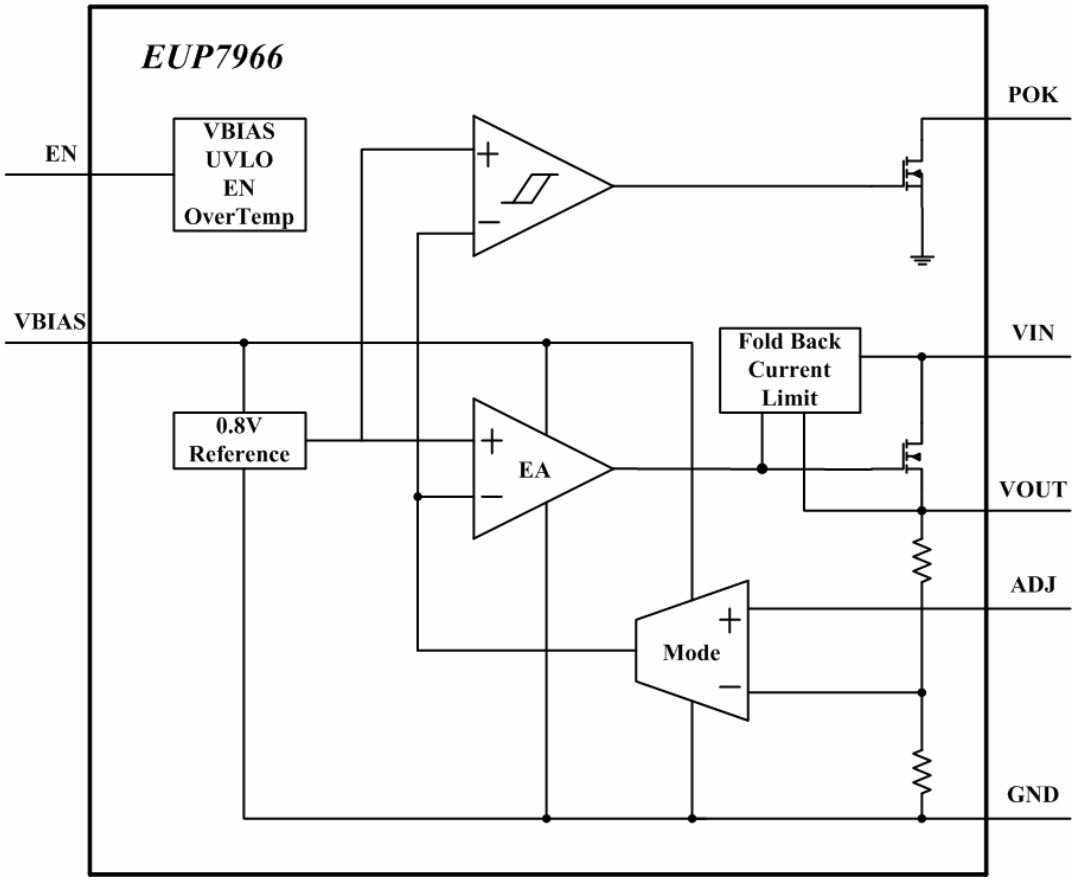
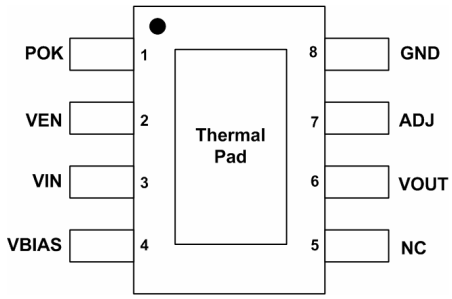


Figure 3.

Pin Configurations

Part Number	Pin Configurations
EUP7966 SOP-8 (FD)	

Pin Description

PIN	SOP-8	DESCRIPTION
POK	1	Assert high once VOUT reaches 92% of its rating voltage. Open-drain output.
VEN	2	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open.
VIN	3	High current input voltage. Large bulk capacitance should be placed closely to this pin . A 10μF ceramic capacitor is recommended at this pin.
VBIAS	4	Input voltage for controlling circuit.
NC	5	Not connected.
VOUT	6	The power output of the device. A pull low resistance exists when deactivate device by VEN.
ADJ	7	This pin, when grounded, sets the output voltage by the internal feedback resistors. If external feedback resistors are used , the output voltage will be VOUT=0.8(R1+R2)/R2 Volts.
GND	8	Reference ground.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUP7966-12DIR1	SOP-8 (FD)	xxxx EUP7966 T	-40 °C to 85°C
EUP7966-15DIR1	SOP-8 (FD)	xxxx EUP7966 C	-40 °C to 85°C
EUP7966-18DIR1	SOP-8 (FD)	xxxx EUP7966 D	-40 °C to 85°C
EUP7966-25DIR1	SOP-8 (FD)	xxxx EUP7966 B	-40 °C to 85°C

EUP7966-□□□ □ □ □ □

Lead Free Code

1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
D: SOP (FD)

Output Voltage
12: 1.2V
15: 1.5V
18: 1.8V
25: 2.5V

Absolute Maximum Ratings

- V_{BIAS},V_{IN} ,Input Voltage ---------- 6V
- Junction Temperature ---------- 150°C
- Storage Temperature ---------- -65°C to +150°C
- Power Dissipation ---------- Internal Limiting
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Thermal Resistance θ_{JA}, SOP-8 (FD) ---------- 42.3°C/W
- ESD Rating
  Human Body Model ---------- 1kV

Operating Ratings

- V_{IN} Voltage ---------- 1.2 to 3.6V
- V_{PP} Voltage ---------- 4.5 to 5.5V
- Temperature Range ---------- $-40°C \le T_A \le 85°C$

Electrical Characteristics

V_{BIAS}= 5V, $V_{IN}=V_{OUT}$+0.5V, I_O=10mA,$C_{IN}=C_{OUT}$=10µF, C_{BIAS}=1µF ,$T_A=T_J$= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	EUP7966			Unit
			Min	Typ	Max.	
V_{IN}	Input Voltage Range		1.2	--	3.6	V
I_Q	Quiescent Current (Ground Current)	$V_{IN}=V_{OUT}$+0.5V,I_O=10mA	--	1	1.6	mA
		$V_{IN}=V_{OUT}$+3.6V,I_O=100mA	--	1.1	2.5	
I_{SD}	Shutdown Current	V_{EN}=0V,V_{IN}=2.2V	--	0.1	1	µA
		V_{EN}=0V,V_{IN}=3.6V	--	0.4	5	
V_{BIAS}	V_{BIAS} Voltage Range		4.2	--	5.5	V
I_{BH}	V_{BIAS} Current	V_{OUT}=1.2V	--	0.8	1.2	mA
I_{BL}		V_{EN}=0V	--	--	1	µA
V_{OUT}	Output Voltage Accuracy (Fixed)		-2	--	2	%
		T_A=-40 to 85℃	-3	--	3	
	Line Regulation	V_{IN}=(V_{OUT}+0.5V) to 5V, T_A=-40 to 85℃	--	0.2	1	%
	Load Regulation	$10mA \le Io \le 1A$	--	3.5	10	mV
V_{DROP}	Dropout Voltage	Io=0.1A	--	10	15	
		Io=2A	--	200	300	mV
I_{SC}	Short Circuit Current	V_O=GND	--	2	--	A
	V_{OUT} Pull Low Resistance	V_{EN}=0V	--	75	--	Ω
ADJ						
V_{REF}	Reference Voltage	$V_{ADJ}=V_{0UT}$	0.792	0.804	0.816	V
	Adjust Pin Current		--	--	1	µA
	Adjust Pin Threshold		0.17	0.22	0.27	V

Electrical Characteristics

V_{BIAS}= 5V, V_{IN}=V_{OUT}+0.5V, I_O=10mA,C_{IN}=C_{OUT}=10µF, C_{BIAS}=1µF ,T_A =T_J= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	EUP7966			Unit
			Min	Typ	Max.	
VEN						
V_{ENH}	V_{EN} Pin Voltage High	T_A=-40 to 85℃	1.6	--	--	V
E_{ENL}	V_{EN} Pin Voltage Low	T_A=-40 to 85℃	--	--	0.4	V
	V_{EN} Pin Bias Current	V_{EN}=0V	--	--	1	µA
POK						
V_{THPOK}	V_{OUT} Power OK Voltage		--	90	--	%
V_{HYPOK}	Hysteresis		--	7.5	--	%
Over Temperature Protection (OTP)						
T_{OT}	Over Temperature		--	155	--	℃
T_{OTHY}	Over Temperature Hysteresis		--	30	--	℃
Under Voltage Lock Out (UVLO)						
	Vbias Thereshold		--	3.9	--	V
	Hysteresis		--	20	--	mV

Typical Operating Characteristics

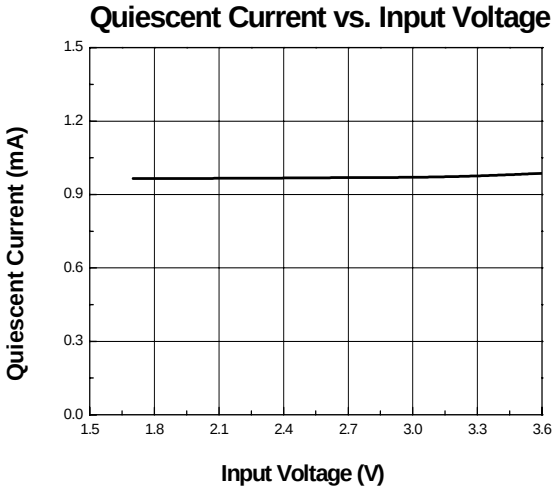


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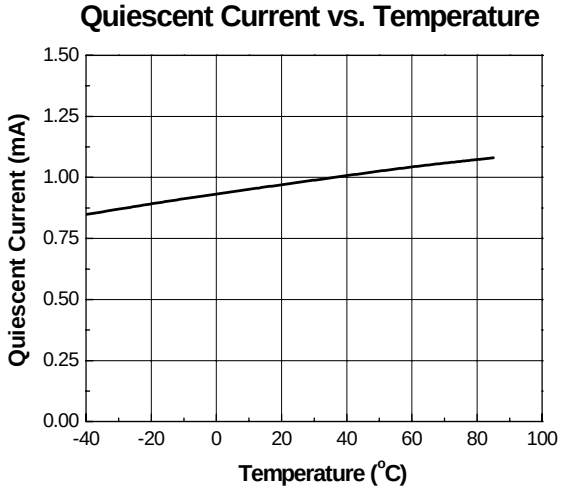


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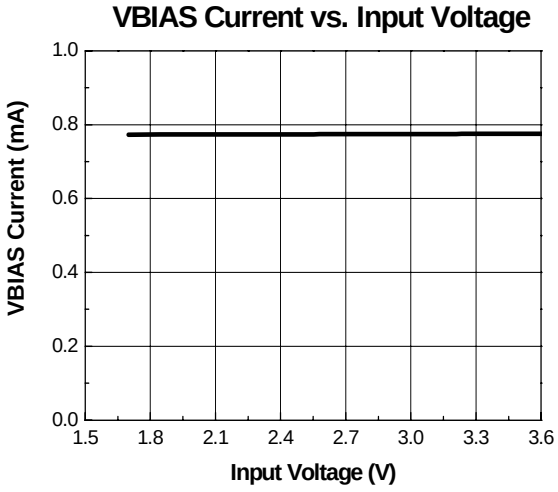


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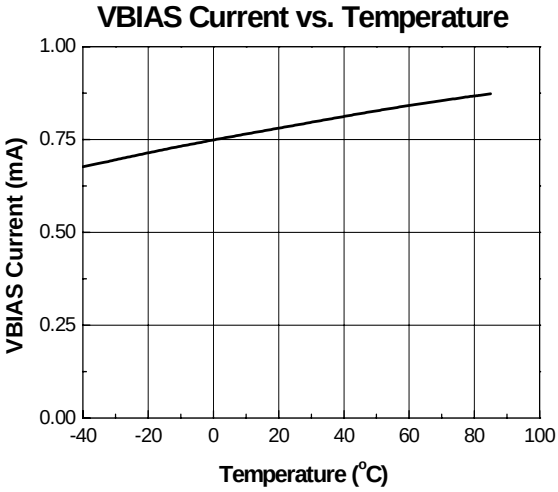


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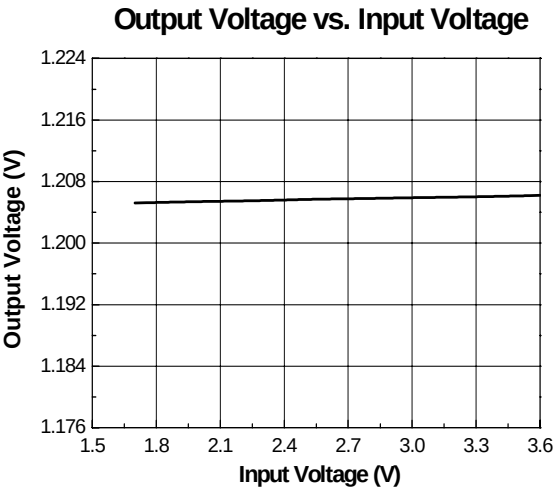


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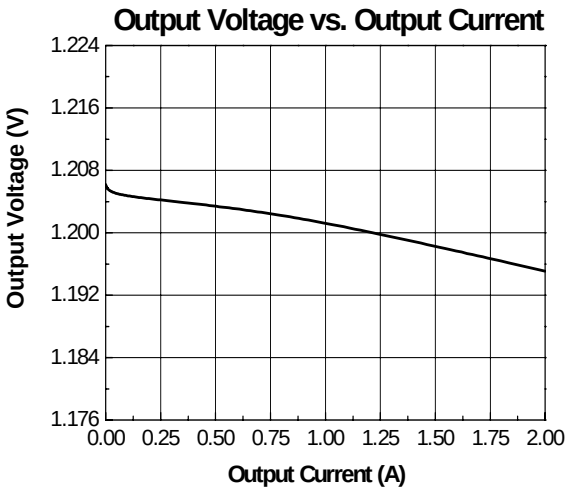


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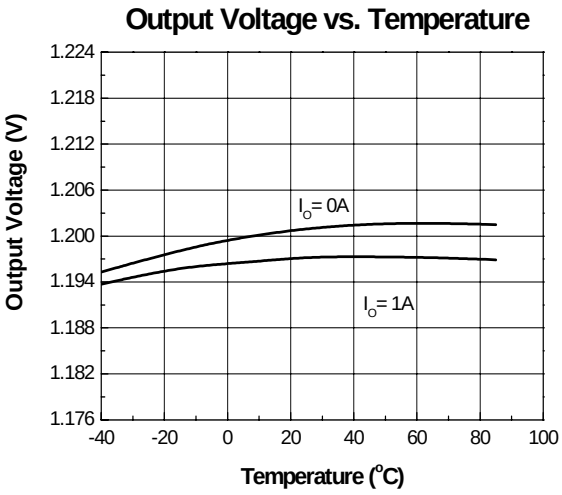


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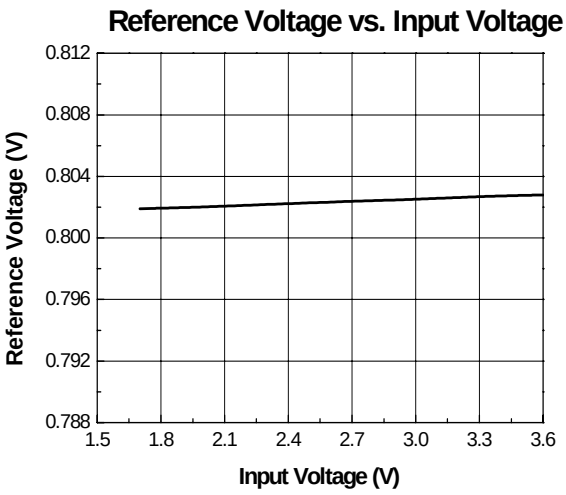


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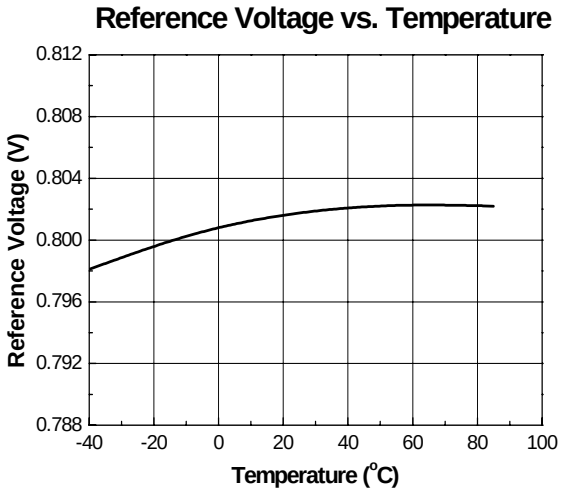


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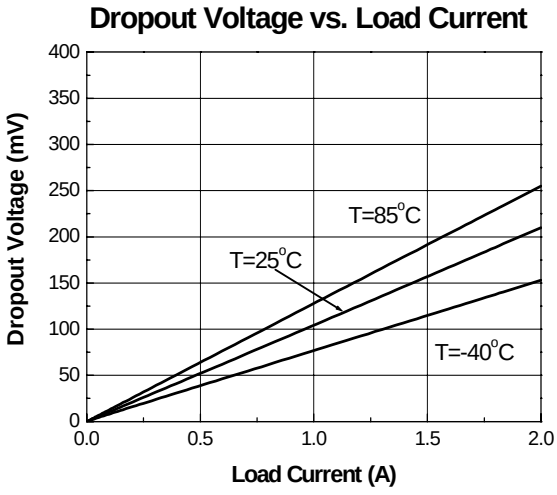


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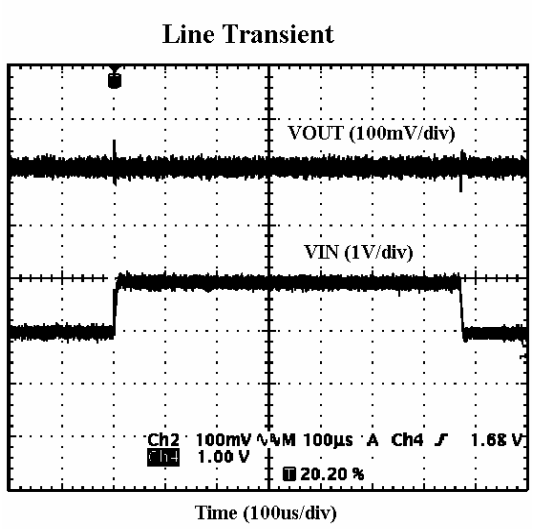


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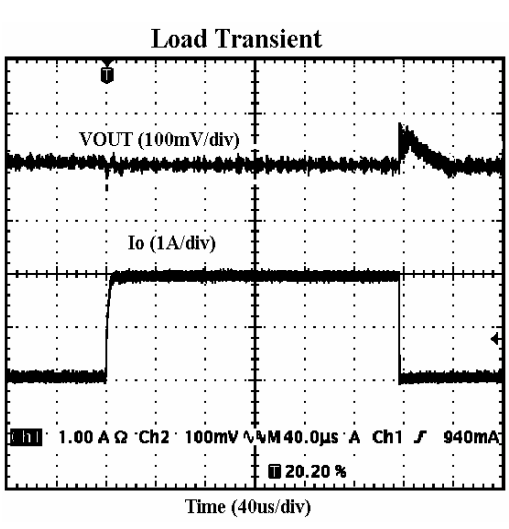


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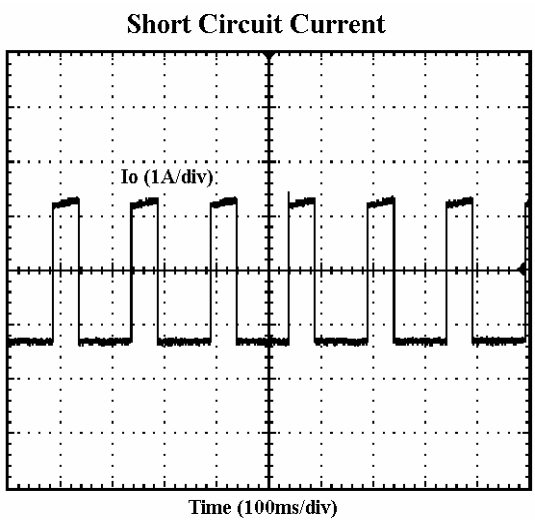


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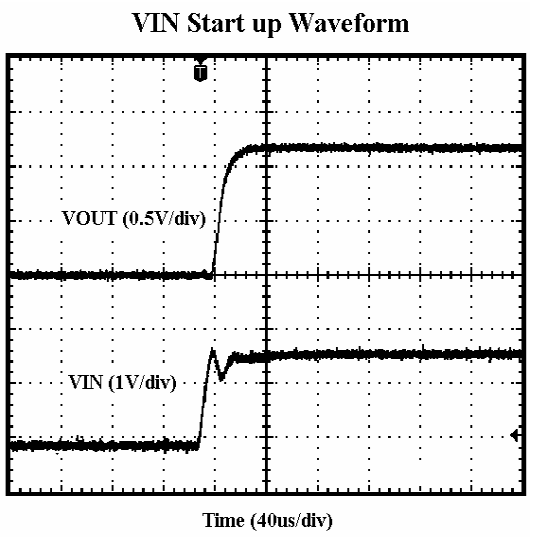


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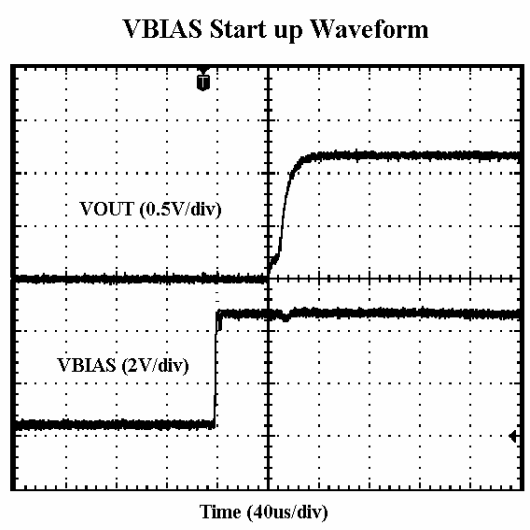


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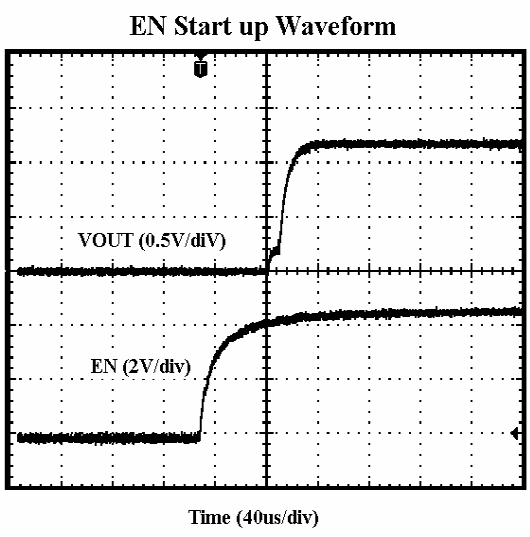


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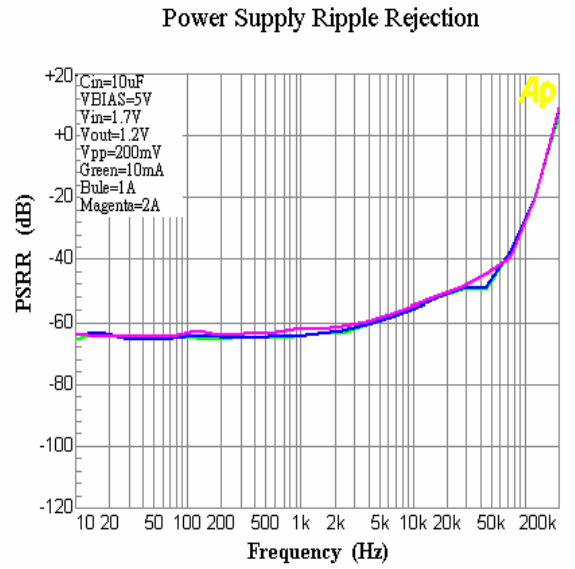


Figure 20.

Application Note

External Capacitors

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

Output Capacitor

The EUP7966 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (temperature characteristics X7R, X5R, Z5U, or Y5V) in 4.7 to 22μF range with 5mΩ to 200mΩ ESR range is suitable in the EUP7966 application circuit.
The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5mΩ to 200mΩ)

Input Capacitor

The input capacitor must be at least 10 μF ceramic, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input.

Bias Capacitor

The 1μF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

Bias Voltage

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 – 5.5V to assure proper operation of the part.

Shutdown Operation

Pulling down the VEN pin will turn-off the regulator. VEN pin must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator) , the pull-up resistor is not required. This pin must be tied to VIN if not used.

Power Dissipation /Heatsinking

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D=(V_{IN}-V_{OUT})I_{OUT}+(V_{IN})I_{GND}$$

where I_{GND} is the operating ground current of the device. The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temper -ature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax}=T_{Jmax}-T_{Amax}$$

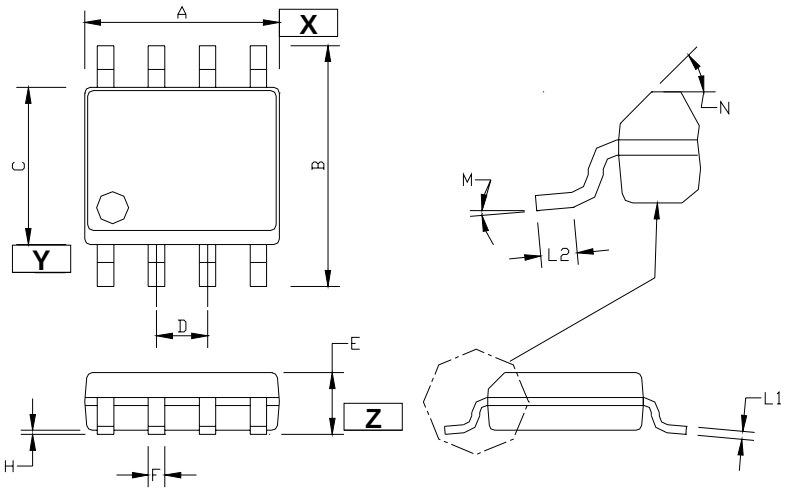
The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA}=T_{Rmax}/P_D$$

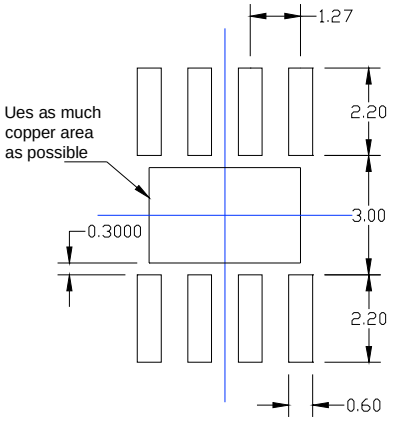
Heatsinking for the SOP-8 (FD) package is accomplished by allowing heat to flow through the ground slug on the bottom of the package into the copper on the PC board. The heat slug must be soldered down to a copper plane to get good heat transfer. It can also be connected through vias to internal copper planes .Since the heat slug is at ground potential, traces must not be routed under it which are not at ground potential. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

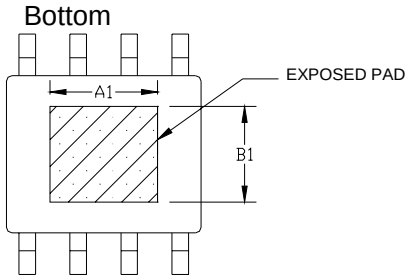
Packaging Information

SOP-8 (FD)



Standard Solder Map





Symbols	Dimension in Millimeters		Dimension in Inches	
	Min.	Max.	Min.	Max.
A	4.80	5.00	0.189	0.197
B	5.80	6.20	0.228	0.244
C	3.80	4.00	0.150	0.157
D	1.194	1.346	0.047	0.053
E	1.45	1.55	0.057	0.061
H	0.00	0.10	0.000	0.004
F	0.33	0.51	0.013	0.020
L1	0.19	0.25	0.007	0.010
L2	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	40°	50°	40°	50°
A1	2.6	2.8	0.102	0.110
B1	2.4	2.6	0.095	0.102