DM141

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8x2-Channels Constant Current LED Driver

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DM141

8x2-Bit Constant Current LED Drivers

General Description

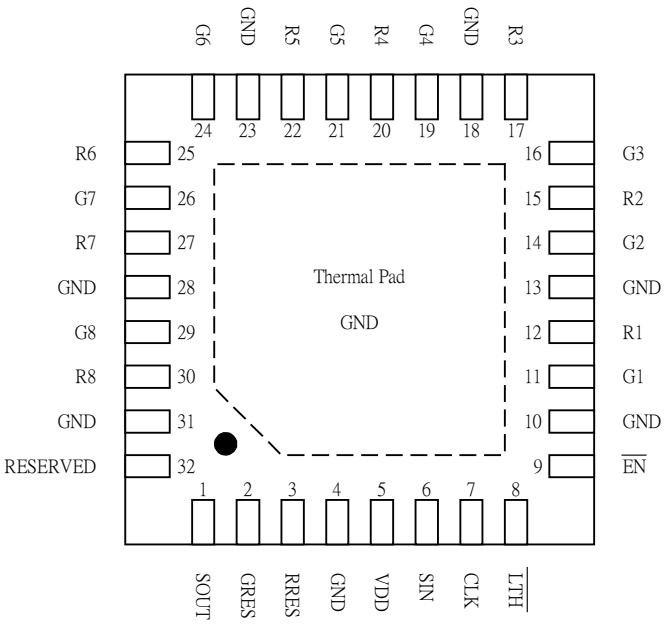
The DM141 is a constant current driver specifically designed for LED display applications. The device includes a 16-bit shift register, a latch, and dual-interleaved banks of constant current drivers on a single Silicon CMOS chip. Each of the dichotomous 8-bit banks requires a current setting resistor. The output current ranges from 5mA to 60mA.

Features

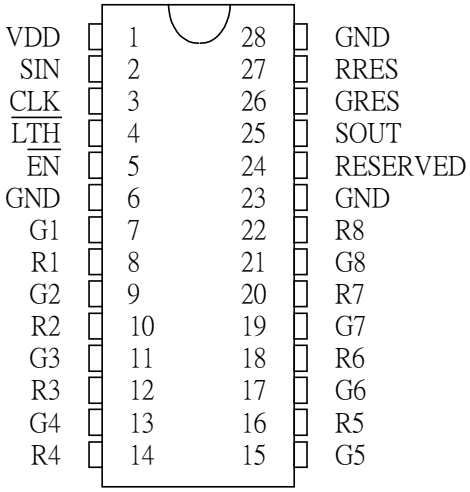
- Constant Current Output: From 5mA to 60mA
- Maximum Clock Frequency: 25MHz (Max)
- Power Supply Voltage: 3.3V to 5.0V
- CMOS Compatible Input/Output
- Package: QFN32, SDIP28, SSOP28
- Constant Current Matching:
  10mA to 60mA : Bit-to-Bit : ± 4.0% (Max)、
  Chip-to-Chip : ± 10.0% (Max)
  5mA to 10mA : Bit-to-Bit : ± 6.0% (Max)、
  Chip-to-Chip : ± 12.0% (Max)
- Maximum Output Voltage: 17V
- Two-color LED driving capability on chip

Pin Connection (Top view)

QFN32



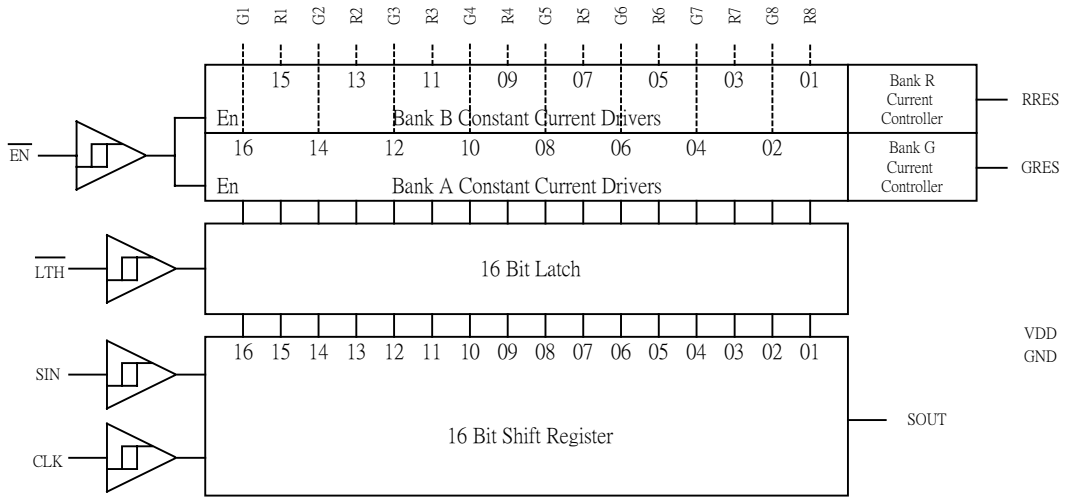
SDIP28, SSOP28



Pin Description

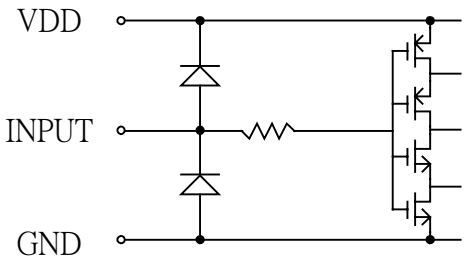
Pin No. (QFN32)	Pin No. (SDIP28, SSOP28)	Pin NAME	FUNCTION
5	1	V_{DD}	Supply voltage terminal.
6	2	SIN	Input terminal of a data shift register. Data for R8 should be shifted in first, and then the data for G8 followed.
7	3	CLK	Input terminal of a clock for shift register. Data is sampled at the rising edge of CLK.
8	4	$\overline{\text{LTH}}$	Input terminal of data strobe. Data is latched when $\overline{\text{LTH}}$ is low. And data on shift register goes through when $\overline{\text{LTH}}$ is high.
9	5	$\overline{\text{EN}}$	Input terminal of output enable (active low), all outputs are off when $\overline{\text{EN}}$ is high.
11, 14, 16, 19, 21, 24, 26, 29	7,9,11,13, 15,17,19,21	G1~8	Constant current output terminals (Bank G).
12, 15, 17, 20, 22, 25, 27, 30	8,10,12,14, 16,18,20,22	R1~8	Constant current output terminals (Bank R).
4, 10, 13, 18, 23, 28, 31	6,23,28	GND	Ground terminals.
32	24	RESERVED	Reserved pin for future.
1	25	SOUT	Output terminal of a data shift register.
2	26	GRES	Input terminal of an external resistor (Bank G). The current flows through the resistor from GRES to ground will be the (Bank G) reference base current of output sink current.
3	27	RRES	Input terminal of an external resistor (Bank R).

Block Diagram

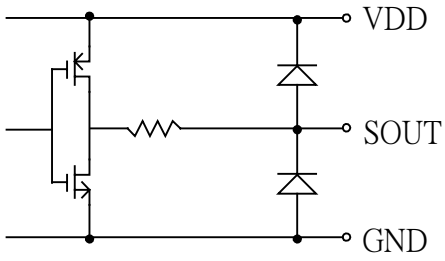


Equivalent Circuit of Inputs and Outputs

1. CLK, SIN, $\overline{\text{LTH}}$, $\overline{\text{EN}}$ terminals



2. SOUT terminal



Maximum Ratings ($T_{j(max)}$ = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0 ~ 7.0	V
Input Voltage	V_{IN}	-0.3 ~ VDD+0.3	V
Output Current	I_{OUT}	60	mA
Output Voltage	V_{OUT}	-0.3 ~ 17	V
Clock Frequency	f_{CLK}	25	MHz
GND Terminal Current	I_{GND}	960	mA
Power Dissipation	P_D	3.08 (QFN-32 : Ta=25°C)	W
		3.12 (SDIP-28 : Ta=25°C)	
		1.1 (SSOP-28 : Ta=25°C)	
Thermal Resistance	$R_{th(j-a)}$	40.6 (QFN-32)	°C/W
		40 (SDIP-28)	
		113.3 (SSOP-28)	
Storage Temperature	T_{stg}	-40 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	3.0	5.0	5.5	V
Output Voltage	V_{OUT}	—	—	—	17	V
Operating temperature	T_{OPR}	—	-20	—	85	℃
Output Current	I_O	(G, R)n	5	—	60	mA
	I_{OH}	SOUT	—	—	1.0	
	I_{OL}	SOUT	—	—	-1.0	
Input Voltage	V_{IH}	—	0.8VDD	—	VDD+0.3	V
	V_{IL}	—	-0.3	—	0.2VDD	
$\overline{LTH}$ Pulse Width	tw LAT	V_{DD} = 3.3 ~ 5.0 V	15	—	—	ns
CLK Pulse Width	tw CLK		15	—	—	ns
Set-up Time for DATA	tsetup(D)		10	—	—	ns
Hold Time for DATA	thold(D)		10	—	—	ns
Set-up Time for $\overline{LTH}$	tsetup(L)		15	—	—	ns
Clock Frequency	f_{CLK}	Cascade operation	—	—	25	MHz

Electrical Characteristics (Typ:VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	—		0.8VDD	—	VDD	V
Input Voltage "L" Level	VIL	—		GND	—	0.2VDD	
Output Leakage Current	IOH	VOH = 17 V		—	—	±1.0	uA
Output Voltage (SOUT)	VOL	IOL = 1.0 mA		—	—	0.3	V
	VOH	IOH = -1.0 mA		VDD-0.3	—	—	
Output Current (Bit-Bit)	IOL1	V(G, R)n = 1.0 RES = 11.2KΩ		—	—	±6	%
Output Current (Chip-Chip)	IOL3	V(G, R)n = 1.0V, RES = 11.2KΩ	Vdd=5.0V	4.66	5.3	5.94	mA
			Vdd=3.3V	4.57	5.2	5.83	
Output Voltage Regulation	% / VDD	RES = 1400Ω, V(G, R)n = 1V to 3V		—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VDD	V(G, R)n = 1.0V, RES = 1400Ω		—	±1.5	±3.0	% / V
Supply Current "OFF"	IDD(off)1	Input Signal is static, RES = OPEN, (G, R)1~8 = off		—	6	—	mA
	IDD(0ff)2	Input Signal is static, RES = 2800Ω, (G, R) 1~8 = off		—	9.5	—	
	IDD(off)3	Input Signal is static, RES = 1400Ω, (G, R) 1~8 = off		—	12.5	—	
Supply Current "ON"	IDD(on)1	Input Signal is static, RES = 2800Ω, (G, R) 1~8 = on		—	9.5	—	
	IDD(on)2	Input Signal is static, RES = 1400Ω, (G, R) 1~8 = on		—	12.5	—	

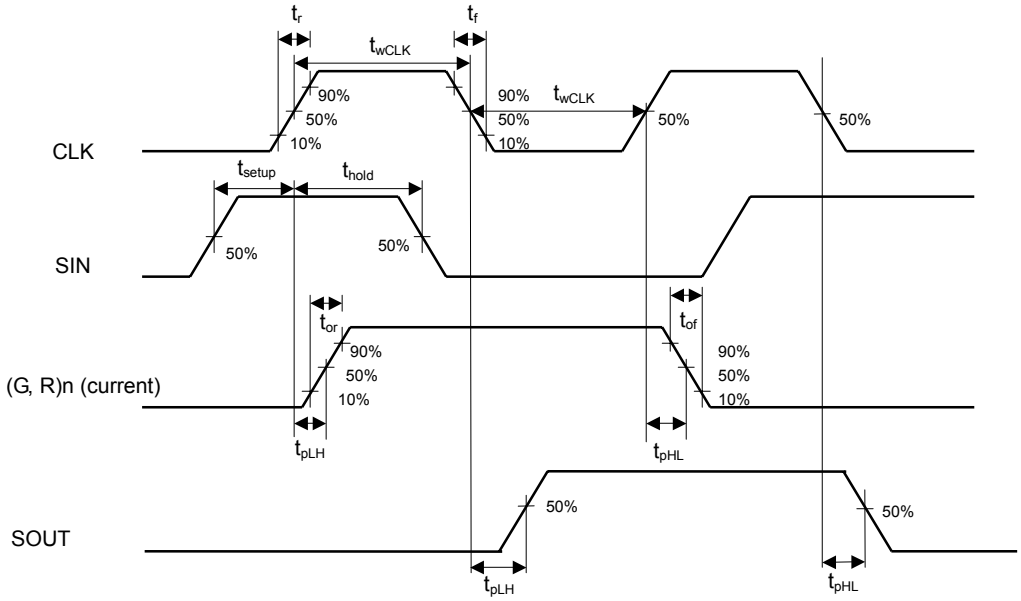
Switching Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	$\overline{EN}$-(G, R)n	tpLH	VDD=5.0V VIH=VDD VIL=GND (G, R)RES=1400Ω VL=3.3V RL=51Ω CL=15pF	—	60	—	ns
Propagation Delay Time ("H" to "L")	$\overline{EN}$-(G, R)n	tpHL		—	30	—	ns
Output Current Rise Time		tor		—	90	—	ns
Output Current Fall Time		tof		—	17	—	ns

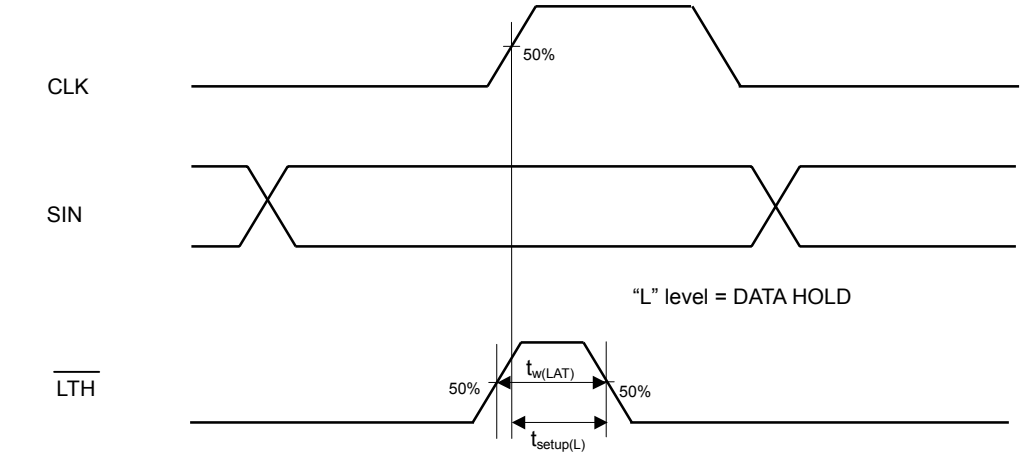
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	$\overline{EN}$-(G, R)n	tpLH	VDD=3.3V VIH=VDD VIL=GND (G, R)RES=1400Ω VL=3.3V RL=51Ω CL=15pF	—	90	—	ns
Propagation Delay Time ("H" to "L")	$\overline{EN}$-(G, R)n	tpHL		—	35	—	ns
Output Current Rise Time		tor		—	140	—	ns
Output Current Fall Time		tof		—	30	—	ns

Timing Diagram

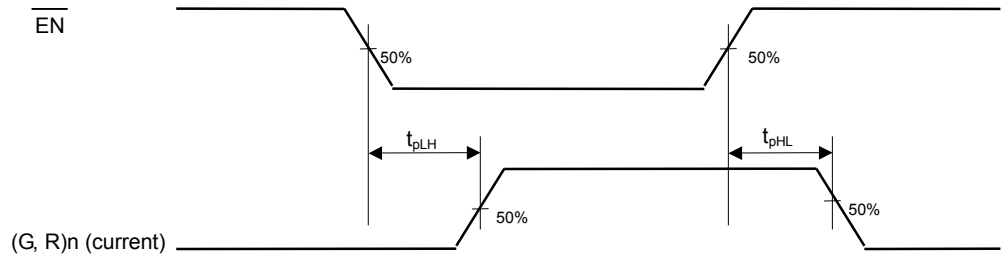
1. CLK-SIN, SOUT, (G,R)n



2. CLK-$\overline{LTH}$



3. $\overline{EN}$-(G, R)n



Detailed Description

- **Constant Current Output Value Setting**

The output current is determined by resistor value. The resistors connected between RES(G, R) pin and GND decide the base current output. Fig1. shows the approximate relation between resistor value and output current value. The resistor should be placed as close to Rext terminal as possible to avoid the noise influence

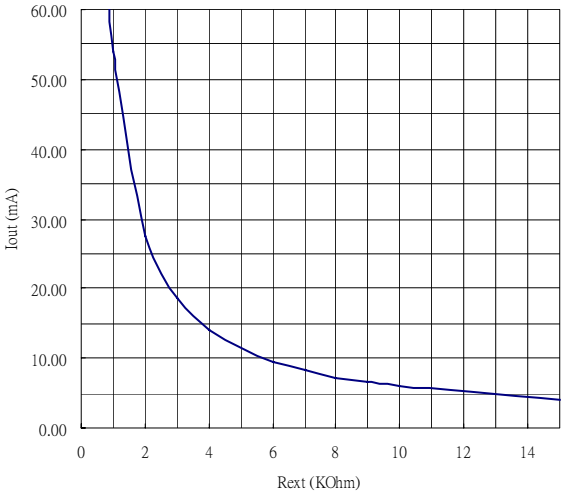


Fig.1

- **Output Current Performance vs. Output Voltage**

In order to obtain the good constant current output performance, the minimum output voltage is necessary.

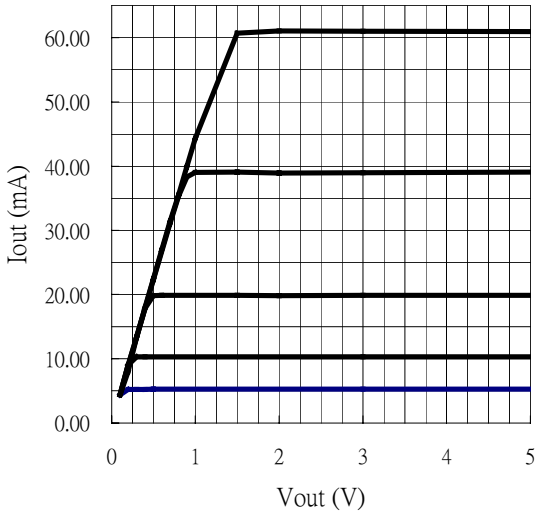
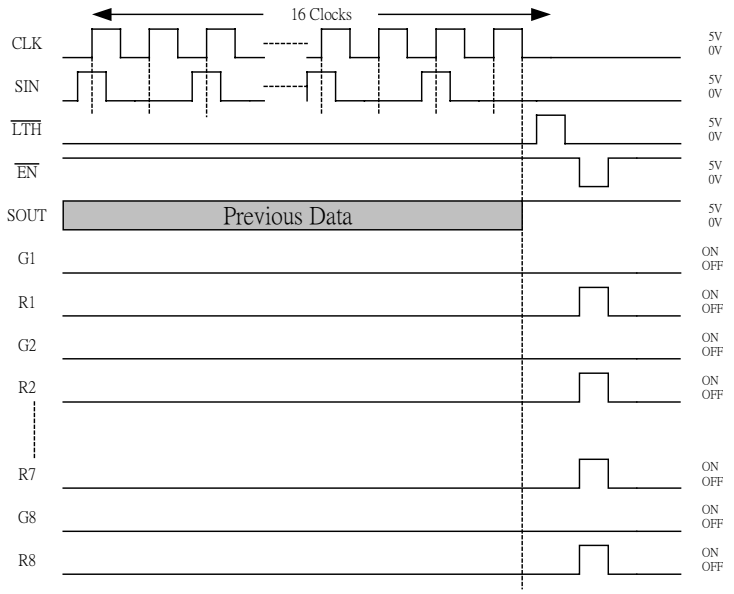


Fig. 2

- **Serial_In Data, Serial_Out and Latch**

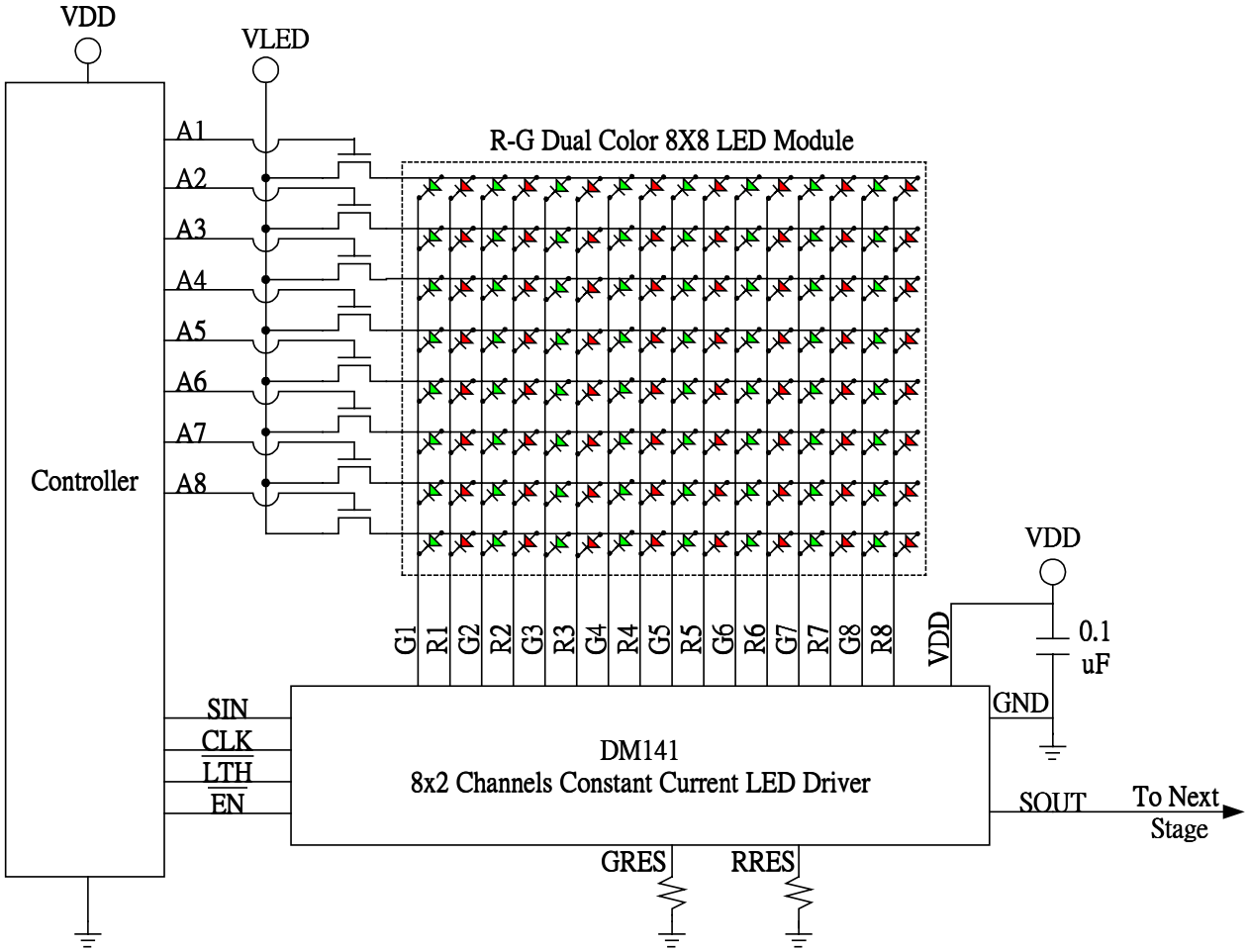
The SIN data will be clocked into the 16 bits shift register synchronized on the rising edge of CLK. And the data '1' represents the corresponding current output 'ON', while the data '0' stands for 'OFF'. The data will be transferred into the latch as the $\overline{\text{LTH}}$ pin goes high. And the data will be latched when $\overline{\text{LTH}}$ goes low.The SERIAL_OUT data is shifted out on synchronization to the falling edge of CLOCK. The graph below depicts the timing of data serial-in and serial-out.



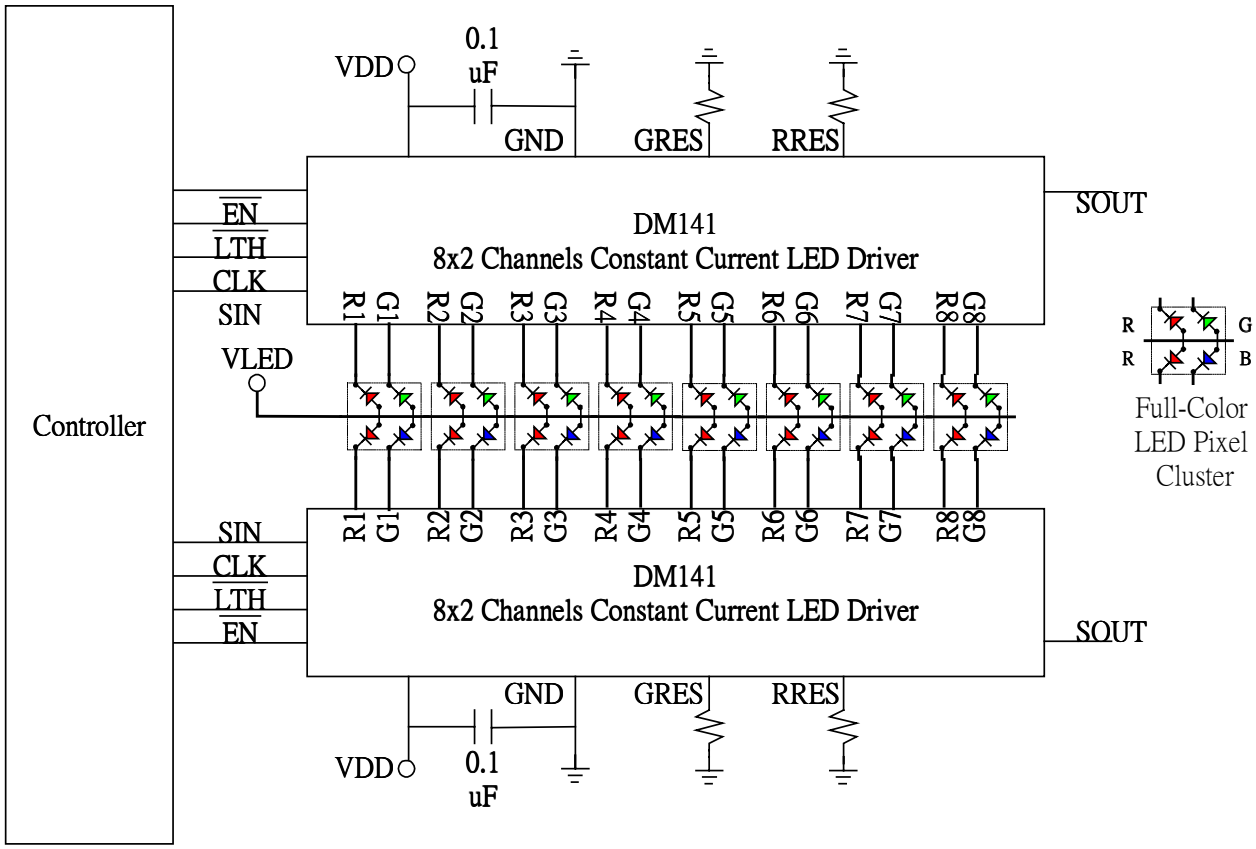
- **Package and Thermal Pad**

The IC's thermal pad (QFN) which is internally connected to the bottom side of chip should be connected to GND. And, good PCB layout pattern conducted to thermal pad will have better performance in thermal effect. Due to the small size and low profile, the majority of heat generated by the die within this package is dissipated through the thermal pad to PCB. The PCB configuration and metal layers embedded in the PCB become important to achieving good thermal performance. By increasing the embedded copper area, the thermal performance will be improved. Thermal vias which conduct heat from the surface of the PCB to the ground plane are necessary. More vias may improve the package thermal performance.

Typical Application

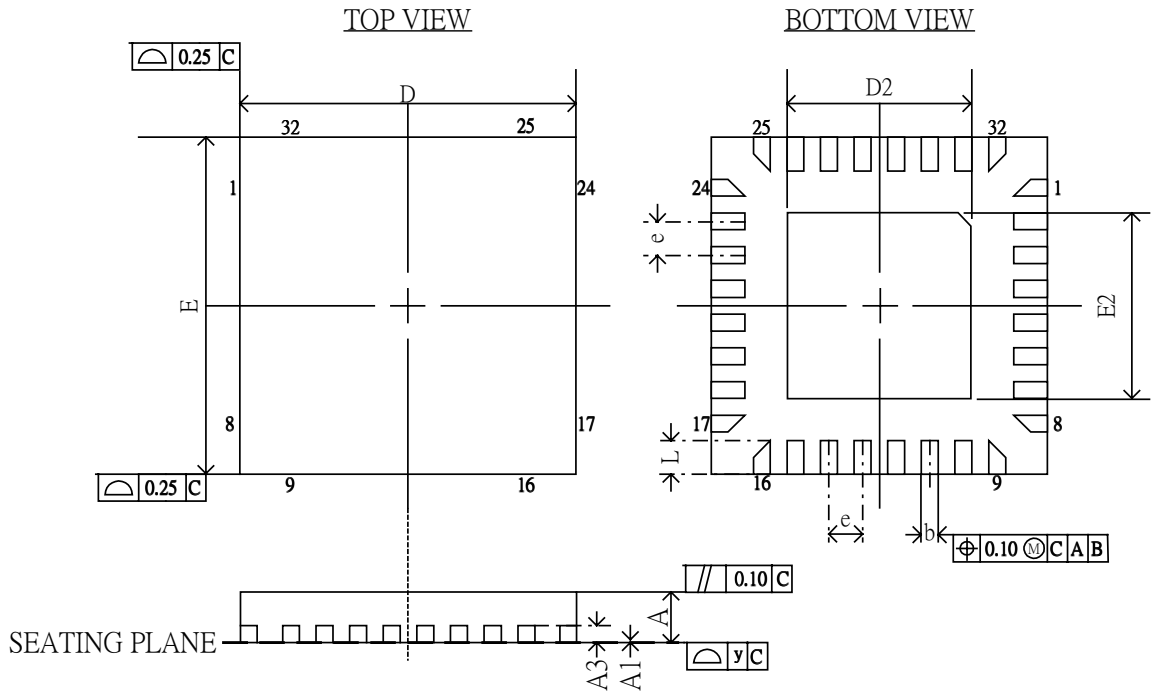


Typical Application



Package Outline

QFN32



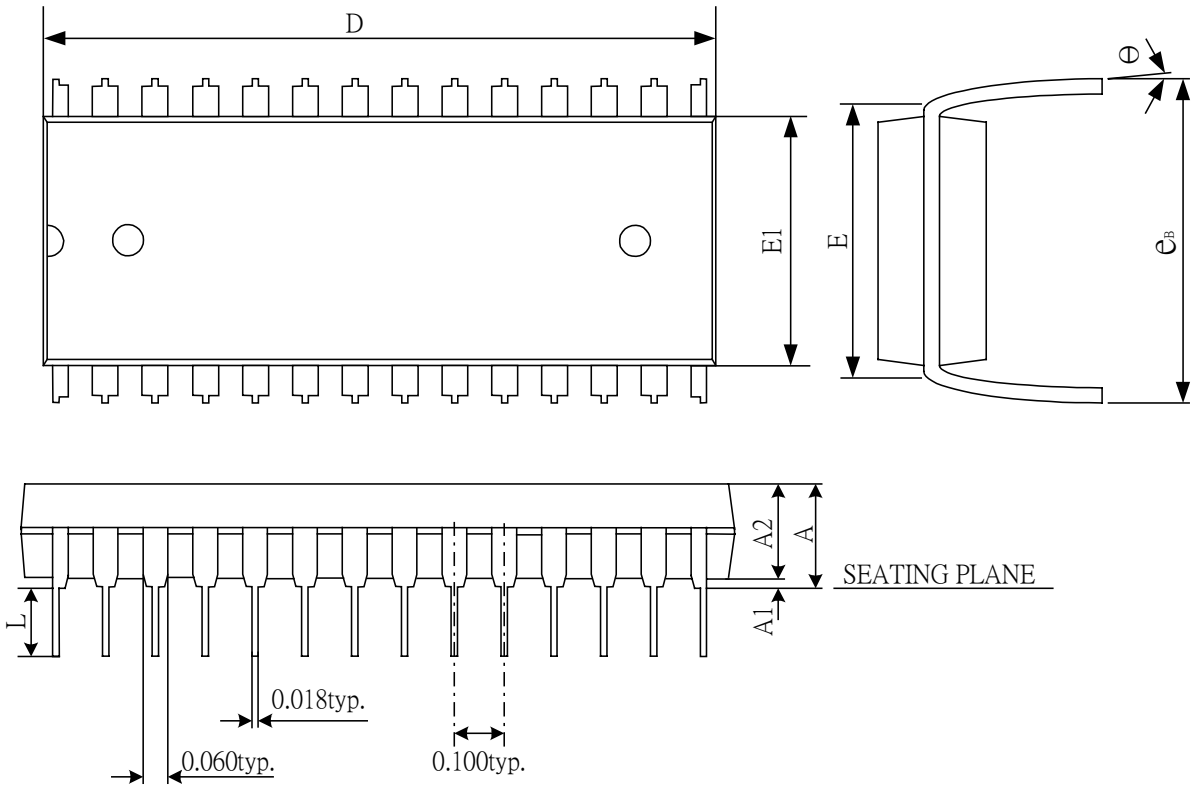
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.25 REF			9.84 REF		
B	0.18	0.23	0.30	7.09	9.06	11.81
D	5.00 BSC			196.85 BSC		
D2	1.25	2.70	3.25	49.21	106.30	127.95
E	5.00 BSC			196.85 BSC		
E2	1.25	2.70	3.25	49.21	106.30	127.95
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.81	15.75	19.69
y	0.10			3.94		

Note: 1.DIMENSIONING AND TOLERANCING CONFORM TO ASME Y145.5M-1994.

2. REFER TO JEDEC STD. MO-220 WHHD-2 ISSUE A

Package Outline

SDIP28

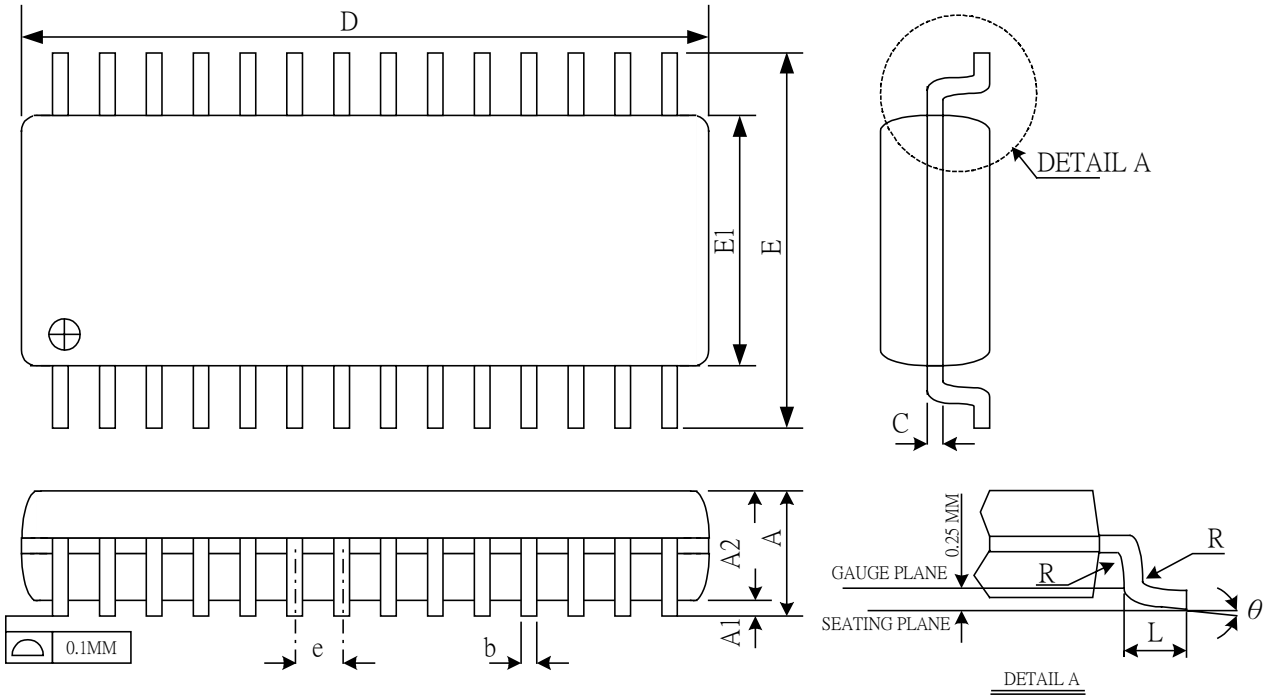


SYMBOLS	DIMENSION IN INCH		
	MIN.	NOM.	MAX.
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E1	0.283	0.288	0.293
E	0.31 BSC		
L	0.115	0.130	0.150
e_B	0.330	0.350	0.370
θ	0	7	15

Note:
1. JEDEC OUTLINE : N/A

Package Outline

SSOP28



NOTES:
1. JEDEC OUTLINE : MO-15D AH

2. DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MODE MISMATCH AND ARE MEASURED AT DATUM PLANE, MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.2MM PER SIDE.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/ INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 9.07mm AT LEAST MATERIAL CONDITION.

SYMBOLS	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	-	-	2.0
A1	0.05	-	-
A2	1.62	1.75	1.85
b	0.22	-	0.38
C	0.09	-	0.25
e	0.65 BSC		
D	9.9	10.20	10.50
E	7.4	7.8	8.2
E1	5.00	5.30	5.60
L	0.55	0.75	0.95
R	0.09	-	-
θ	0	4	8

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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