# MIC5821/5822

## 8-Bit Serial-Input Latched Drivers

## General Description

BiCMOS technology gives the MIC5821/5822 family flexibility beyond the reach of standard logic buffers and power driver arrays. These devices each have an eight-bit CMOS shift register, CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. The 500mA outputs are suitable for use with incandescent bulbs and other moderate to high current loads. The drivers can be operated with a split supply where the negative supply is down to –20V. Except for maximum driver output voltage ratings, the MIC5821 and MIC5822 are identical.

These devices have greatly improved data-input rates. With a 5V logic supply they will typically operate faster than 5 MHz. With a 12V supply significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

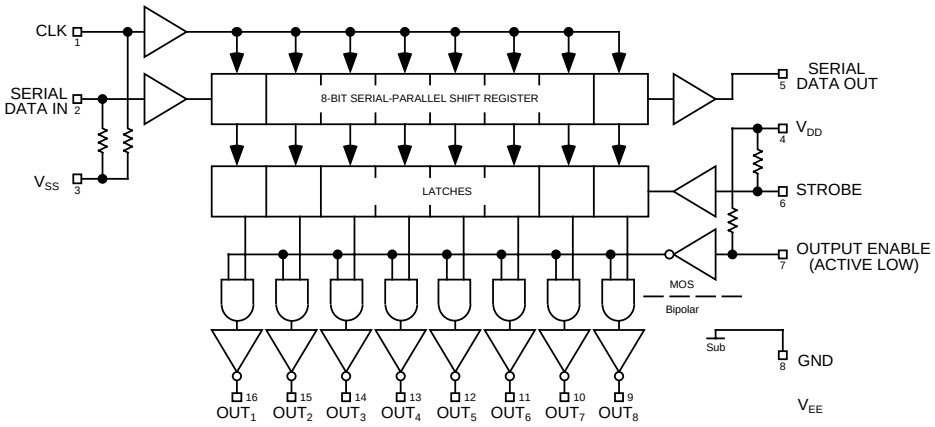
## Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down or Pull-Up Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Single or Split Supply Operation

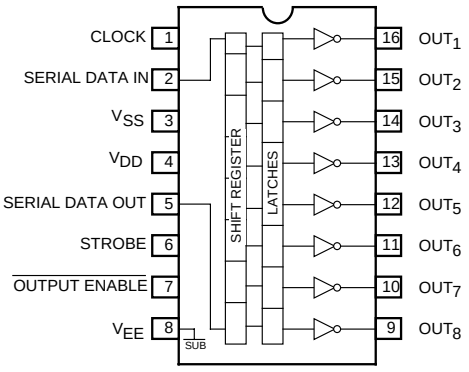
## Ordering Information

| Part Number | Temperature Range | Package |
|---|---|---|
| MIC5821BN | –40°C to +85°C | 16-Pin Plastic DIP |
| MIC5822BN | –40°C to +85°C | 16-Pin Plastic DIP |

## Functional Diagram

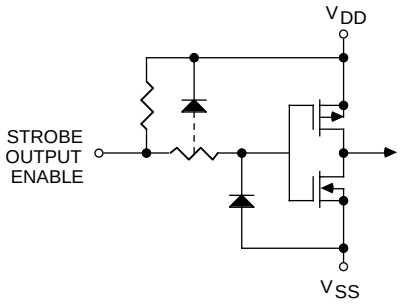



## Pin Configuration




(Plastic DIP)

## Typical Input Circuits

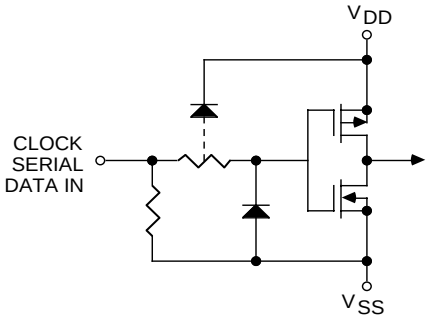



## Absolute Maximum Ratings (Note 1)

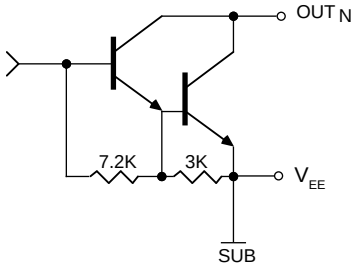
at 25°C Free-Air Temperature and $V_{SS}$ = 0V

| | | |
|---|---|---|
| Output Voltage, $V_{CE}$ | (MIC5821) | 50V |
| | (MIC5822) | 80V |
| Output Voltage, $V_{CE\ SUS}$ | (MIC5821)(Note 3) | 35V |
| | (MIC5822)(Note 3) | 50V |
| Logic Supply Voltage, $V_{DD}$ | | 15V |
| Input Voltage Range, $V_{IN}$ | | –0.3V to $V_{DD}$ + 0.3V |
| $V_{DD} - V_{EE}$ | | 25V |
| Emitter Supply Voltage, $V_{EE}$ | | –20V |
| Continuous Output Current, $I_{OUT}$ | | 500mA |
| Package Power Dissipation, $P_{D(Note\ 1)}$ | | 1.67W |
| Operating Temperature Range, $T_A$ | | –55°C to +85°C |
| Storage Temperature Range, $T_S$ | | –65°C to +150°C |

Note 1: Derate at the rate of 16.7mW/°C above $T_A$ = 25°C.
Note 2: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.
Note 3: For inductive load applications.




## Typical Output Driver




## Maximum Allowable Duty Cycle (Plastic DIP)

| Number of Outputs ON ($I_{OUT}$ = 200mA $V_{DD}$ = 12V) | Maximum Allowable Duty Cycle at Ambient Temperature of | | | | |
|---|---|---|---|---|---|
| | 25°C | 40°C | 50°C | 60°C | 70°C |
| 8 | 73% | 62% | 55% | 47% | 40% |
| 7 | 83% | 71% | 62% | 54% | 46% |
| 6 | 97% | 82% | 72% | 63% | 53% |
| 5 | 100% | 98% | 87% | 75% | 63% |
| 4 | 100% | 100% | 100% | 93% | 79% |
| 3 | 100% | 100% | 100% | 100% | 100% |
| 2 | 100% | 100% | 100% | 100% | 100% |
| 1 | 100% | 100% | 100% | 100% | 100% |

## Electrical Characteristics at $T_A$ = 25°C $V_{DD}$ = 5V, $V_{EE}$ = $V_{SS}$ = 0V (unless otherwise specified)

| Characteristic | Symbol | Applicable Devices | Test Conditions | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| Output Leakage Current | $I_{CEX}$ | MIC5821 | $V_{OUT}$ = 50V | | 50 | µA |
| | | | $V_{OUT}$ = 50V, $T_A$ = +70°C | | 100 | |
| | | MIC5822 | $V_{OUT}$ = 80V | | 50 | |
| | | | $V_{OUT}$ = 80V, $T_A$ = +70°C | | 100 | |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | Both | $I_{OUT}$ = 100mA | | 1.1 | V |
| | | | $I_{OUT}$ = 200mA | | 1.3 | |
| | | | $I_{OUT}$ = 350mA, $V_{DD}$ = 7.0V | | 1.6 | |
| Input Voltage | $V_{IN(0)}$ | Both | | | 0.8 | V |
| | $V_{IN(1)}$ | Both | $V_{DD}$ = 12V | 10.5 | | |
| | | | $V_{DD}$ = 10V | 8.5 | | |
| | | | $V_{DD}$ = 5.0V | 3.5 | | |
| Input Resistance | $R_{IN}$ | Both | $V_{DD}$ = 12V | 50 | | kΩ |
| | | | $V_{DD}$ = 10V | 50 | | |
| | | | $V_{DD}$ = 5.0V | 50 | | |
| Supply Current | $I_{DD(ON)}$ | Both | One Driver ON, $V_{DD}$ = 12V | | 4.5 | mA |
| | | | One Driver ON, $V_{DD}$ = 10V | | 3.9 | |
| | | | One Driver ON, $V_{DD}$ = 5.0V | | 2.4 | |
| | | | All Drivers ON, $V_{DD}$ = 12V | | 16 | |
| | | | All Drivers ON, $V_{DD}$ = 10V | | 14 | |
| | | | All Drivers ON, $V_{DD}$ = 5.0V | | 8 | |
| | $I_{DD(OFF)}$ | Both | All Drivers OFF, $V_{DD}$ = 5.0V, All Inputs = 0V | | 1.6 | |
| | | | All Drivers OFF, $V_{DD}$ = 12V, All Inputs= 0V | | 2.9 | |

## Electrical Characteristics $T_A$ = –55°C, $V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V (unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|
| Output Leakage Current | $I_{CEX}$ | $V_{OUT}$ = 80V | | 50 | µA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_{OUT}$ = 100mA | | 1.3 | V |
| | | $I_{OUT}$ = 200mA | | 1.5 | |
| | | $I_{OUT}$ = 350mA, $V_{DD}$ = 7.0V | | 1.8 | |
| Input Voltage | $V_{IN0)}$ | | | 0.8 | V |
| | $V_{IN(1)}$ | $V_{DD}$ = 12V | 10.5 | | |
| | | $V_{DD}$ = 5.0V | 3.5 | | |
| Input Resistance | RIN | $V_{DD}$ = 12V | 35 | | kΩ |
| | | $V_{DD}$ = 10V | 35 | | |
| | | $V_{DD}$ = 5.0V | 35 | | |
| Supply Current | $I_{DD(ON)}$ | One Driver ON, $V_{DD}$ = 12V | | 5.5 | mA |
| | | One Driver ON, $V_{DD}$ = 10V | | 4.5 | |
| | | One Driver ON, $V_{DD}$ = 5.0V | | 3.0 | |
| | | All Drivers ON, $V_{DD}$ = 12V | | 16 | |
| | | All Drivers ON, $V_{DD}$ = 10V | | 14 | |
| | | All Drivers ON, $V_{DD}$ = 5.0V | | 10 | |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{DD}$ = 12V | | 3.5 | |
| | | All Drivers OFF, $V_{DD}$ = 5.0V | | 2.0 | |

## Electrical Characteristics $T_A$ = +125°C, $V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V (unless otherwise noted)

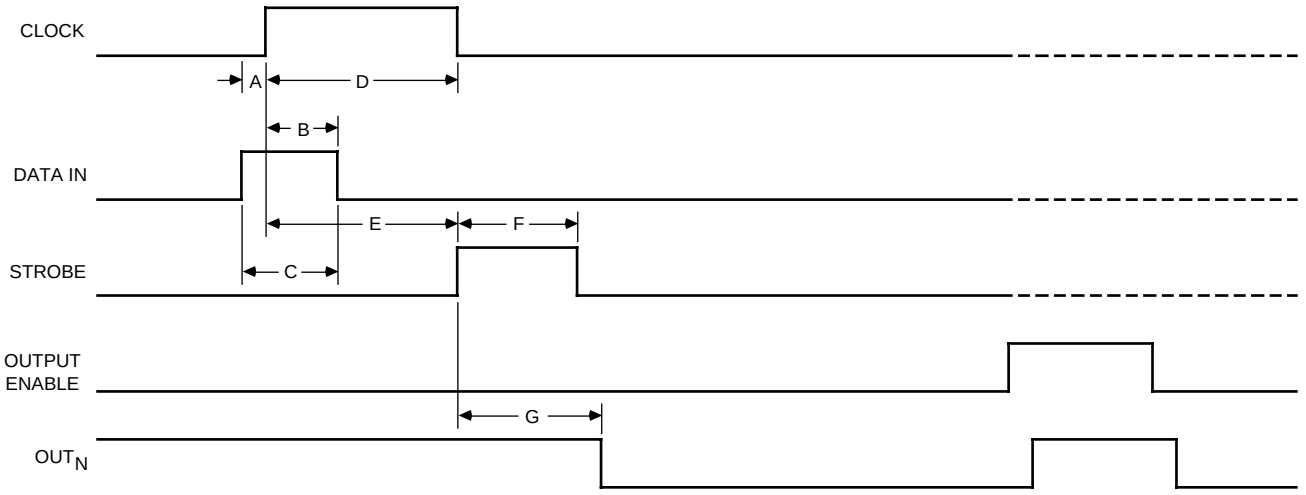
| Characteristic | Symbol | Test Conditions | Limits | | |
|---|---|---|---|---|---|
| | | | Min. | Max. | Unit |
| Output Leakage Current | $I_{CEX}$ | $V_{OUT}$ = 80V | | 500 | µA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_{OUT}$ = 100mA | | 1.3 | V |
| | | $I_{OUT}$ = 200mA | | 1.5 | |
| | | $I_{OUT}$ = 350mA, $V_{DD}$ = 7.0V | | 1.8 | |
| Input Voltage | $V_{IN(0)}$ | | | 0.8 | V |
| | $V_{IN(1)}$ | $V_{DD}$ = 12V | 10.5 | | |
| | | $V_{DD}$ = 5.0V | 3.5 | | |
| Input Resistance | $R_{IN}$ | $V_{DD}$ = 12V | 50 | | kΩ |
| | | $V_{DD}$ = 10V | 50 | | |
| | | $V_{DD}$ = 5.0V | 50 | | |
| Supply Current | $I_{DD(ON)}$ | One Driver ON, $V_{DD}$ = 12V | | 4.5 | mA |
| | | One Driver ON, $V_{DD}$ = 10V | | 3.9 | |
| | | One Driver ON, $V_{DD}$ = 5.0V | | 2.4 | |
| | | All Drivers ON, $V_{DD}$ = 12V | | 16 | |
| | | All Drivers ON, $V_{DD}$ = 10V | | 14 | |
| | | All Drivers ON, $V_{DD}$ = 5.0V | | 8 | |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{DD}$ = 12V | | 2.9 | |
| | | All Drivers OFF, $V_{DD}$ = 5.0V | | 1.6 | |

## MIC5821/5822 Family Truth Table

| Serial Data Input | Clock Input | Shift Register Contents $I_1$ | $I_2$ | $I_3$ | …… | $I_8$ | Serial Data Output | Strobe Input | Latch Contents $I_1$ | $I_2$ | $I_3$ | …… | $I_8$ | Output Enable | Output Contents $I_1$ | $I_2$ | $I_3$ | …… | $I_8$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | ⎍ | H | $R_1$ | $R_2$ | …… | $R_7$ | $R_7$ | | | | | | | | | | | | |
| L | ⎍ | L | $R_1$ | $R_2$ | …… | $R_7$ | $R_7$ | | | | | | | | | | | | |
| X | ⎎ | $R_1$ | $R_2$ | $R_3$ | …… | $R_8$ | $R_8$ | | | | | | | | | | | | |
| | | X | X | X | …… | X | X | L | $R_1$ | $R_2$ | $R_3$ | …… | $R_8$ | | | | | | |
| | | $P_1$ | $P_2$ | $P_3$ | …… | $P_8$ | $P_8$ | H | $P_1$ | $P_2$ | $P_3$ | …… | $P_8$ | L | $P_1$ | $P_2$ | $P_3$ | …… | $P_8$ |
| | | | | | | | | | X | X | X | …… | X | H | H | H | H | …… | H |

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

## Timing Diagram



## Timing Conditions

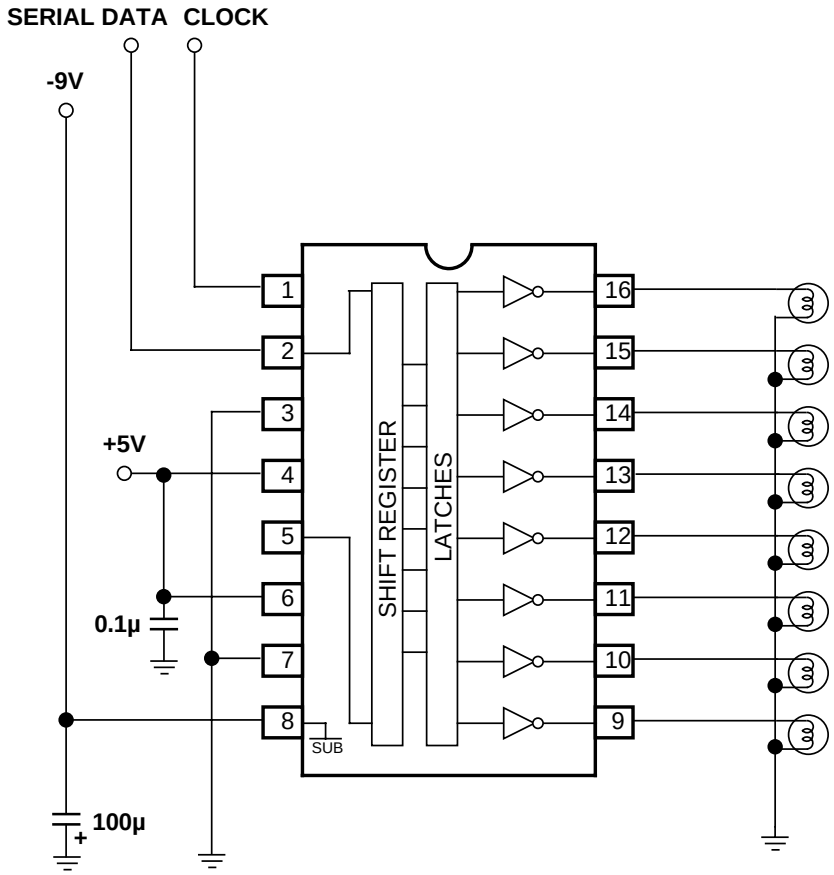
($T_A$ = +25°C, Logic Levels are $V_{DD}$ and $V_{SS}$)

| | $V_{DD}$ = 5.0V |
|---|---|
| A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) | 75 ns |
| B. Minimum Data Active Time After Clock Pulse (Data Hold Time) | 75 ns |
| C. Minimum Data Pulse Width | 150 ns |
| D. Minimum Clock Pulse Width | 150 ns |
| E. Minimum Time Between Clock Activation and Strobe | 300 ns |
| F. Minimum Strobe Pulse Width | 100 ns |
| G. Typical Time Between Strobe Activation and Output Transition | 500 ns |

SERIAL DATA present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

## Typical Applications

**MIC5822 Level Shifting Lamp Driver with Darlington Emitters Tied to a Negative Supply**