Data Sheet
January 1999

microelectronics group

Lucent Technologies
Bell Labs Innovations

Quad Differential Drivers
BDG1A, BDP1A, BDGLA, BPNGA, BPNPA, and BPPGA

Features

- Pin-equivalent to the general-trade 26LS31 device, with improved speed, reduced power consumption, and significantly lower levels of EMI
- Four line drivers per package
- Meets ESDI standards
- 2.0 ns maximum propagation delay
- Single 5.0 V ± 10% supply
- Operating temperature range: –40 °C to +125 °C (wider than the 41 Series)
- 400 Mbits/s maximum data rate
- Logic to convert TTL input logic levels to differential, pseudo-ECL output logic levels
- No line loading when V_{CC} = 0 (BDG1A, BDP1A only)
- High output driver for 50 Ω loads
- <0.2 ns output skew (typical)
- On-chip 220 Ω loads available
- Third-state outputs available
- Surge-protection to ±60 V for 10 ms available (BPNGA, BPNPA, BPPGA)
- Available in four package types
- ESD performance better than the 41 Series
- Lower power requirement than the 41 Series

Description

These quad differential drivers are TTL input-to-pseudo-ECL-differential-output used for digital data transmission over balanced transmission lines. All devices in this family have four drivers with a single enable control in a common package. These drivers are compatible with many receivers, including the Lucent Technologies Microelectronics Group 41 Series receivers and transceivers. They are pin equivalent to the general-trade 26LS31, but offer increased speed, decreased power consumption, and significantly lower levels of electromagnetic interference (EMI). They replace the Lucent 41 Series drivers.

The BDG1A device is the generic driver in this family and requires the user to supply external resistors on the circuit board for impedance matching.

The BDGLA is a low-power version of the BDG1A, reducing the power requirement by more than one half. The BDGLA features a 3-state output with a typical third-state level of 0.2 V.

The BDP1A is equivalent to the BDG1A but has 220 Ω termination resistors to ground on each driver output. This eliminates the need for external pull-down resistors when driving a 100 Ω impedance line.

The BPNGA and BPNPA are equivalent to the BDG1A and BDP1A, respectively, except that a lightning protection circuit has been added to the driver outputs. This circuit will absorb large transitions on the transmission lines without destroying the device.

The BPPGA combines the features of the BPNGA and BPNPA. Two of the gates have their outputs terminated to ground through 220 Ω resistors while the two remaining gates require external termination resistors.

When the BDG1A and the BDP1A devices are powered down, the output circuit appears as an open circuit relative to the power supplies; hence, they will not load the transmission line. For those circuits with termination resistors, the line will remain impedance matched when the circuit is powered down. The BPNGA, BPNPA, BPPGA, and BDGLA will load the transmission line, because of the protection circuit, when the circuit is powered down.

The packaging options that are available for these quad differential line drivers include a 16-pin DIP; a 16-pin, J-lead SOJ; a 16-pin, gull-wing SOIC; and a 16-pin, narrow-body, gull-wing SOIC.

Pin Information

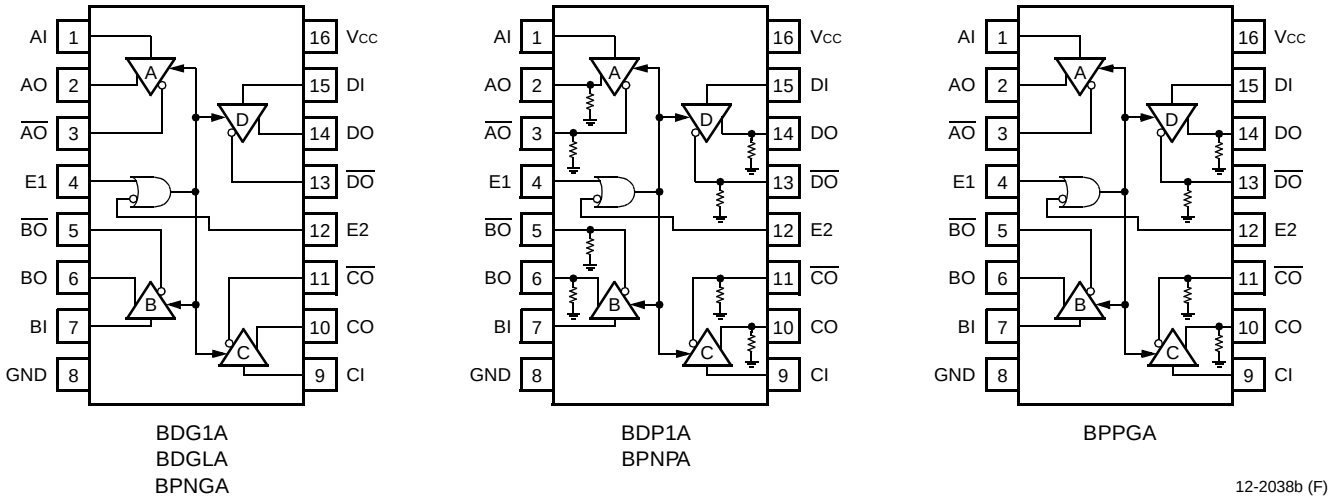


Figure 1. Quad Differential Driver Logic Diagrams

Table 1. Enable Truth Table

E1	E2	Condition
0	0	Active
1	0	Active
0	1	Disabled
1	1	Active

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	6.5	V
Ambient Operating Temperature	T_A	–40	125	°C
Storage Temperature	T_{stg}	–55	150	°C

Electrical Characteristics

For electrical characteristics over the entire temperature range, see Figures 7 through 9.

Table 2. Power Supply Current Characteristics

T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{CC} = 5.5 V):					
All Outputs Disabled:					
BDG1A*, BPNGA*	I_{CC}	—	45	65	mA
BDP1A†, BPNPA†	I_{CC}	—	120	160	mA
BDGLA*	I_{CC}	—	35	55	mA
BPPGA*†	I_{CC}	—	85	115	mA
All Outputs Enabled:					
BDG1A*, BPNGA*	I_{CC}	—	25	40	mA
BDP1A†, BPNPA†	I_{CC}	—	150	200	mA
BDGLA*	I_{CC}	—	14	20	mA
BPPGA*†	I_{CC}	—	90	115	mA

* Measured with no load (BPPGA has no load on drivers C and D).

† The additional power dissipation is the result of integrating the termination resistors into the device. I_{CC} is measured with a 100 Ω resistor across the driver outputs (BPPGA has terminating resistors on drivers A and B).

Third State

These drivers produce pseudo-ECL levels, and the third-state mode is different than the conventional TTL devices. When a driver is placed in the third state, the bases of the output transistors are pulled low, bringing the outputs below the active-low levels. This voltage is typically 2 V for most drivers. In the bidirectional bus application, the driver of one device, which is in its third state, may be back driven by another driver on the bus whose voltage in the low state is lower than the third-stated device. This could come about due to differences in the drivers' independent power supplies. In this case, the device in the third state will control the line, thus clamping the line and reducing the signal swing. If the difference voltage between the independent power supplies and the drivers is small, then this consideration can be ignored. In the typical case, the difference voltage can be as much as 1 V without significantly affecting the amplitude of the driving signal.

Electrical Characteristics (continued)

Table 3. Voltage and Current Characteristics

For the variation in V_{OH} and V_{OL} over the temperature range, see Figures 7 and 8.

T_A = –40 °C to +125 °C.*

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages:					
Low*	V_{OL}	V_{OH} – 1.4	V_{OH} – 1.1	V_{OH} – 0.65	V
High*:					
BDG1A, BDP1A, BPNGA, BPNPA, BPPGA	V_{OH}	V_{CC} – 1.8	V_{CC} – 1	V_{CC} – 0.8	V
BDGLA	V_{OH}	V_{CC} – 2.5	V_{CC} – 2	V_{CC} – 1.6	V
Differential Voltage (V_{OH} – V_{OL})	V_{DIFF}	0.65	1.1	1.4	V
Output Voltages (T_A = 0 °C to 85 °C):					
Low*	V_{OL}	V_{OH} – 1.4	V_{OH} – 1.1	V_{OH} – 0.8	V
High*:					
BDG1A, BDP1A, BPNGA, BPNPA, BPPGA	V_{OH}	V_{CC} – 1.5	V_{CC} – 1	V_{CC} – 0.8	V
BDGLA	V_{OH}	V_{CC} – 2.5	V_{CC} – 2	V_{CC} – 1.6	V
Differential Voltage (V_{OH} – V_{OL})	V_{DIFF}	0.8	1.1	1.4	V
Third State, I_{OH} = –1.0 mA, V_{CC} = 4.5 V:					
BDG1A, BDP1A, BPNGA, BPNPA, BPPGA	V_{OZ}	—	V_{OL} – 0.5	V_{OL} – 0.2	V
BDGLA	V_{OZ}	—	0.2	0.5	V
Input Voltages:					
Low, V_{CC} = 5.5 V:					
Data Input	V_{IL}†	—	—	0.8	V
Enable Input	V_{IL}†	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}	2.0	—	—	V
Clamp, V_{CC} = 4.5 V, I_I = –5.0 mA	V_{IK}	—	—	–1.0	V
Short-circuit Output Current, V_{CC} = 5.5 V	I_{OS}‡	–100	—	—	mA
Input Currents, V_{CC} = 5.5 V:					
Low, V_I = 0.4 V	I_{IL}	—	—	–400	µA
High, V_I = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_I = 5.5 V	I_{IH}	—	—	100	µA
Output Resistors:					
BDP1A, BPNPA, BPPGA§	R_O	—	220	—	Ω

* Values are with terminations as per Figure 4 or equivalent.

† The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

‡ Test must be performed one lead at a time to prevent damage to the device.

§ See Figure 1 for BPPGA terminations.

Timing Characteristics

Table 4. Timing Characteristics (See Figures 2 and 3.)

For t_{P1} and t_{P2} propagation delays over the temperature range, see Figure 9.

Propagation delay test circuit connected to output (see Figure 6).

T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay:					
Input High to Output†	t_{P1}*	0.8	1.2	2.0	ns
Input Low to Output†	t_{P2}*	0.8	1.2	2.0	ns
Capacitive Delay	Δt_p	—	0.02	0.03	ns/pF
Disable Time (either E1 or E2):					
High-to-high Impedance	t_{PHZ}	4	8	12	ns
Low-to-high Impedance	t_{PLZ}	4	8	12	ns
Enable Time (either E1 or E2):					
High Impedance to High	t_{PZH}	4	8	12	ns
High Impedance to Low	t_{PZL}	4	8	12	ns
Output Skew, $\lvert t_{P1} - t_{P2} \rvert$	t_{skew1}	—	0.1	0.3	ns
$\lvert t_{PHH} - t_{PHL} \rvert$, $\lvert t_{PLH} - t_{PLL} \rvert$	t_{skew2}	—	0.2	0.5	ns
Difference Between Drivers	Δt_{skew}	—	—	0.3	ns
Rise Time (20%—80%)	t_{tLH}	—	0.7	2	ns
Fall Time (80%—20%)	t_{tHL}	—	0.7	2	ns

* t_{P1} and t_{P2} are measured from the 1.5 V point of the input to the crossover point of the outputs (see Figure 2).

† CL = 5 pF. Capacitor is connected from each output to ground.

Timing Characteristics (continued)

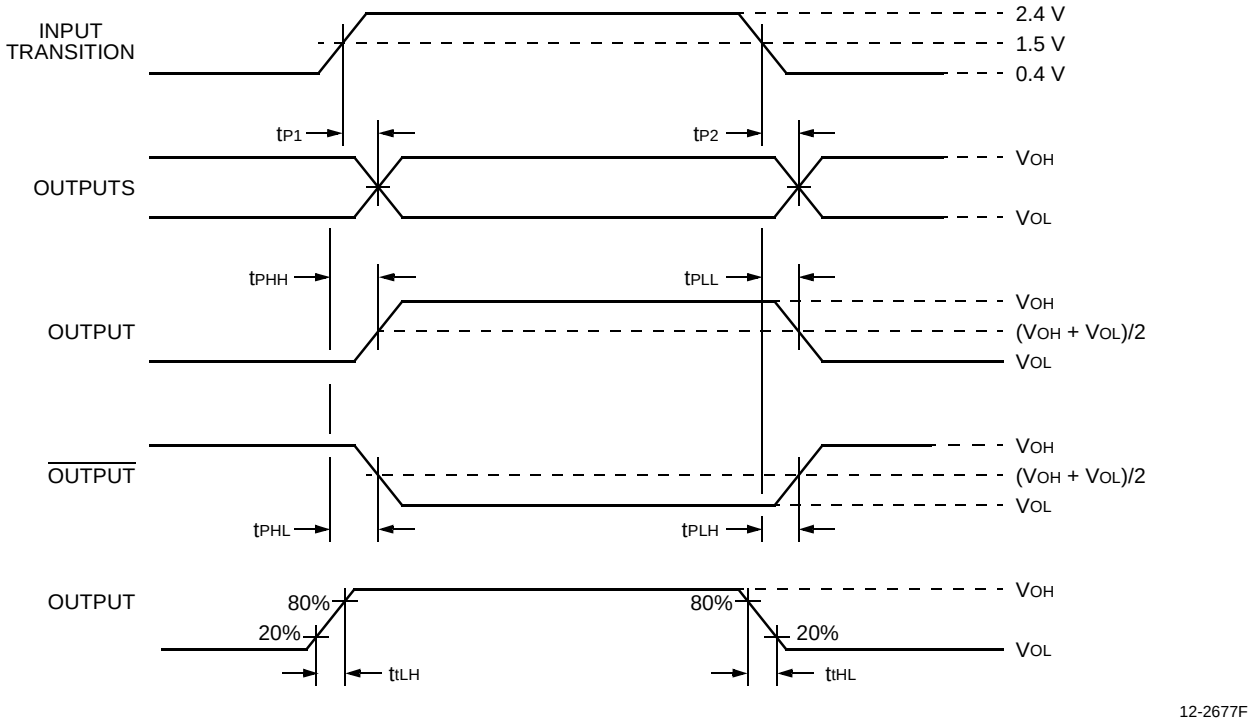
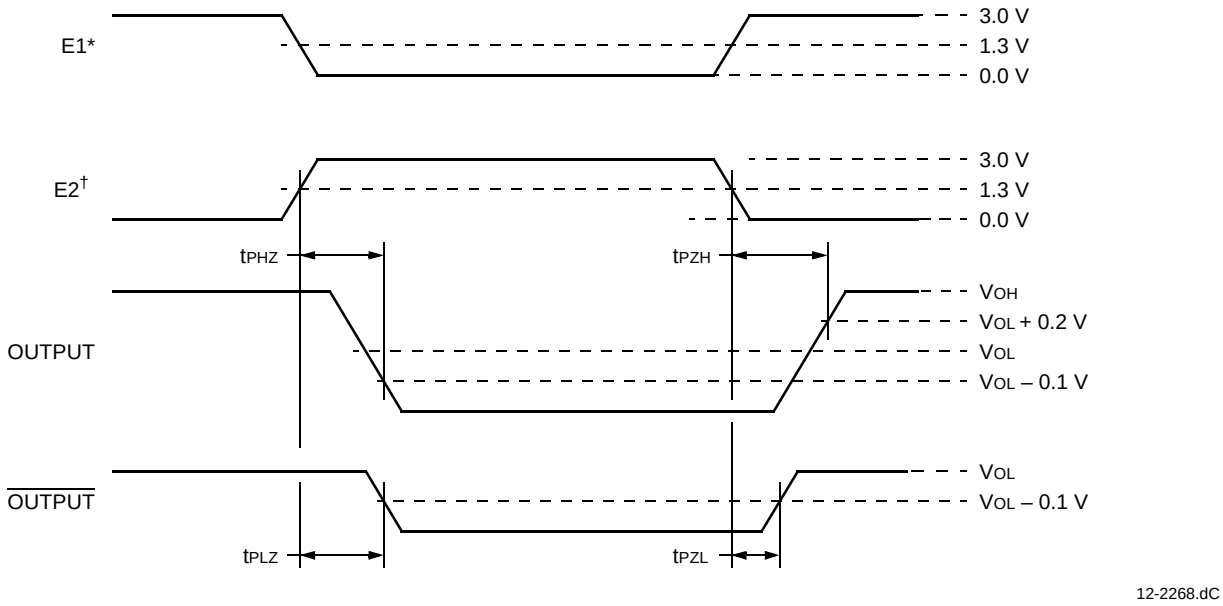


Figure 2. Driver Propagation-Delay Timing



* E2 = 1 while E1 changes state.

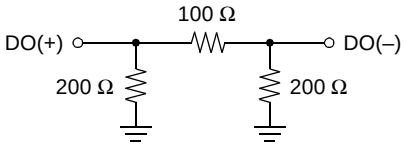
† E1 = 0 while E2 changes state.

Note: In the third state, both outputs (i.e., OUTPUT and $\overline{\text{OUTPUT}}$) are 0.2 V below the low state.

Figure 3. Driver Enable and Disable Timing for a High Input

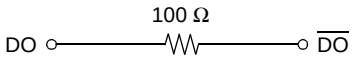
Test Conditions

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.



BDG1A, BPNGA, BDGLA, BPPGA (Gates A & B)

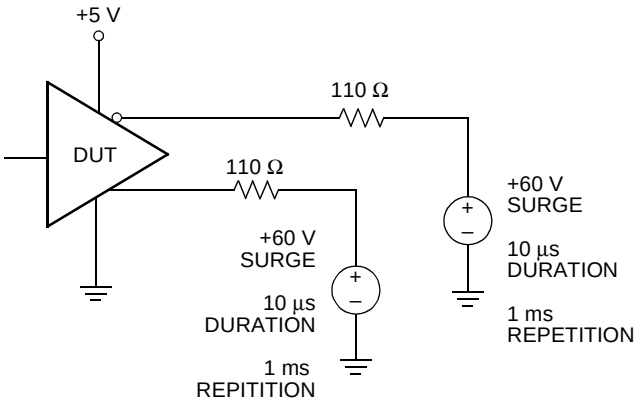
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BDP1A, BPNPA, BPPGA (Gates C & D)

12-2271.bC

Figure 4. Driver Test Circuit



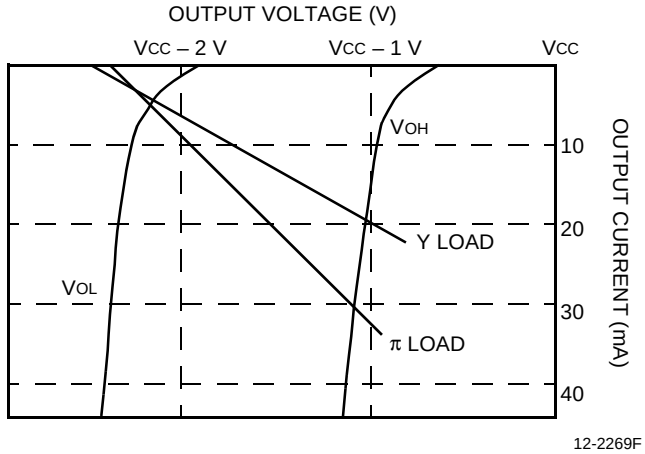
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Note: Surges can be applied simultaneously, but never in opposite polarities.

Figure 5. Lightning-Surge Testing Configuration (BPNGA, BPNPA, and BPPGA)

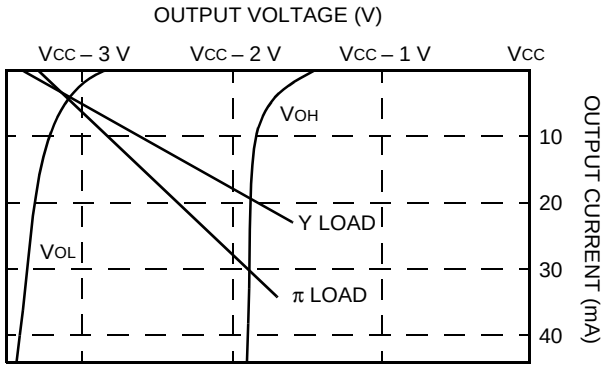
Output Characteristics

Figure 6 illustrates typical driver output characteristics. Included are load lines for two typical termination configurations.



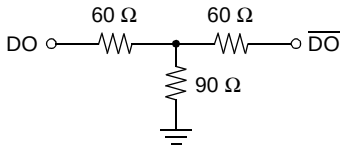
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A. Output Current vs. Output Voltage for Loads Shown in C and D (BDG1A, BDP1A, BPNGA, BPNPA, and BPPGA)



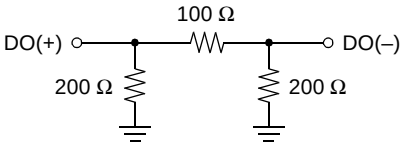
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B. Output Current vs. Output Voltage for Loads Shown in C and D (BDGLA)



12-2270F

C. Y Load



12-2271F

D. π Load

Figure 6. Driver Output Current vs. Voltage Characteristics

Temperature Characteristics

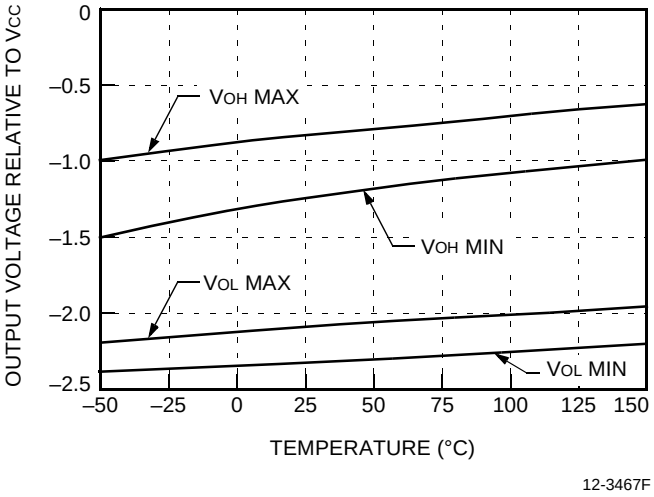


Figure 7. V_{OL} and V_{OH} Extremes vs. Temperature for 100 Ω Load

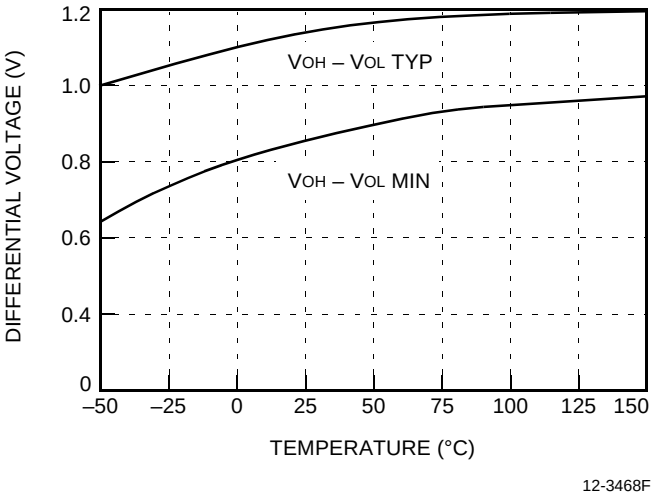


Figure 8. Differential Voltage (V_{OH} – V_{OL}) vs. Temperature for 100 Ω Load

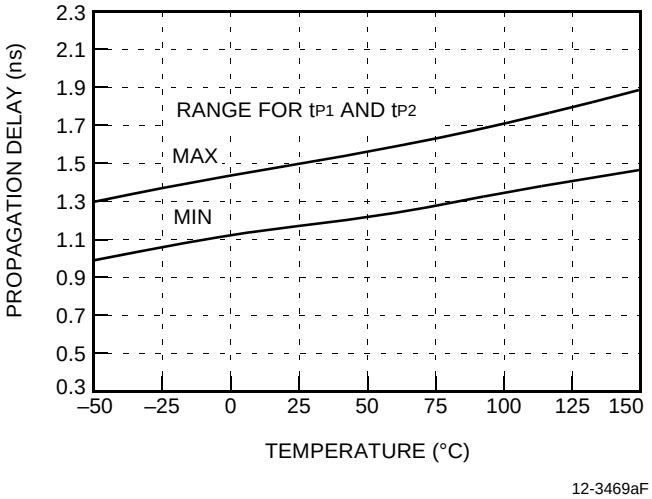


Figure 9. Min and Max for t_{P1} and t_{P2} Propagation Delays vs. Temperature

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

When handling and mounting line driver products, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD). The user should adhere to the following basic rules for ESD control:

1. Assume that all electronic components are sensitive to ESD damage.
2. Never touch a sensitive component unless properly grounded.
3. Never transport, store, or handle sensitive components except in a static-safe environment.

ESD Failure Models

Lucent employs two models for ESD events that can cause device damage or failure.

1. A human-body model (HBM) that is used by most of the industry for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.
2. A charged-device model (CDM), which many believe is the better simulator of electronics manufacturing exposure.

Tables 5 and 6 illustrate the role these two models play in the overall prevention of ESD damage. HBM ESD testing is intended to simulate an ESD event from a charged person. The CDM ESD testing simulates charging and discharging events that occur in production equipment and processes, e.g., an integrated circuit sliding down a shipping tube.

The HBM ESD threshold voltage presented here was obtained by using these circuit parameters.

Table 5. Typical ESD Thresholds for Data Transmission Drivers

Device	HBM Threshold	CDM Threshold
BDG1A, BDGLA	>2500	>1000
BDP1A	>2500	>2000
BPPGA, BPNGA, BPNPA	>3000	>2000

Table 6. ESD Damage Protection

	ESD Threat Controls	
	Personnel	**Processes**
Control	Wrist straps ESD shoes Antistatic flooring	Static-dissipative materials Air ionization
Model	Human-body model (HBM)	Charged-device model (CDM)

Latch-Up

Latch-up evaluation has been performed on the data transmission drivers. Latch-up testing determines if power-supply current exceeds the specified maximum due to the application of a stress to the device under test. A device is considered susceptible to latch-up if the power supply current exceeds the maximum level and remains at that level after the stress is removed.

Lucent performs latch-up testing per an internal test method that is consistent with JEDEC Standard No. 17 (previously JC-40.2) “CMOS Latch-Up Standardized Test Procedure.”

Latch-up evaluation involves three separate stresses to evaluate latch-up susceptibility levels:

1. dc current stressing of input and output pins.
2. Power supply slew rate.
3. Power supply overvoltage.

Table 7. Latch-Up Test Criteria and Test Results

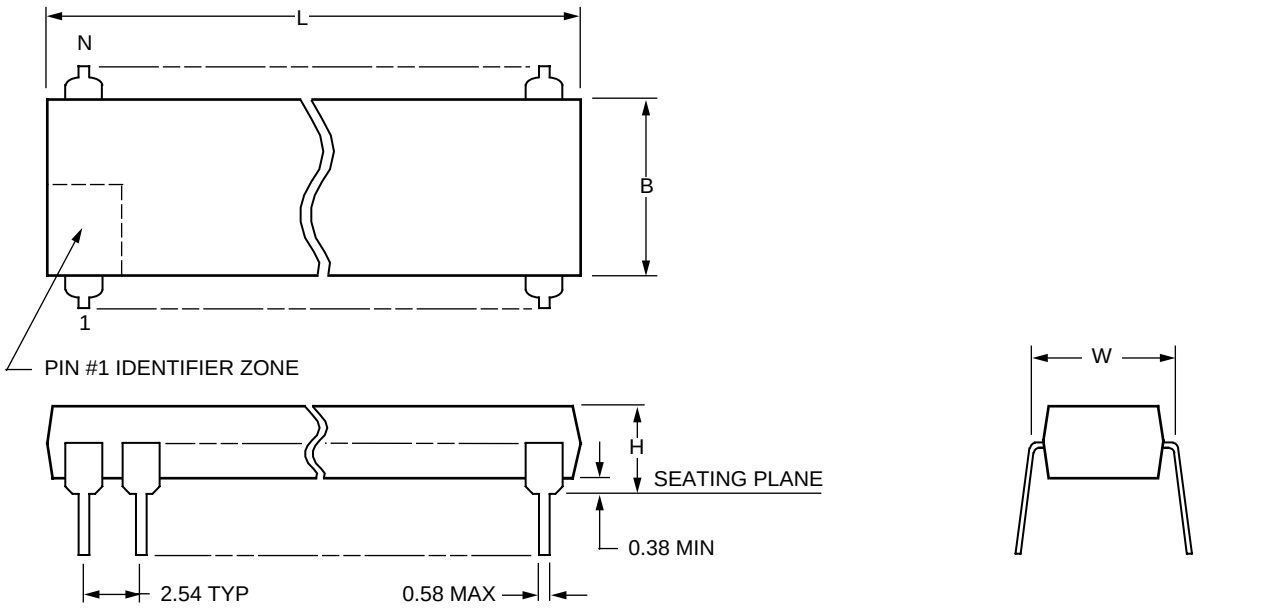
		dc Current Stress of I/O Pins	Power Supply Slew Rate	Power Supply Overvoltage
Data Transmission Driver ICs	**Minimum Criteria**	≥150 mA	≤1 µs	≥1.75 × Vmax
	Test Results	≥250 mA	≤100 ns	≥2.25 × Vmax

Based on the results in Table 6, the data transmission drivers pass the Lucent latch-up testing requirements and are considered not susceptible to latch-up.

Outline Diagrams

16-Pin DIP

Dimensions are in millimeters.



5-4410r.2 (C)

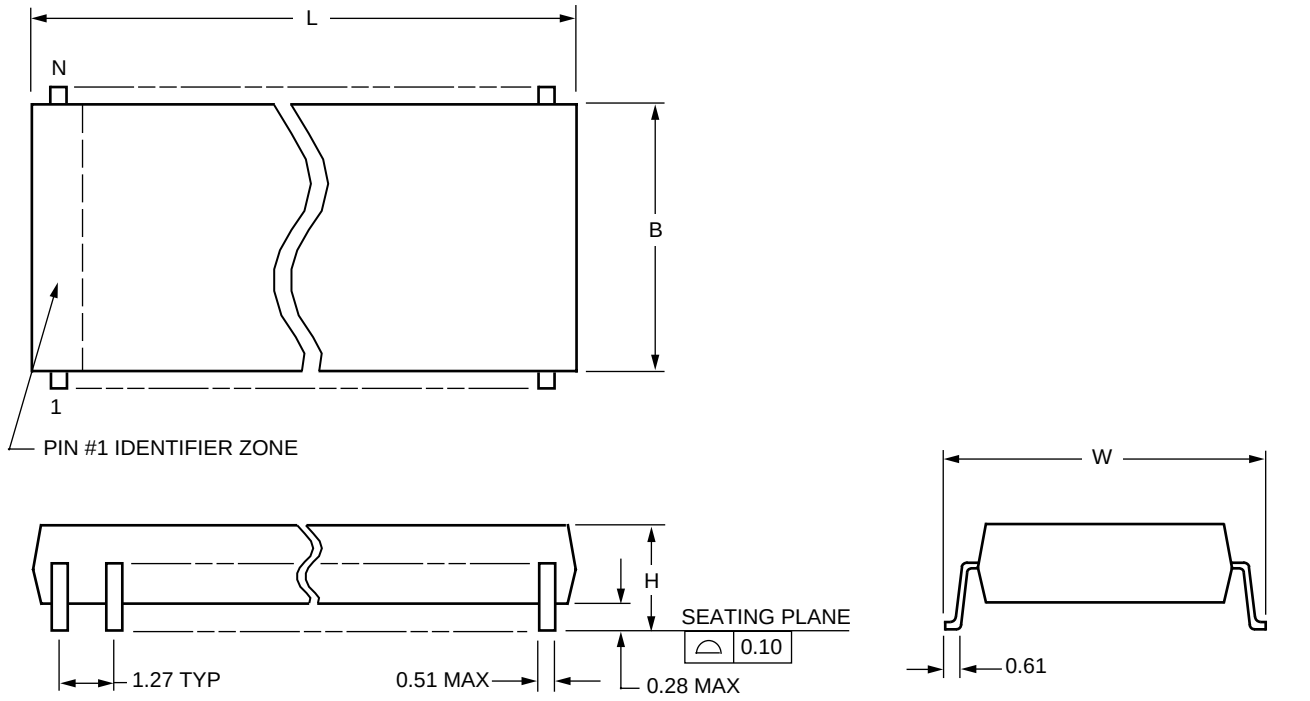
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
PDIP3 (Plastic Dual-In-Line Package)	16	20.57	6.48	7.87	5.08

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.

Outline Diagrams (continued)

16-Pin SOIC (SONB/SOG)

Dimensions are in millimeters.



5-4414r.3 (C)

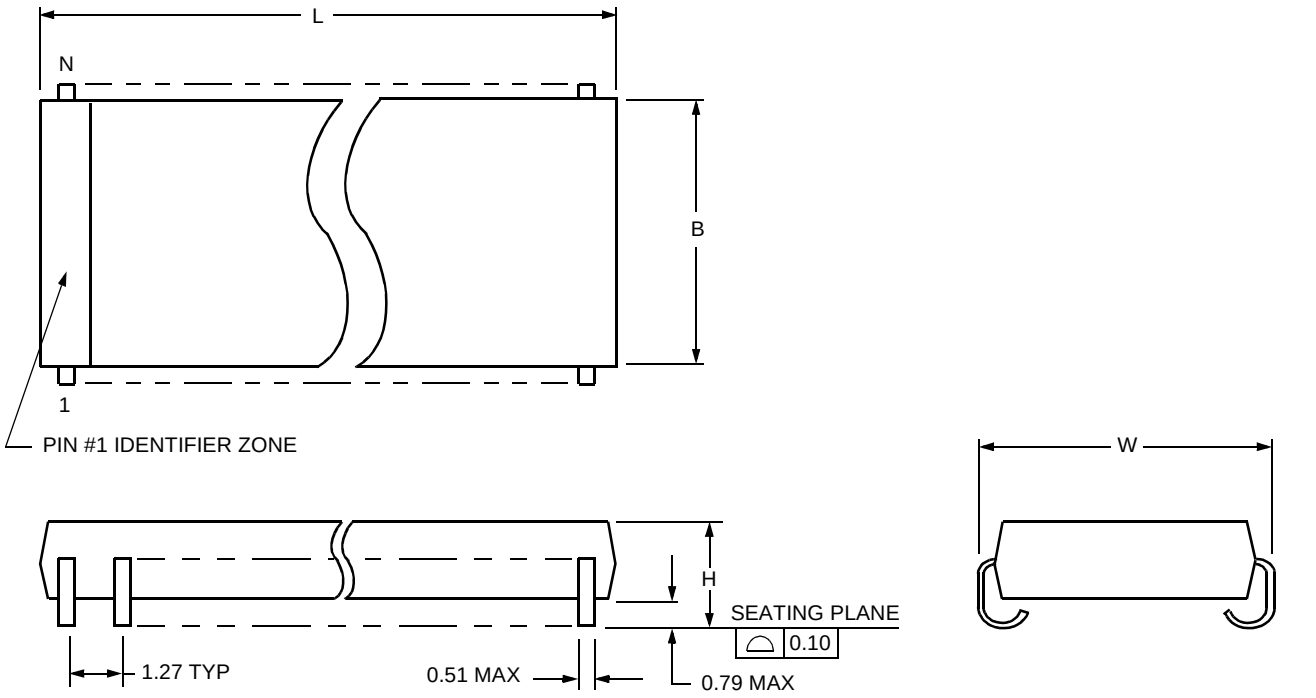
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
SONB (Small-Outline, Narrow Body)	16	10.11	4.01	6.17	1.73
SOG (Small-Outline, Gull-Wing)	16	10.49	7.62	10.64	2.67

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.

Outline Diagrams (continued)

16-Pin SOIC (SOJ)

Dimensions are in millimeters.



5-4413r.3 (C)

Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
SOJ (Small-Outline, J-Lead)	16	10.41	7.62	8.81	3.18

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.

Power Dissipation

System designers incorporating Lucent data transmission drivers in their applications should be aware of package and thermal information associated with these components.

Proper thermal management is essential to the long-term reliability of any plastic encapsulated integrated circuit. Thermal management is especially important for surface-mount devices, given the increasing circuit pack density and resulting higher thermal density. A key aspect of thermal management involves the junction temperature (silicon temperature) of the integrated circuit.

Several factors contribute to the resulting junction temperature of an integrated circuit:

- Ambient use temperature
- Device power dissipation
- Component placement on the board
- Thermal properties of the board
- Thermal impedance of the package

Thermal impedance of the package is referred to as Θ_{ja} and is measured in °C rise in junction temperature per watt of power dissipation. Thermal impedance is also a function of airflow present in system application.

The following equation can be used to estimate the junction temperature of any device:

$T_j = T_A + P_D \Theta_{ja}$

where:

T_j is device junction temperature (°C).

T_A is ambient temperature (°C).

P_D is power dissipation (W).

Θ_{ja} is package thermal impedance (junction to ambient—°C/W).

The power dissipation estimate is derived from two factors:

- Internal device power
- Power associated with output terminations

Multiplying I_{CC} times V_{CC} provides an estimate of internal power dissipation.

The power dissipated in the output is a function of the:

- Termination scheme on the outputs
- Termination resistors
- Duty cycle of the output

Package thermal impedance depends on:

- Airflow
- Package type (e.g., DIP, SOIC, SOIC/NB)

The junction temperature can be calculated using the previous equation, after power dissipation levels and package thermal impedances are known.

Figure 10 illustrates the thermal impedance estimates for the various package types as a function of airflow. This figure shows that package thermal impedance is higher for the narrow-body SOIC package. Particular attention should, therefore, be paid to the thermal management issues when using this package type.

In general, system designers should attempt to maintain junction temperature below 125 °C. The following factors should be used to determine if specific data transmission drivers in particular package types meet the system reliability objectives:

- System ambient temperature
- Power dissipation
- Package type
- Airflow

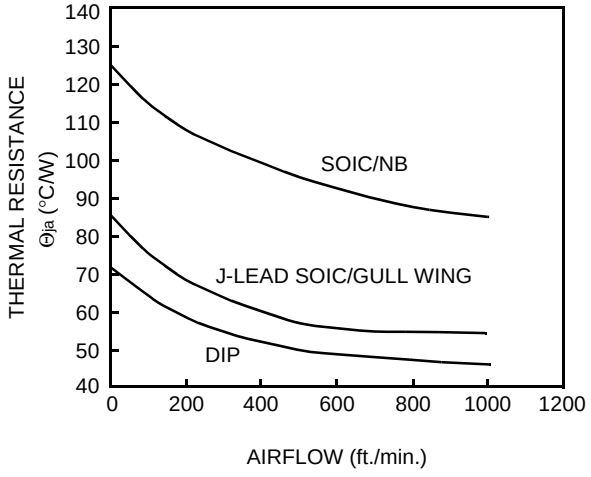


Figure 10. Power Dissipation

Ordering Information

Part Number	Intern. Term.	Surge Prot.	Package Type	Comcode	Former Pkg. Type	Former Part #
BDG1A16E	None	No	16-pin, Plastic SOJ	107914186	1041	LG, MG, MGA
BDG1A16E-TR	None	No	Tape & Reel SOJ	107914194	1041	LG, MG, MGA
BDG1A16G	None	No	16-pin, Plastic SOIC	107914160	1141	LG, MG, MGA
BDG1A16G-TR	None	No	Tape & Reel SOIC	107914178	1141	LG, MG, MGA
BDG1A16NB	None	No	Plastic SOIC/NB	107914202	1241	LG, MG, MGA
BDG1A16NB-TR	None	No	Tape & Reel SOIC/NB	107914210	1241	LG, MG, MGA
BDG1A16P	None	No	16-pin, Plastic DIP	107914004	41	LG, MG, MGA
BDP1A16E	220 Ω	No	16-pin, Plastic SOJ	107914293	1041	LP, MP, MPA
BDP1A16E-TR	220 Ω	No	Tape & Reel SOJ	107914301	1041	LP, MP, MPA
BDP1A16G	220 Ω	No	16-pin, Plastic SOIC	107914319	1141	LP, MP, MPA
BDP1A16G-TR	220 Ω	No	Tape & Reel SOIC	107914327	1141	LP, MP, MPA
BDP1A16P	220 Ω	No	16-pin, Plastic DIP	107914335	41	LP, MP, MPA
BDGLA16E	None	No	16-pin, Plastic SOJ	107914228	1041	MGL3
BDGLA16E-TR	None	No	Tape & Reel SOJ	107914236	1041	MGL3
BDGLA16G	None	No	16-pin, Plastic SOIC	107914244	1141	MGL3
BDGLA16G-TR	None	No	Tape & Reel SOIC	107914251	1141	MGL3
BDGLA16NB	None	No	Plastic SOIC/NB	107914269	1241	MGL3
BDGLA16NB-TR	None	No	Tape & Reel SOIC/NB	107914277	1241	MGL3
BDGLA16P	None	No	16-pin, Plastic DIP	107914285	41	MGL3
BPNGA16E	None	Yes	16-pin, Plastic SOJ	107914343	1041	NG
BPNGA16E-TR	None	Yes	Tape & Reel SOJ	107914350	1041	NG
BPNGA16G	None	Yes	16-pin, Plastic SOIC	107914368	1141	NG
BPNGA16G-TR	None	Yes	Tape & Reel SOIC	107914376	1141	NG
BPNGA16NB	None	Yes	Plastic SOIC/NB	107914384	1241	NG
BPNGA16NB-TR	None	Yes	Tape & Reel SOIC/NB	107914392	1241	NG
BPNGA16P	None	Yes	16-pin, Plastic DIP	107914400	41	NG
BPNPA16E	220 Ω	Yes	16-pin, Plastic SOJ	107914418	1041	NP
BPNPA16E-TR	220 Ω	Yes	Tape & Reel SOJ	107914426	1041	NP
BPNPA16G	220 Ω	Yes	16-pin, Plastic SOIC	107914434	1141	NP
BPNPA16G-TR	220 Ω	Yes	Tape & Reel SOIC	107914442	1141	NP
BPNPA16P	220 Ω	Yes	16-pin, Plastic DIP	107949745	41	NP
BPPGA16E	220 Ω	Yes	16-pin, Plastic SOJ	107949752	1041	PG
BPPGA16E-TR	220 Ω	Yes	Tape & Reel SOJ	107949760	1041	PG
BPPGA16G	220 Ω	Yes	16-pin, Plastic SOIC	107949778	1141	PG
BPPGA16G-TR	220 Ω	Yes	Tape & Reel SOIC	107949786	1141	PG
BPPGA16P	220 Ω	Yes	16-pin, Plastic DIP	107949794	41	PG

Notes

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January 1999
DS99-144HSI (Replaces DS99-044HSI)

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