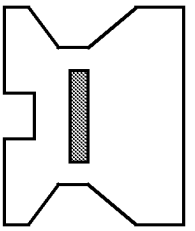
# LCD Segment / Common Driver with Controller
## CMOS

**MC141532**
**MC141533**

MC141532 / MC141533 is a CMOS LCD Driver which consists of 4 annunciator outputs and 153 high voltage LCD driving signals (33 commons and 120 segments). MC141532 is one sided common output while MC141533 is split common output design. It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has an on chip LCD bias Voltage Generator circuit such that fewer external components are required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30 to 85°C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 Bit Parallel Interface
- Graphic Mode Operation
- On Chip 120 x 33 Graphic Display Data RAM
- 120 Segment Drivers, 33 Common Drivers
- Selectable 1/16, 1/32, 1/33 Multiplex Ratio
- Selectable on Chip Voltage Doubler and Tripler
- Selectable 1:5 or 1:7 Bias Ratio
- Re-mapping of Row and Column Drivers
- Four Stand Alone Annunciator (Static Icon) Driver Circuits
- Low Power Icon Mode Driven by Com32 in Special Driving Scheme
- Selectable LCD Driving Voltage Temperature Coefficients
- 16 Level Internal Contrast Control
- External Contrast Control Provided
- Master Clear RAM
- Standard TAB, Gold Bump Die







**ORDERING INFORMATION**

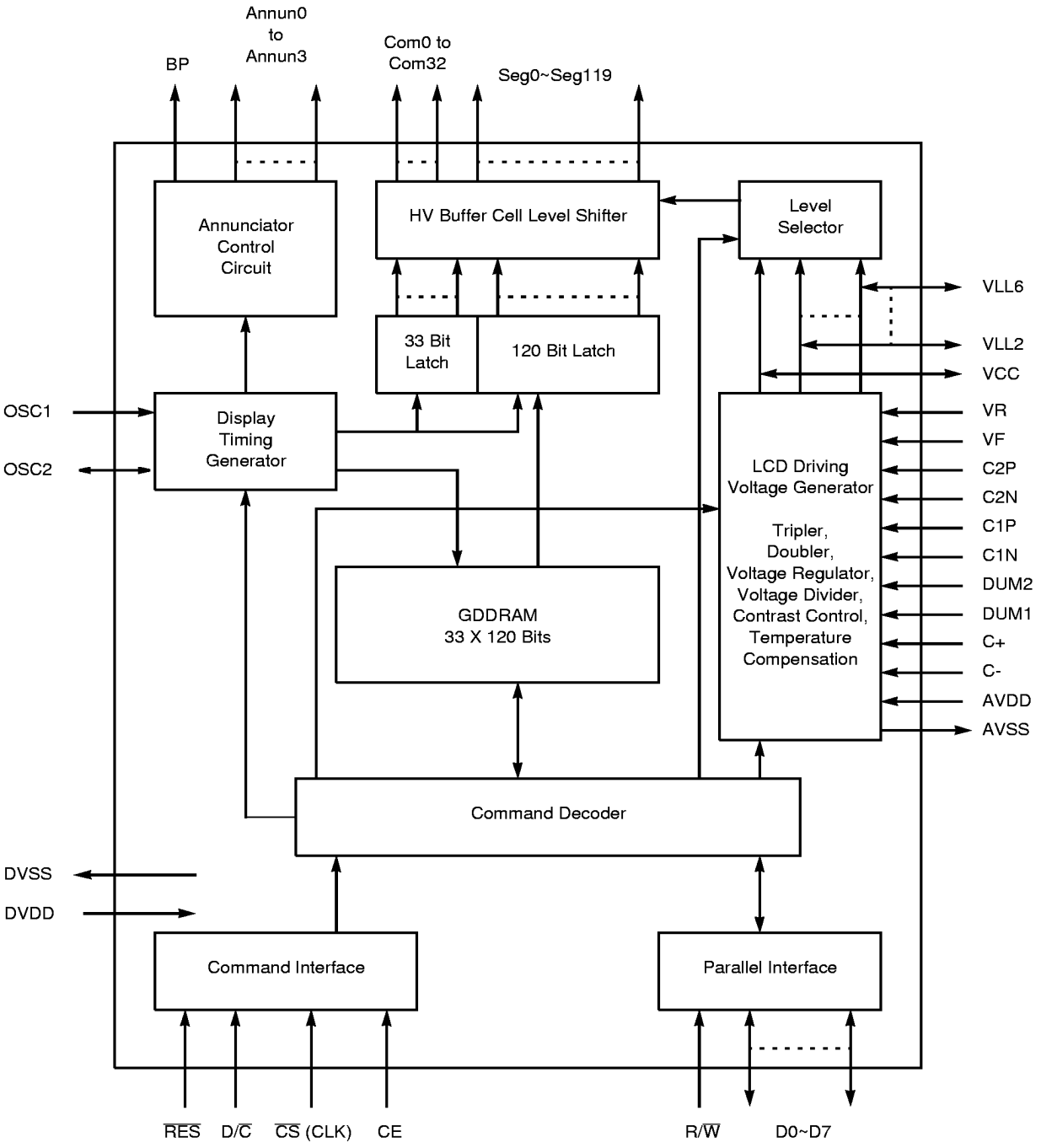
| | |
|---|---|
| MC141532T | TAB |
| MCC141532Z | Gold Bump Die |
| MCC141533Z | Gold Bump Die |

REV 12
2/98



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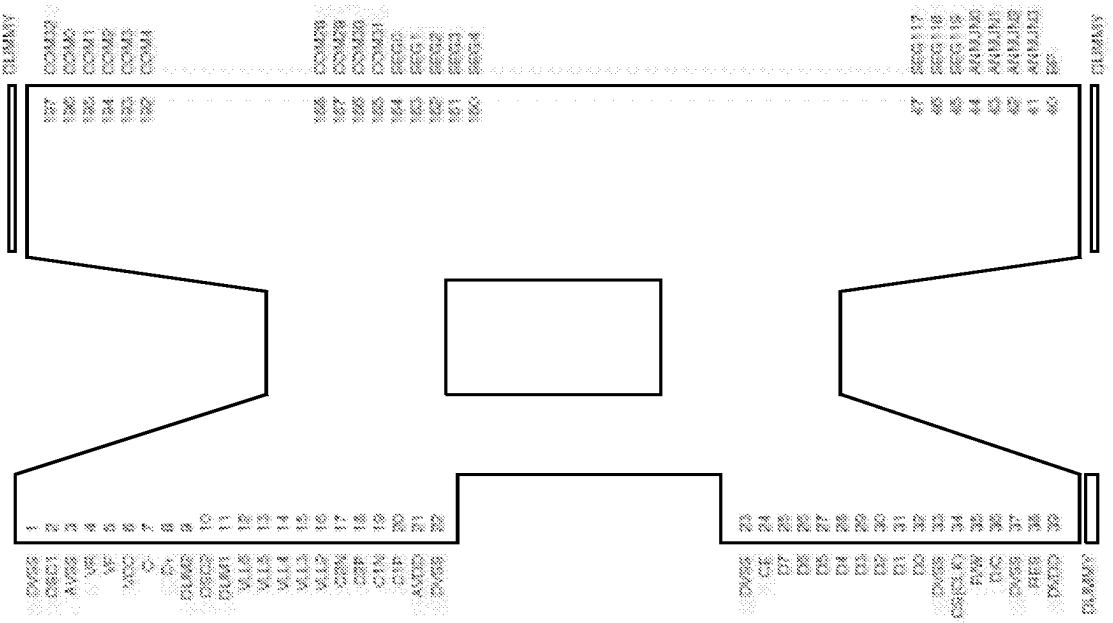
## Block Diagram







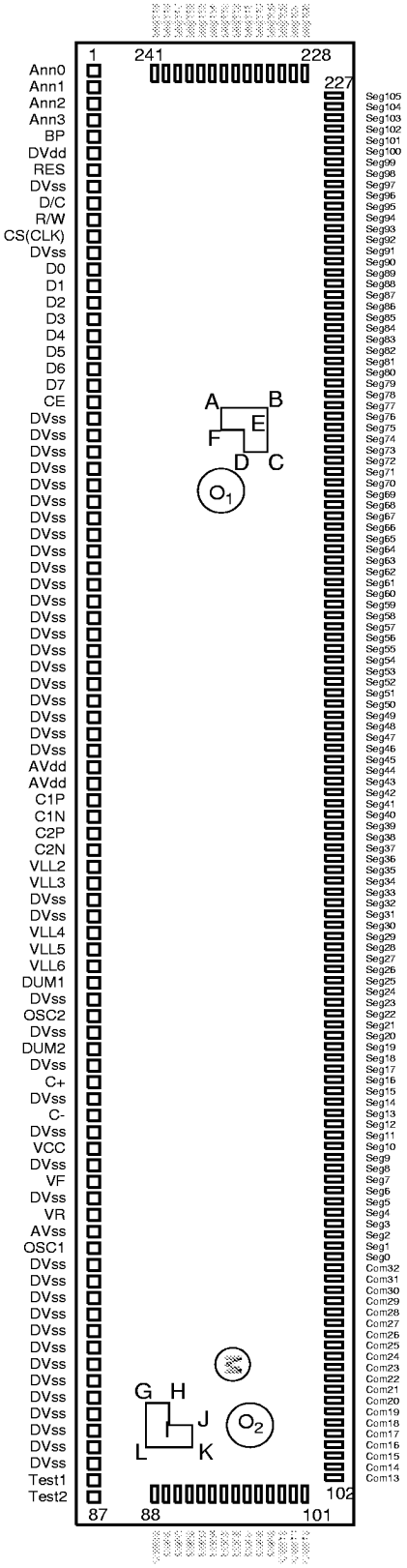
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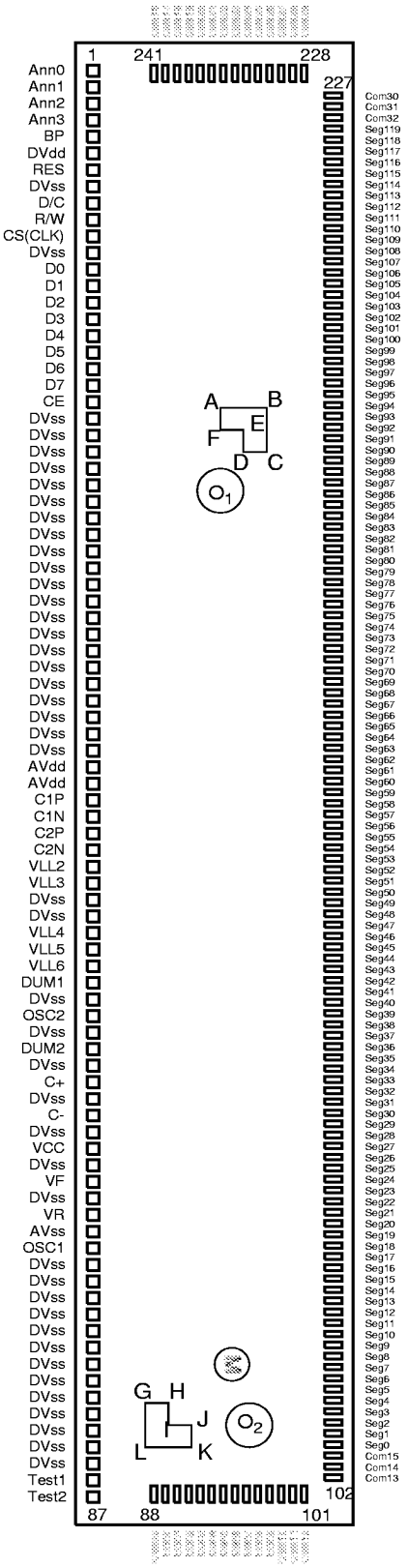
**MC141532T PIN ASSIGNMENT**
**(COPPER VIEW)**



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**MC141532 Die Pin Assignment**



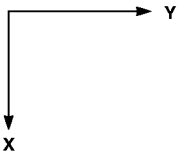

**MC141533 Die Pin Assignment**

## Alignment Mark Co-ordination

| | X (μm) | Y(μm) |
|---|---|---|
| A | -2625.2 | -78 |
| B | -2625.2 | 22 |
| C | -2525.2 | 22 |
| D | -2525.2 | -26 |
| E | -2575.2 | -26 |
| F | -2575.2 | -78 |
| $O_1$ | -2436.8 | -75.8 |
| G | 4360.2 | -186.7 |
| H | 4360.2 | -138.7 |
| I | 4410.2 | -138.7 |
| J | 4410.2 | -86.7 |
| K | 4460.2 | -86.7 |
| L | 4460.2 | -186.0 |
| $O_2$ | 4421.6 | 14.0 |
| d | 116 | |
| Keep out area 1* | -72.6 | 4802.2 |
| | 27.4 | 4802.2 |
| | 27.4 | 4702.2 |
| | -72.6 | 4702.2 |
| Keep out area 2* | 490.6 | 4866.2 |
| | 636.2 | 4867.2 |
| | 636.2 | 4824.8 |
| | 490.6 | 4674.6 |

$O_1$ and $O_2$ are the centers of the circular alignment marks which diameter is d.

* Areas not shown in the figure also with gold bumps






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**MAXIMUM RATINGS*** (Voltages Referenced to $V_{SS}$, $T_A$=25˚C)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $AV_{DD}$,$DV_{DD}$ | Supply Voltage | -0.3 to +4.0 | V |
| $V_{CC}$ | | $V_{SS}$-0.3 to $V_{SS}$+10.5 | V |
| $V_{in}$ | Input Voltage | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| I | Current Drain Per Pin Excluding $V_{DD}$ and $V_{SS}$ | 25 | mA |
| $T_A$ | Operating Temperature | -30 to +85 | ˚C |
| $T_{stg}$ | Storage Temperature Range | -65 to +150 | ˚C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
$V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ ($DV_{SS}$ = $V_{SS}$ of Digital circuit, $AV_{SS}$ = $V_{SS}$ of Analogue Circuit)
$V_{DD}$ = $AV_{DD}$ = $DV_{DD}$ ($DV_{DD}$ = $V_{DD}$ of Digital circuit, $AV_{DD}$ = $V_{DD}$ of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS}$ < or = ($V_{in}$ or $V_{out}$) < or = $V_{DD}$. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

**ELECTRICAL CHARACTERISTICS** (Voltage Referenced to $V_{SS}$, $T_A$=25˚C)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage (Absolute value Referenced to $V_{SS}$) | $AV_{DD}$ = $DV_{DD}$ | 2.4 | 3.15 | 3.5 | V |
| | Supply Current (Measure with $V_{DD}$ fixed at 3.15V) | | | | | |
| $I_{AC}$ | Access Mode Supply Current Drain from Pin AVDD and DVDD. | Internal DC/DC Converter On, Display On, Tripler Enable, R/W Accessing, $T_{cyc}$=1MHz, Osc. Freq.=50kHz, 1/33 Duty Cycle,1/7 Bias. | 0 | 200 | 300 | µA |
| $I_{DP1}$ | Display Mode Supply Current Drain from Pin AVDD and DVDD. | Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=50kHz, 1/33 Duty Cycle,1/7 Bias. | 0 | 80 | 150 | µA |
| $I_{DP2}$ | Display Mode Supply Current Drain from Pin AVDD and DVDD | Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz, 1/33 Duty Cycle,1/7 Bias. | 0 | 60 | 100 | µA |
| $I_{SB1}$ | Stand-by Mode Supply Current Drain from Pin AVDD and DVDD | Display Off, Oscillator Disabled, R/W Halt | 0 | 300 | 500 | nA |
| $I_{SB2}$ | Stand-by Mode Supply Current Drain from Pin AVDD and DVDD. | Display Off, Oscillator Enable, R/W Halt, External Oscillator and Frequency = 50kHz. | 0 | 2.5 | 5 | µA |
| $I_{SB3}$ | Stand-by Mode Supply Current Drain from Pin AVDD and DVDD. | Display Off, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 50kHz. | 0 | 5 | 10 | µA |
| $I_{ICON}$ | Stand-by Mode Supply Current Drain from Pin AVDD and DVDD | Low Power Icon Mode, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 50kHz | - | 15 | 25 | µA |
| | VLCD Voltage (Absolute Value Referenced to $V_{SS}$) | | | | | |
| $V_{CC1}$ | LCD Driving Voltage Generator Output Voltage at Pin $V_{CC}$. | Display On, Internal DC/DC Converter Enabled, Tripler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100µA | - | 3*$DV_{DD}$ | 10.5 | V |
| $V_{CC2}$ | LCD Driving Voltage Generator Output Voltage at Pin $V_{CC}$. | Display On, Internal DC/DC Converter Enabled, Doubler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100µA | - | 2*$DV_{DD}$ | 7 | V |
| $V_{LCD}$ | LCD Driving Voltage input at pin $V_{CC}$. | Internal DC/DC Converter Disabled. | 5 | - | 10.5 | V |
| | Output Voltage | | | | | |
| $V_{OH1}$ | Output High Voltage at Pins D0-D7, Annun0-3, BP and OSC2. | $I_{out}$=100µA | 0.8*$V_{DD}$ | - | $V_{DD}$ | V |
| $V_{OL1}$ | Output Low Voltage at Pins D0-D7, Annun0-3, BP and OSC2. | $I_{out}$=100µA | 0 | - | 0.2*$V_{DD}$ | V |
| $V_{R1}$ | LCD Driving Voltage Source at Pin VR | Regulator Enabled, $I_{out}$=50µA | 0 | - | $V_{CC}$ | V |
| $V_{R2}$ | LCD Driving Voltage Source at Pin VR | Regulator Disabled | - | Floating | - | V |
| | Input Voltage | | | | | |
| $V_{IH1}$ | Input High Voltage at Pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1 and OSC2. | | 0.8*$V_{DD}$ | - | $V_{DD}$ | V |
| $V_{IL1}$ | Input Low Voltage at Pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1 and OSC2. | | 0 | - | 0.2*$V_{DD}$ | V |



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**ELECTRICAL CHARACTERISTICS** (Voltage Referenced to $V_{SS}$, $DV_{DD}$=2.4-3.15V, $T_A$=25˚C)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | LCD Display Voltage. (LCD Driving Voltage Output from Pins VLL6, VLL5, VLL4, VLL3 and VLL2.) | 1/5 Bias Ratio, Voltage Divider Enabled, Regulator Enabled. | | | | |
| $V_{LL6}$ | | | - | $V_R$ | - | V |
| $V_{LL5}$ | | | - | 0.8*$V_R$ | - | V |
| $V_{LL4}$ | | | - | 0.6*$V_R$ | - | V |
| $V_{LL3}$ | | | - | 0.4*$V_R$ | - | V |
| $V_{LL2}$ | | | - | 0.2*$V_R$ | - | V |
| $V_{LL6}$ | | 1/7 Bias Ratio, Internal Voltage Divider Enabled, Regulator Enabled | - | $V_R$ | - | V |
| $V_{LL5}$ | | | - | 6/7*$V_R$ | - | V |
| $V_{LL4}$ | | | - | 5/7*$V_R$ | - | V |
| DUM2 | | | - | 4/7*$V_R$ | - | V |
| DUM1 | | | - | 3/7*$V_R$ | - | V |
| $V_{LL3}$ | | | - | 2/7*$V_R$ | - | V |
| $V_{LL2}$ | | | - | 1/7*$V_R$ | - | V |
| $V_{LL6}$ | | External Voltage Generator, Internal Voltage Divider Disable | 0.5$V_{CC}$ | - | $V_{CC}$ | V |
| $V_{LL5}$ | | | 0.5$V_{CC}$ | - | $V_{CC}$ | V |
| $V_{LL4}$ | | | 0.5$V_{CC}$ | - | $V_{CC}$ | V |
| $V_{LL3}$ | | | $V_{SS}$ | - | 0.5$V_{CC}$ | V |
| $V_{LL2}$ | | | $V_{SS}$ | - | 0.5$V_{CC}$ | V |
| | Output Current | | | | | |
| $I_{OH}$ | Output High Current Source from Pins D0-D7, Annun0-3, BP and OSC2 | $V_{out}$=$V_{DD}$-0.4V. | 100 | - | - | µA |
| $I_{OL}$ | Output Low Current Drain by Pins D0-D7, Annun0-3, BP and OSC2 | $V_{out}$=0.4V. | - | - | -100 | µA |
| $I_{OZ}$ | Output Tri-state Current Drain Source at pins D0-D7 and OSC2 | | -1 | - | 1 | µA |
| $I_{IL}$/$I_{IH}$ | Input Current at pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$ OSC1 and OSC2. | | -1 | - | 1 | µA |
| Ron | On Resistance<br>Channel Resistance between LCD Driving Signal Pins (SEG and COM) and Driving Voltage Input Pins ($V_{LL2}$ to $V_{LL6}$). | During Display on, 0.1V Apply between Two Terminals, $V_{CC}$ within Operating Voltage Range. | - | - | 10 | kΩ |
| $V_{SB}$ | Memory Retention Voltage ($DV_{DD}$)<br>Standby Mode, Retained All Internal Configuration and RAM Data | | 1.8 | - | - | V |
| $C_{IN}$ | Input Capacitance<br>All Control Pins | | - | 5 | 7.5 | pF |
| | Temperature Coefficient Compensation | | | | | |
| PTC0 | Flat Temperature Coefficient | TC1=0, TC2=0, Voltage Regulator Disabled. | - | 0.0 | - | % |
| PTC1 | Temperature Coefficient 1* | TC1=0, TC2=1, Voltage Regulator Enabled. | - | -0.18 | - | % |
| PTC2 | Temperature Coefficient 2* | TC1=1, TC2=0, Voltage Regulator Enabled. | - | -0.22 | - | % |
| PTC3 | Temperature Coefficient 3* | TC1=1, TC2=1, Voltage Regulator Enabled. | - | -0.35 | - | % |
| $V_{CN}$ | Internal Contrast Control<br>VR Output Voltage with Internal Contrast Control Selected. 16 Voltage Levels Controlled by Software. Each Level is Typical of 2.25% of the Regulator Output Voltage. | Internal Regulator Enabled, Internal Contrast Control Enabled. | - | ±18 | - | % |

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{VR \text{ at } 50^{\circ}C - VR \text{ at } 0^{\circ}C}{50^{\circ}C - 0^{\circ}C} \times \frac{1}{VR \text{ at } 25^{\circ}C} \times 100\%$$



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**ELECTRICAL CHARACTERISTICS** (Voltage Referenced to $V_{SS}$, $AV_{DD}$=$DV_{DD}$=2.4 to 3.5V, $T_A$=25˚C)

Total variation of VR $\Delta V_{RT}$ is affected by the following factors :

Process variation of Regulator $\Delta V_R$

External $V_{DD}$ Variation contributed to Regulator $\Delta V_{VDD}$

External resistor pair Ra/Rf contributed to Regulator $\Delta V_{res}$

where $\Delta V_{RT} = \sqrt{(\Delta V_R)^2 + (\Delta V_{V_{DD}})^2 + (\Delta V_{res})^2}$

Assume external $V_{DD}$ variation is ±6% at 3.15V and 1% variation resistor used at application

| | TC Level | $\Delta V_{VDD}$ (%) | $\Delta V_R$ (%) | $\Delta V_{res}$ (%) | $\Delta V_{RT}$ (%) |
|---|---|---|---|---|---|
| Reference Generator | TC0 | ±6.0 | ±2.5 | ±1.414 | ±6.652 |
| | TC1 | ±4.0 | | | ±4.924 |
| | TC2 | ±2.5 | | | ±3.805 |
| | TC3 | ±1.4 | | | ±3.195 |

**AC ELECTRICAL CHARACTERISTICS** ($T_A$=25˚C, Voltage referenced to $V_{SS}$, $V_{DD}$=2.4 to 3.15V)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Oscillation Frequency. | Set Clock Frequency to Slow | | | | |
| $F_{OSC1}$ | Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency. | | - | 38.4 | - | kHz |
| $F_{ANN1}$ | Annunciator Display (50% duty cycle) from Pins Annun0-3 and BP | | - | 18.75 | - | Hz |
| $F_{FRM1}$ | LCD Driving Signal Frame Frequency. | Either External Clock Input or Internal Oscillator Enable, Either 1/32 or 1/16 Duty Cycle, Graphic Display Mode. | - | 66 | - | Hz |
| $F_{CON1}$ | LCD Driving Signal Frame Frequency. | Either External Clock Input or Internal Oscillator Enable, 1/33 Duty Cycle, Graphic Display Mode. | - | 64 | - | Hz |
| | Oscillation Freq. | Set Clock Frequency to Normal | | | | |
| $Fosc_2$ | Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency. | | - | 50 | - | kHz |
| $F_{ANN2}$ | Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP | | - | 24.4 | - | Hz |
| $F_{FRM2}$ | LCD driving Signal Frame Frequency. | Either External Clock Input or Internal Oscillator Enable, Either 1/32 or 1/16 Duty Cycle. | - | 65 | - | Hz |
| $F_{CON2}$ | LCD driving Signal Frame Frequency. | Either External Clock Input or Internal Oscillator Enable, 1/33 Duty Cycle. | - | 63 | - | Hz |
| OSC | Internal Oscillation Frequency<br>Internal OSC Oscillation Frequency with Different Value of Feedback Resistor. | Internal Oscillator Enabled. $V_{DD}$ within Operation Range. | See Figure 1 for the relationship | | | |

Set Clock Frequency to Slow : $F_{FRM1}$=$F_{OSC1}$/576

Set Clock Frequency to Normal : $F_{FRM2}$=$F_{OSC2}$/768



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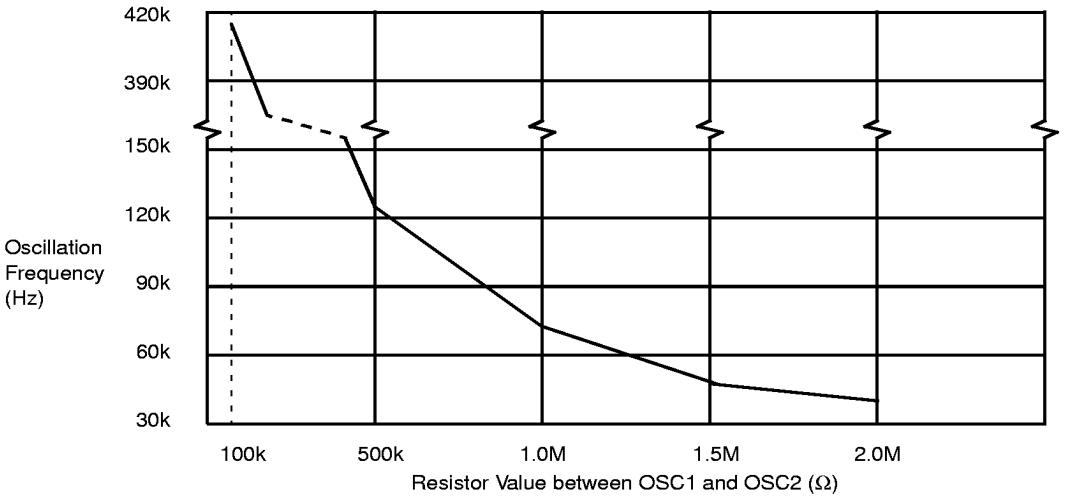



**Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value**

**AC OPERATION CONDITIONS AND CHARATERISTICS**

**ELECTRICAL CHARACTERISTICS** LCD Panel driving signal timing ($T_A$=-30 to 85˚C, $V_{DD}$ = 2.4 to 3.5V, $V_{SS}$ = 0V)

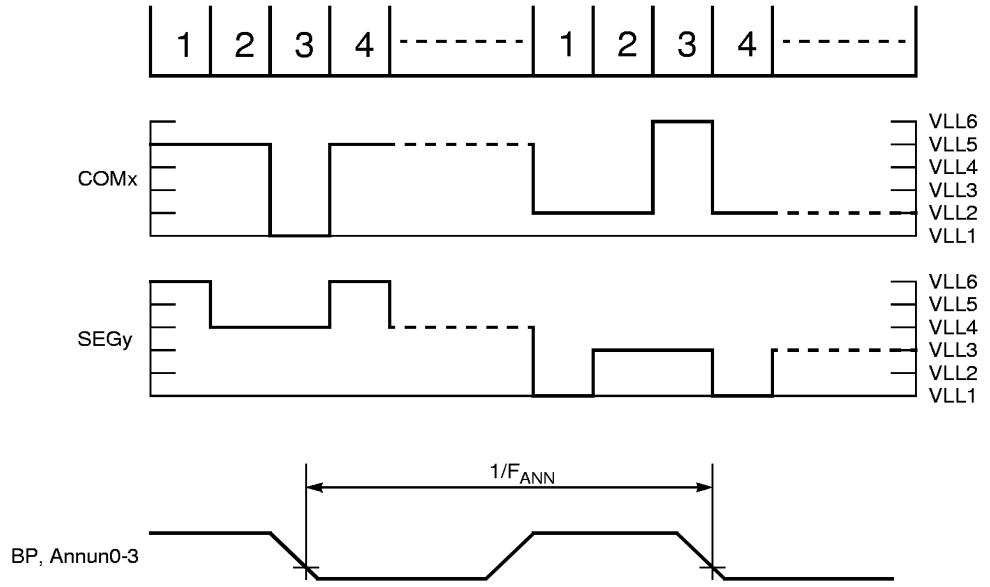



**Figure 2. LCD Driving Signal Timing Diagram**



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**TABLE 2a. Parallel Timing Characteristics (Write Cycle)** ($T_A$=-30 to 85˚C, $DV_{DD}$=2.4 to 3.5V, $V_{SS}$=0V)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Enable Cycle Time | 600 | - | - | ns |
| $t_{EH}$ | Enable Pulse Width | 290 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 5 | - | - | ns |
| $t_{DS}$ | Data Setup Time | 290 | - | - | ns |
| $t_{DH}$ | Data Hold Time | 20 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 20 | - | - | ns |

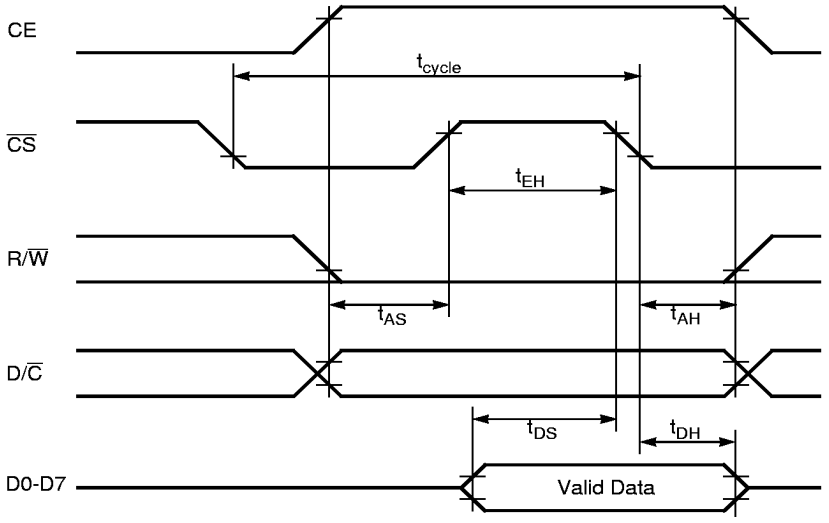



**Figure 3. Timing Characteristics (Write Cycle)**



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**TABLE 2b. Parallel Timing Characteristics (Read Cycle)** ($T_A$=-30 to 85˚C, $DV_{DD}$=2.4 to 3.5V, $V_{SS}$=0V)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Enable Cycle Time | 600 | - | - | ns |
| $t_{EH}$ | Enable Pulse Width | 290 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 5 | - | - | ns |
| $t_{DS}$ | Data Setup Time | - | - | 290 | ns |
| $t_{DH}$ | Data Hold Time | 10 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 20 | - | - | ns |

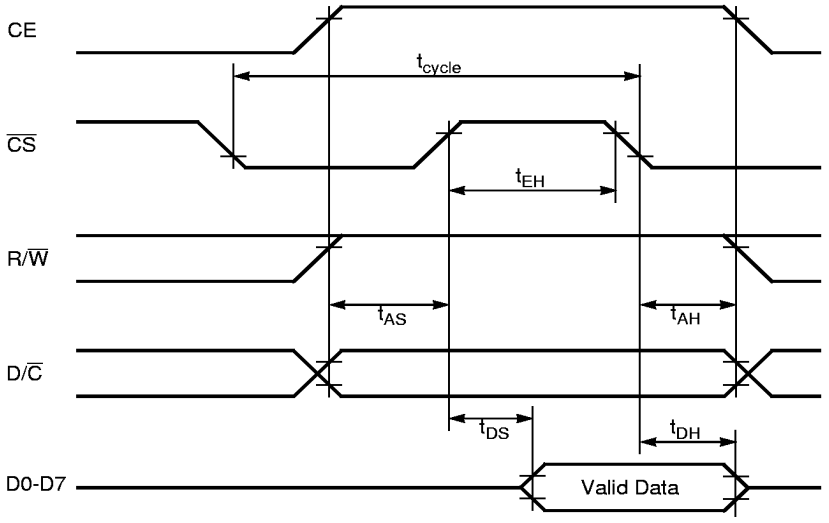



**Figure 4. Timing Characteristics (Read Cycle)**



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## PIN DESCRIPTIONS

**D/$\overline{C}$ (Data / Command)**
This input pin let the driver distinguish the input at D0-D7 is data or command. Input High for data while input Low for command.

**$\overline{CS}$ (CLK) (Chip Select / Input Clock)**
This pin is normal Low clock input. Data on D0-D7 is latched at the falling edge of $\overline{CS}$.

**$\overline{RES}$ (Reset)**
An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

**CE (Chip Enable)**
HIGH input to this pin to enable the control pins on the driver.

**D0-D7**
This bi-directional bus is used for data / command transferring.

**R/$\overline{W}$ (Read/Write)**
This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/W input Low indicates a write operation to the display data RAM or to the internal setup registers.

**OSC1 (Oscillator Input)**
For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

**OSC2 (Oscillator Output / External Oscillator Input)**
This is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

**VLL6 - VLL2**
Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal Voltage Divider enabled, a capacitor to $AV_{SS}$ is required on each pin.

**DUM1 and DUM2**
If internal Voltage Divider is enabled with 1/7 bias selected, a capacitor to $AV_{SS}$ is required on each pin. Otherwise, pull these two pin to $AV_{SS}$

**C1N and C1P**
If Internal DC/DC Converter is enabled, a capacitor is required to connect these two pins.

**C2N and C2P**
If internal Tripler is enabled, a capacitor is required between these two pins. Otherwise, leave these pin open.

**C+ and C-**
If internal divider circuit is enabled, a capacitor is required to connect between these two pins.

**VR and VF**
This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 µF capacitor placed between VR and AVSS. (Refer to the Application Circuit)

**COM0-COM32 (Row Drivers)**
These pins provide the row driving signal to LCD panel. Com0-Com31 are used in 32 mux configuration. Com0-Com15 are used in 16 mux and no row remap configuration while Com16-Com31 are used in 16 mux with row remap configuration. Com32 is used to drive the non-static icons in 33 Mux. They output 0V during display off. (Note : The IC facilitates two Com32 pins, which output same signal, for the LCD panel layout flexibility.)

**SEG0-SEG119 (Column Drivers)**
These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

**BP (Annunciator Backplane)**
This pin combines with Annun0-Annun3 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of $F_{ANNn}$ Hz. It outputs low when oscillator is disabled.

**Annun0 - Annun3 (Annunciator Frontplanes)**
These pins are four independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a $F_{ANNn}$ Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When oscillator is disabled, all these pins output 0V.

**AVDD and AVSS**
AVDD is the positive supply to the noise sensitive circuitry in LCD Driver and should be at same level as DVDD. AVSS is ground.

**VCC**
For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Positive power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

**DVDD and DVSS**
Power is supplied to the digital control circuit and other circuitry in LCD bias Voltage Generator of the driver using these two pins. DVDD is power and DVSS is ground.



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## OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

### Description of Block Diagram Module

**Command Decoder and Command Interface**

This module determines whether the input data is interpreted as data or command.

Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

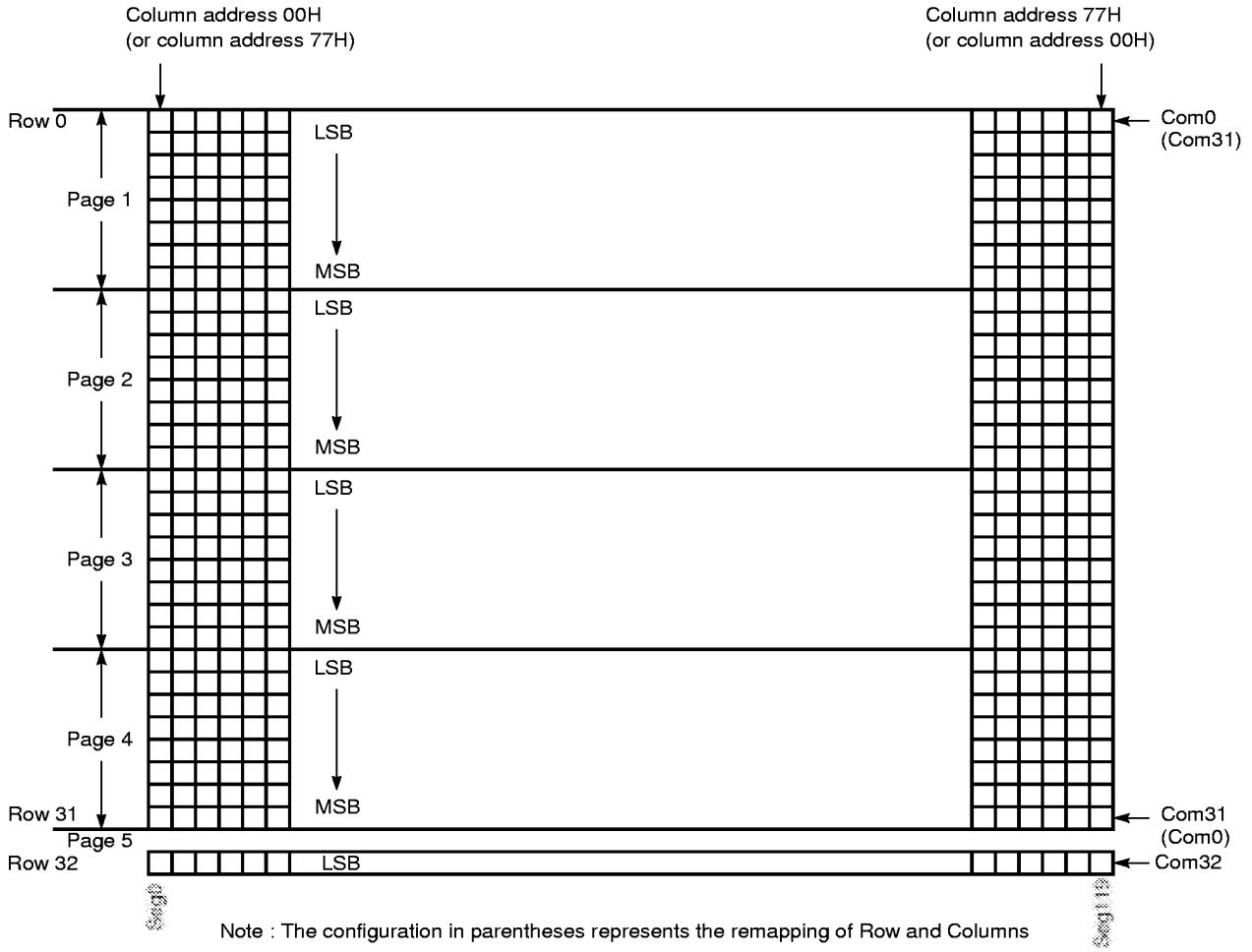
CE is the master chip selection signal. A High input enable the input lines ready to sample signals. Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

**MPU Parallel Interface**

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

**Graphic Display Data RAM (GDDRAM)**

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (120x33 = 3960 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.




Note : The configuration in parentheses represents the remapping of Row and Columns

**Figure 5. Graphic Display Data RAM (GDDRAM) Address Map**




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**Display Timing Generator**

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15 kHz to 50 kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

**Annunciator Control Circuit**

The LCD waveform of the 4 annunciators and BP are generated by this module. The 4 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit too. Annunciator output waveform shown in Figure 7.

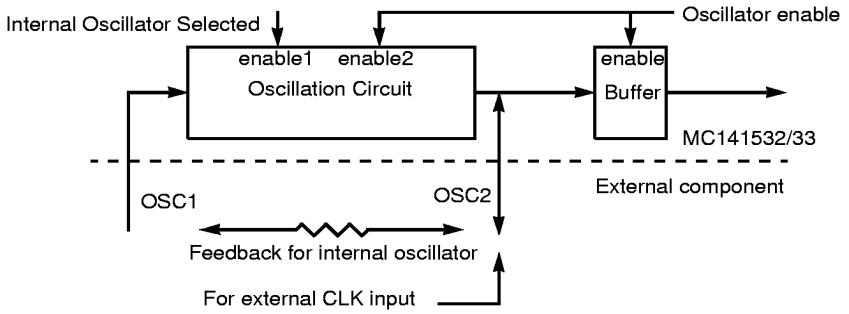



**Figure 6. Oscillator Circuitry**

**LCD Driving Voltage Generator**

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. it can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage ($V_{LL2}$-$V_{LL6}$) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Bias Ratio Selection circuitry
   Software control of 1/5 and 1/7 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
6. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.
7. External Contrast Control
   By adjusting the gain control resistors connected externally, the contrast can be varied. Refer to the application circuit for details.

   All blocks can be individually turned off if external voltage generator is employed.

## LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 7a, 7b and 7c illustrate the desired multiplex scheme.

**33 Bit Latch / 120 Bit Latch**

A 153 bit long register which carry the display signal information. First 33 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

**Level Selector**

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

**HV Buffer Cell (Level Shifter)**

HV Buffer Cell works as a level shift-er which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

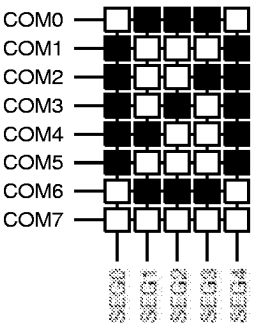



**Figure 7a. LCD Display Example "0"**



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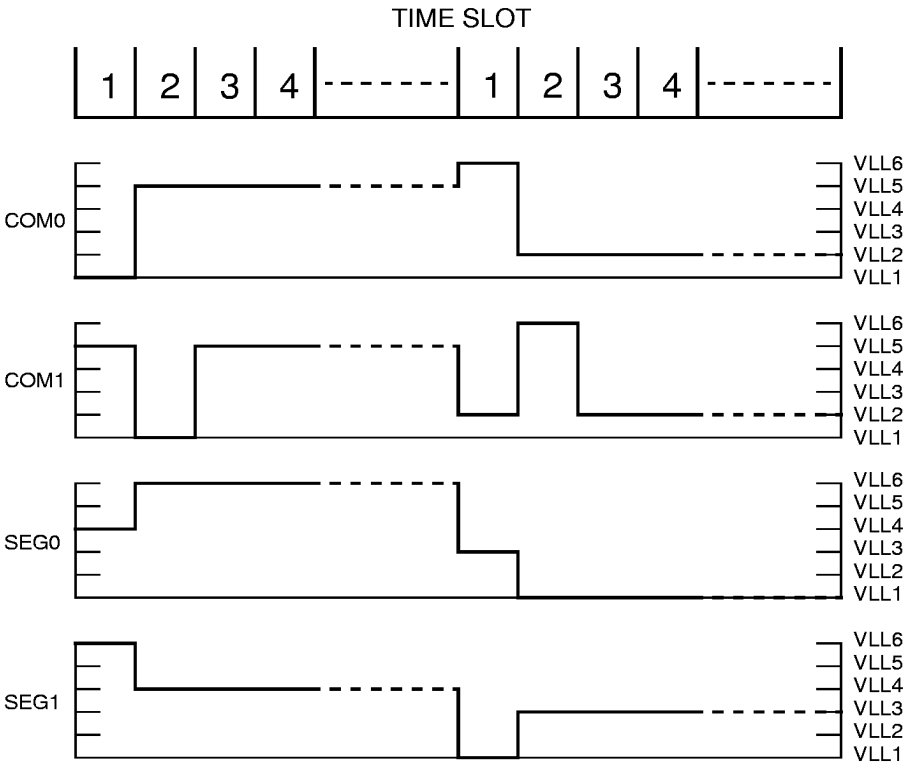



**Figure 7b. LCD Driving Signal from MC141532/33**

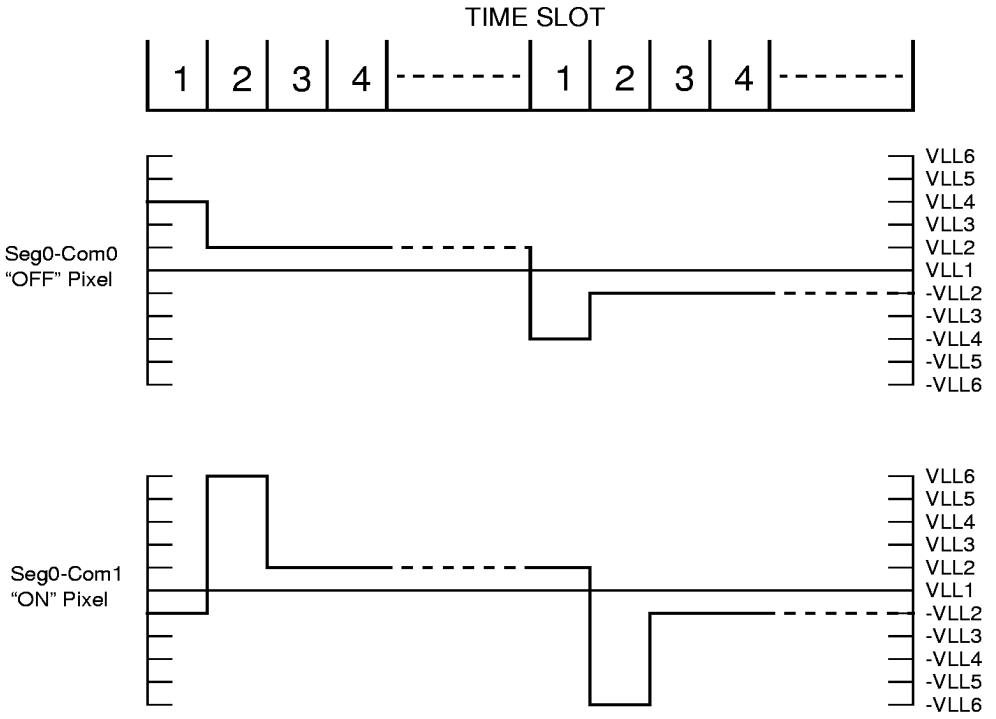



**Figure 7c. Effective LCD waveform on LCD pixel**



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## Command Description

**Set Display On/Off (Display Mode / Stand-by Mode)**

The Display On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command causes the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : "Oscillator On" command should be sent before "Display On" is selected)

The Display Off command turns the display off and the states of the LCD driver are as follow during display off :

1. The Common and Segment outputs are fixed at $V_{LL1}$ ($V_{SS}$).
2. The bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by Display Off command.

**Set GDDRAM Column Address**

This command positions the address pointer on a column location. The address can be set to location 00H-77H (120 columns). The column address will be increased by one automatically after a read or write operation. Refer to "Address Increment Table" and command "Set GDDRAM Page Address".

**Set GDDRAM Page Address**

This command positions the row address to 1 of 5 possible positions in GDDRAM. Refer to figure 5.

**Master Clear GDDRAM**

This command is to clear the 480 byte GDDRAM by setting the RAM data to zero. Issue this command followed by a dummy write command. The RAM for icon line will not be affected by this command.

**Master Clear Icons**

This command is used to clear the data in page 5 of GDDRAM which stores the icon line data. Before using this command, set the page address to Page 5 by the command "Set GDDRAM Page Address". A dummy write data is also needed after this "Master Clear Icons" command to make the clear icon action effective.

**Set Display with Icon Line**

If 1/32 Mux selected, use this command change to 1/33 Mux for using the Icon LIne. This command can also change Icon Display Mode to Normal Display Mode (1/32 or 1/33 MUX).

**Set Icon Display Mode**

This command force the output to the icon display mode. Display on Row 0 to Row 31 will be disabled.

**Set Icon Line / Annunciator Contrast Level**

The contrast of the icon line and annunciators in Icon Mode can be set by this command. There are four levels to select from.

**Set Vertical Scroll Value**

This command is used to scroll the screen vertically with scroll value 0 to 31. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 31 are mapped to Com1 through Com31 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 31 will be mapped to Com1 through Com30 respectively and Row 0 will be mapped to Com31. Com32 is not affected by this command.

**Save / Restore GDDRAM Column Address**

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

**Set Column Mapping**

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 119 of GDDRAM mapped to Seg0-Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119-Seg0 respectively.

Com32 will not be affected by this command. Detailed information please refer to section "Display Output Description".

**Set Row Mapping**

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 31 of GDDRAM to Com0 - Com31 respectively;
2. Row 0 - Row 31 of GDDRAM to Com31 - Com0 respectively.

Com32 will not be affected by this command. See section "Display Output Description" for related information.

**Set Annunciator Control Signals**

This command is used to control the active states of the 4 stand alone annunciator drivers.

**Set Oscillator Disable / Enable**

This command is used to either disable or enable the Oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command "Set Display On/Off" and "Set Annunciator Control Signal". See command "Set Internal / External Oscillator" for more information

**Set Internal / External Oscillator**

This command is used to select either internal or external oscillator. When Internal Oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

**Set Clock Frequency**

Use this command to choose from two different oscillation frequency (50kHz or 38.4kHz) to get the 60 Hz frame frequency. With frequency high, 50 kHz clock frequency is preferred. 38.4kHz clock frequency (low frequency) enable for power saving purpose.

**Set DC/DC Converter On/Off**

Use this command selects the Internal DC/DC Converter to generate the $V_{CC}$ from $AV_{DD}$. Disable the Internal DC/DC Converter if external Vcc is provided.

**Set Voltage Doubler / Tripler**

Use this command to choose Doubler or Tripler when the Internal DC/DC Converter is enabled.

**Set Internal Regulator On/Off**

Choose bit option 0 to disable the Internal Regulator. Choose bit option 1 to enable Internal Regulator which consists of the internal contrast control and temperature compensation circuits.



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**Set Internal Voltage Divider On/Off**

If the Internal Voltage Divider is disabled, external bias can be used for $V_{LL6}$ to $V_{LL2}$. If the Internal Voltage Divider is enabled, the internal circuit will automatically select the correct bias level according to the number of multiplex. Refer to command "Bias Ratio Select".

**Set Duty Cycle**

This command is to select 16 mux or 32 mux display. When 16 mux is enabled, the unused 16 common outputs will be swinging between VLL2 and VLL5 for dummy scan purpose and doubler will be used.

**Set Bias Ratio**

This command sets the 1/5 bias or 1/7 bias for the divider output. The selection should match the characteristic of LCD Panel.

**Set Internal Contrast Control On/Off**

This command is used to turn on or off the intrernal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

**Increase / Decrease Contrast Level**

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after POR.

**Set Contrast Level**

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use.

**Read Contrast Value**

This command allows the user to read the current contrast level value. With R/$\overline{W}$ input high (READ), D/$\overline{C}$ input low (COMMAND) and D7 D6 D5 D4 are equal to 0 0 0 1, the value of the internal contrast value can be read on D0-D3 at the falling edge of CS.

**Set Temperature Coefficient**

This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

**Set $I_{DD}$ Reduction Mode On/Off**

By using this command to reduce the display clock frequency by half. Use in Icon Mode to reduce stand-by current.



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**COMMAND TABLE**

| Bit Pattern | Command | Comment |
|---|---|---|
| $00000X_2X_1X_0$ | Set GDDRAM Page Address | Set GDDRAM Page Address using $X_2X_1X_0$ as address bits.<br>$X_2X_1X_0$=000 : page 1 (POR)<br>$X_2X_1X_0$=001 : page 2<br>$X_2X_1X_0$=010 : page 3<br>$X_2X_1X_0$=011 : page 4<br>$X_2X_1X_0$=100 : page 5 |
| $000011X_1X_0$ | Set Icon Line / Annunciator Contrast Level | Set one of the 4 available values to the icon and annunciator contrast, using $X_1X_0$ as data bits.<br>$X_1X_0$=00 (Von = $0.87V_{DD}$)<br>$X_1X_0$=01 (Von = $0.71V_{DD}$)<br>$X_1X_0$=10 (Von = $0.61V_{DD}$) POR<br>$X_1X_0$=11 (Von = $0.55V_{DD}$) |
| $0001X_3X_2X_1X_0$ | Set Contrast Level | Set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR. |
| $0001X_3X_2X_1X_0$ | Read Contrast Value | With D/$\overline{C}$ pin input Low, R/$\overline{W}$ pin input high, and D7 D6 D5 D4 pins equal to 0001 at the rising edge of $\overline{CS}$, the value of the internal contrast register will be latched out at D3 D2 D1 D0 pins, i.e. $X_3X_2X_1X_0$, at the rising edge of $\overline{CS}$. |
| $0010000X_0$ | Set Voltage Doubler / Tripler | $X_0$=0: Select Voltage Tripler (POR)<br>$X_0$=1: Select Voltage Doubler |
| $0010001X_0$ | Set Column Mapping | $X_0$=0 : Col0 to Seg0 (POR)<br>$X_0$=1 : Col0 to Seg119 |
| $0010010X_0$ | Set Row Mapping | $X_0$=0 : Row0 to Com0 (POR)<br>$X_0$=1: Row0 to Com31 |
| $0010011X_0$ | Reserved | |
| $0010100X_0$ | Set Display On/Off | $X_0$=0: display off (POR)<br>$X_0$=1: display on |
| $0010101X_0$ | Set DC/DC Converter On/Off | $X_0$=0: DC/DC Converter off (POR)<br>$X_0$=1: DC/DC Converter on |
| $0010110X_0$ | Set Internal Regulator On/Off | $X_0$=0: Internal Regulator off (POR)<br>$X_0$=1: Internal Regulator on<br>When the application employs external contrast control, the internal contrast control, temperature compensation and the Regulator must be enabled. |
| $0010111X_0$ | Set Internal Voltage Divider On/Off | $X_0$=0: Internal Voltage Divider off (POR)<br>$X_0$=1: Internal Voltage Divider on<br>When an external bias network is preferred, the voltage divider should be disabled. |
| $0011000X_0$ | Set Internal Contrast Control On/Off | $X_0$=0: Internal Contrast Control off (POR)<br>$X_0$=1: Internal Contrast Control on<br>Internal contrast circuits can be disabled if external contrast circuits is preferred. |
| $0011001X_0$ | Set Clock Frequency | $X_0$=0 : low frequency (38.4kHz) (POR)<br>$X_0$=1 : high frequency (50kHz) |
| $0011010X_0$ | Save/Restore GDDRAM Column Address | $X_0$=0 : restore address<br>$X_0$=1 : save address |
| 00110110 | Master Clear GDDRAM | Master clear GDDRAM page 1 to 4 |
| 00110111 | Master Clear Icons | Master Clear of GDDRAM page 5.<br>GDDRAM page 5 should be selected and dummy write is required |
| $0011100X_0$ | Set Bias Ratio | $X_0$=0: set 1/7 bias (POR)<br>$X_0$=1: set 1/5 bias |
| $0011101X_0$ | Reserved. | $X_0$=0: normal operation (POR)<br>$X_0$=1: test mode<br>(Note: Make sure to set $X_0$=0 during application) |



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| Bit Pattern | Command | Comment |
|---|---|---|
| $0011110X_0$ | Set Display with Icon Line | $X_0$=0: set display mode without Icon Line<br>$X_0$=1: set display mode with Icon Line |
| 00111110 | Set Icon Display Mode | Power saving icon display mode, Com0 to Com31 will be disabled |
| $010X_4X_3X_2X_1X_0$ | Set Vertical Scroll Value | Use $X_4X_3X_2X_1X_0$ as number of lines to scroll.<br>Scroll value = 0 upon POR |
| $01100A_1A_0X_0$ | Set Annunciator Control Signals | $A_1A_0$=00: select annunciator 1 (POR)<br>$A_1A_0$=01: select annunciator 2<br>$A_1A_0$=10: select annunciator 3<br>$A_1A_0$=11: select annunciator 4<br>$X_0$=0: turn selected annunciator off (POR)<br>$X_0$=1: turn selected annunciator on |
| $0110100X_0$ | Set Duty Cycle | $X_0$=0: 1/32 duty and tripler enabled (POR)<br>$X_0$=1: 1/16 duty and doubler enabled |
| $0110101X_0$ | Set $I_{DD}$ Reduction Mode | $X_0$=0: Normal Mode<br>$X_0$=1: $I_{DD}$ Reduction Mode |
| $011011X_1X_0$ | Set Temperature Coefficient | $X_1X_0$=00 : 0.00% (POR)<br>$X_1X_0$=01 : -0.18%<br>$X_1X_0$=10 : -0.22%<br>$X_1X_0$=11 : -0.35% |
| $0111000X_0$ | Increase / Decrease Contrast Value | $X_0$=0: Decrease by one level<br>$X_0$=1: Increase by one level<br>(Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR. |
| $0111001X_0$ | Reserved | |
| $0111010X_0$ | Reserved | |
| $0111011X_0$ | Reserved | $X_0$=0: normal operation (POR)<br>$X_0$=1: test mode select<br>(Note: Make sure to set $X_0$=0 during application) |
| $0111100X_0$ | Reserved | |
| $0111101X_0$ | Set Internal / External Oscillator | $X_0$=0: Internal oscillator (POR)<br>$X_0$=1: External oscillator.<br>Internal oscillator circuit is automatically enabled if resistors are placed at OSC1 and OSC2. For external oscillator, simply feed clock in OSC2. |
| $0111110X_0$ | Reserved | |
| $0111111X_0$ | Set Oscillator Disable / Enable | $X_0$=0: oscillator disable (POR)<br>$X_0$=1: oscillator enable.<br>This is the master control fro oscillator circuitry. This command should be issued after the “External / Internal Oscillator” command. |
| $1X_6X_5X_4X_3X_2X_1X_0$ | Set GDDRAM Column Address | Set GDDRAM Column Address.<br>Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits. |

**Data Read / Write**

To read data from the GDDRAM, input High to R/$\overline{W}$ pin and D/$\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to R/$\overline{W}$ pin and High to D/$\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the “Commands Required for R/W Actions on RAM” Table)



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### Address Increment Table (Automatic)

| D/$\overline{C}$ | R/$\overline{W}$ | Comment | Address Increment | Remarks |
|---|---|---|---|---|
| 0 | 0 | Write Command | No | |
| 0 | 1 | Read Command | No | *1 |
| 1 | 0 | Write Data | Yes | *2 |
| 1 | 1 | Read Data | Yes | |

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.

Remarks : *1. Refer to the command "Read Contrast Value".
*2. If write data is issued after Command Clear RAM, Address increase is not applied.
*3. Column Address will be wrapped round when overflow.

### Power Up Sequence (Commands Required)

| Command Required | POR Status | Remarks |
|---|---|---|
| Set Clock Frequency | Low | *1 |
| Set Oscillator Enable | Disable | *1 |
| Set Annunciator Control Signals | Annunciator all Off | *1 |
| Set Duty Cycle | 1/32 duty | *1 |
| Set Bias Ratio | 1/7 bias | *1 |
| Set Interna DC/DC Converter On | Off | *1 |
| Set Internal Regulator On | Off | *1 |
| Set Temperature Coefficient | TC=0% | *1, *3 |
| Set Internal Contrast Control On | Off | *1, *3 |
| Increase Contrast Level | Contrast Level = 0 | *1, *2, *3 |
| Set Internal Voltage Divider On | Off | *1 |
| Set Segment Mapping | Seg. 0 = Col. 0 | |
| Set Common Mapping | Com. 0 = Row 0 | |
| Set Vertical Scroll Value | Scroll Value = 0 | |
| Set Display On | Off | |

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

### Commands Required for Display Mode Setup

| Display Mode | Commands Required | |
|---|---|---|
| Display Mode | Set External / Internal Oscillator,<br>Set Oscillator Enable,<br>Set Display On. | $(0111101X_0)$*<br>(01111111)*<br>(00101001)* |
| Annunciator Display | Set External / Internal Oscillator,<br>Set Oscillator Enable,<br>Set Annunciator Control Signal. | $(0111101X_0)$*<br>(01111111)*<br>$(01100A_1A_0X_0)$* |
| Standby Mode 1. | Set Display Off,<br>Set Oscillator Disable. | (00101000)*<br>(01111110)* |
| Standby Mode 2. | Set External Oscillator,<br>Set Annunciator Control Signal,<br>Set Display Off,<br>Set Oscillator Enable. | (01111011)*<br>$(01100A_1A_0X_0)$*<br>(00101000)*<br>(01111111)* |
| Standby Mode 3. | Set Internal Oscillator,<br>Set Annunciator Control Signal,<br>Set Display Off,<br>Set Oscillator Enable. | (01111010)*<br>$(01100A_1A_0X_0)$*<br>(00101000)*<br>(01111111)* |

Other Related Command with Display Mode : Set Duty Cycle, Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

Commands Related to Internal DC/DC Converter :
Set Oscillator Disable / Enable, Set Internal Regulator On/Off, Set Duty Cycle, Set Temperature Coefficient, Set Internal Contrast Control On/Off, Increase / Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Bias Ratio, Set Display On/Off, Set Internal / External Oscillator, Set Contrast Level, Set Voltage Doubler / Tripler, Set 33 Mux Display Mode, Set Icon Display Mode

* No need to resend the command again if it is set previously.



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**Commands Required for R/W Actions on RAM**

| R/W Actions on RAMs | Commands Required | |
|---|---|---|
| Read/Write Data from/to GDDRAM. | Set GDDRAM Page Address<br>Set GDDRAM Column Address<br>Read/Write Data | $(000X_4X_3X_2X_1X_0)$*<br>$(1X_6X_5X_4X_3X_2X_1X_0)$*<br>$(X_7X_6X_5X_4X_3X_2X_1X_0)$ |
| Save/Restore GDDRAM Column Address. | Save/Restore GDDRAM Column Address. | $(0011010X_0)$ |
| Increase GDDRAM Address by One | Dummy Read Data | $(X_7X_6X_5X_4X_3X_2X_1X_0)$ |
| Master Clear GDDRAM | Master Clear GDDRAM<br>Dummy Write Data | (00110110)<br>$(X_7X_6X_5X_4X_3X_2X_1X_0)$ |

* No need to resend the command again if it is set previously.

**Display Output Description**

This is an example of output pattern on the LCD panel. Figure 8b and 8c are data map of GDDRAM and the output pattern on the LCD display with different command enabled.

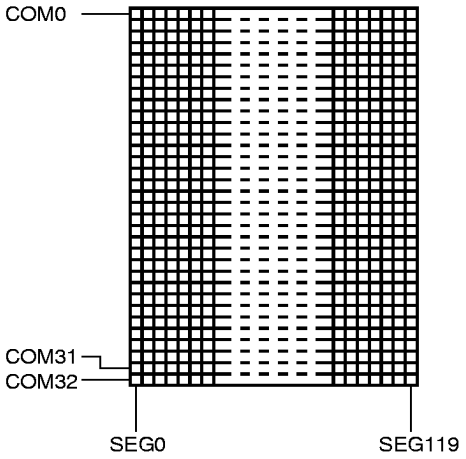



Figure 8a

| | | Content of GDDRAM |
|---|---|---|
| PAGE 1 | Upper Nibble | 5 A 5 A 5 A 5 A - - - - - - - - - - 5 A 5 A 5 A 5 A 5 A |
| | Lower Nibble | 5 A 5 A 5 A 5 A - - - - - - - - - - 5 A 5 A 5 A 5 A 5 A |
| PAGE 2 | Upper Nibble | 3 3 C C 3 3 C C 3 3 - - - - - - - - - - C C 3 3 C C 3 3 C C |
| | Lower Nibble | 3 3 C C 3 3 C C 3 3 - - - - - - - - - - C C 3 3 C C 3 3 C C |
| PAGE 3 | Upper Nibble | 0 0 0 0 F F F F 0 0 - - - - - - - - - - F F 0 0 0 0 F F F F |
| | Lower Nibble | F F F F 0 0 0 0 F F - - - - - - - - - - 0 0 F F F F 0 0 0 0 |
| PAGE 4 | Upper Nibble | F F F F F F F F 0 0 - - - - - - - - - - F F 0 0 0 0 0 0 0 0 |
| | Lower Nibble | F F F F F F F F 0 0 - - - - - - - - - - F F 0 0 0 0 0 0 0 0 |
| PAGE 5 | Upper Nibble | 0 0 0 0 0 0 0 0 0 0 - - - - - - - - - - 0 0 0 0 0 0 0 0 0 0 |
| | Lower Nibble | 0 0 0 1 1 1 0 0 0 0 - - - - - - - - - - 0 0 0 0 1 1 1 0 0 0 |

Figure 8b

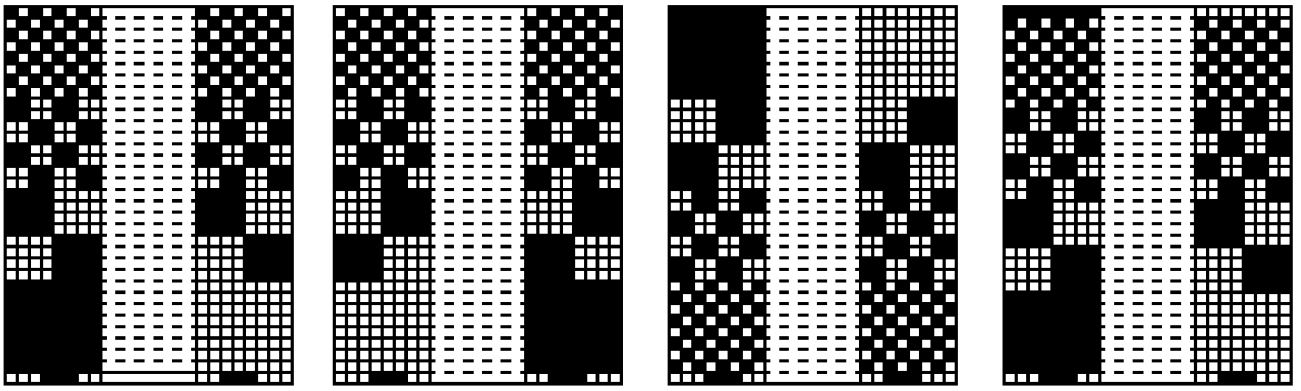
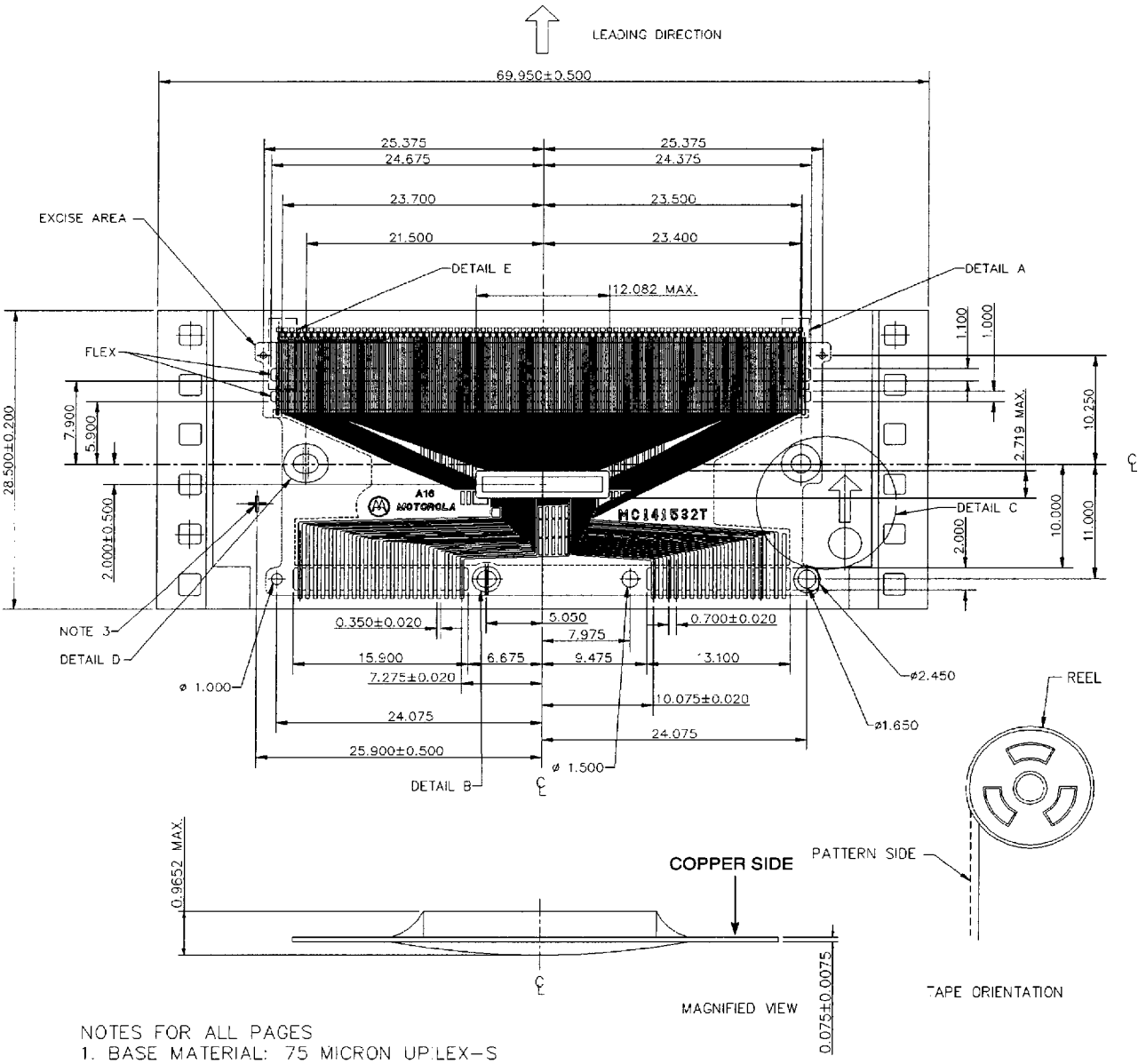



**Figure 8c. Examples of LCD display with different command enabled**




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**MC141532T TAB PACKAGE DIMENSION (1 OF 2)**
**98ASL00243A ISSUE A**
**DO NOT SCALE THIS DRAWING**



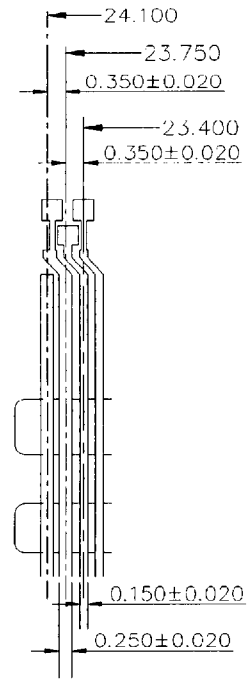

NOTES FOR ALL PAGES
1. BASE MATERIAL: 75 MICRON UPILEX-S
2. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
3. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.
4. IF NOT SPECIFIED, SIZE IN MILLIMETER
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. 6 SPROCKET HOLES DEVICE
7. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05



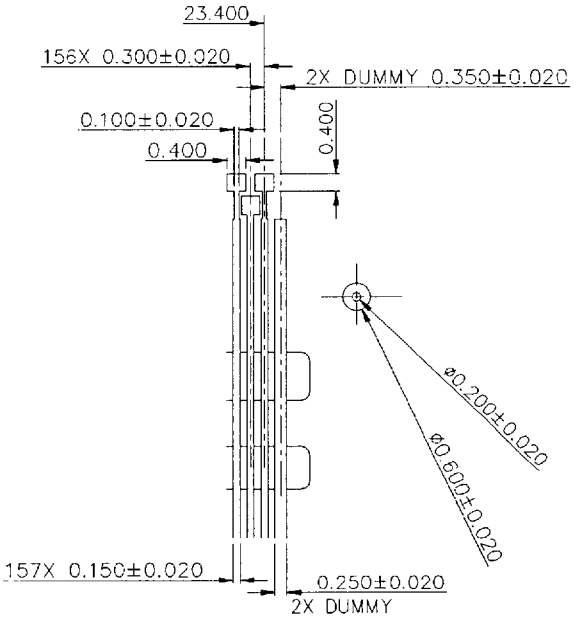

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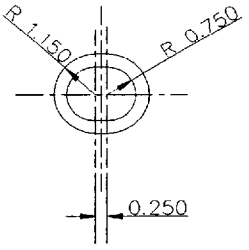
**MC141532T TAB PACKAGE DIMENSION (2 OF 2)**
**98ASL00243A ISSUE A**
**DO NOT SCALE THIS DRAWING**



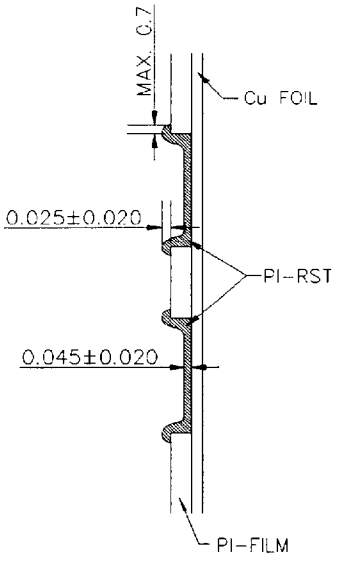

DETAIL E



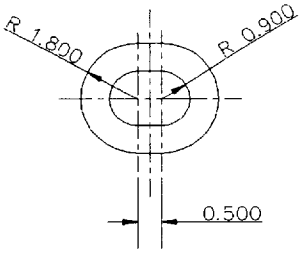

DETAIL A



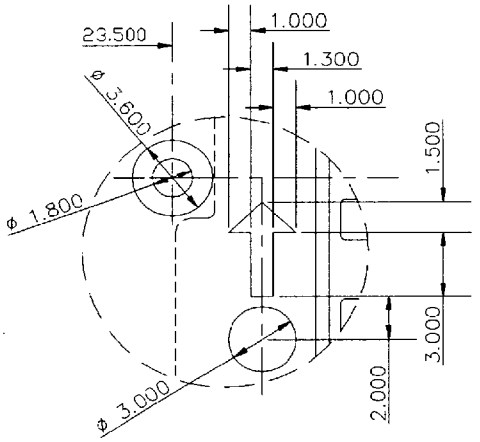

DETAIL B




FLEX MATERIAL DETAIL




DETAIL D




DETAIL C

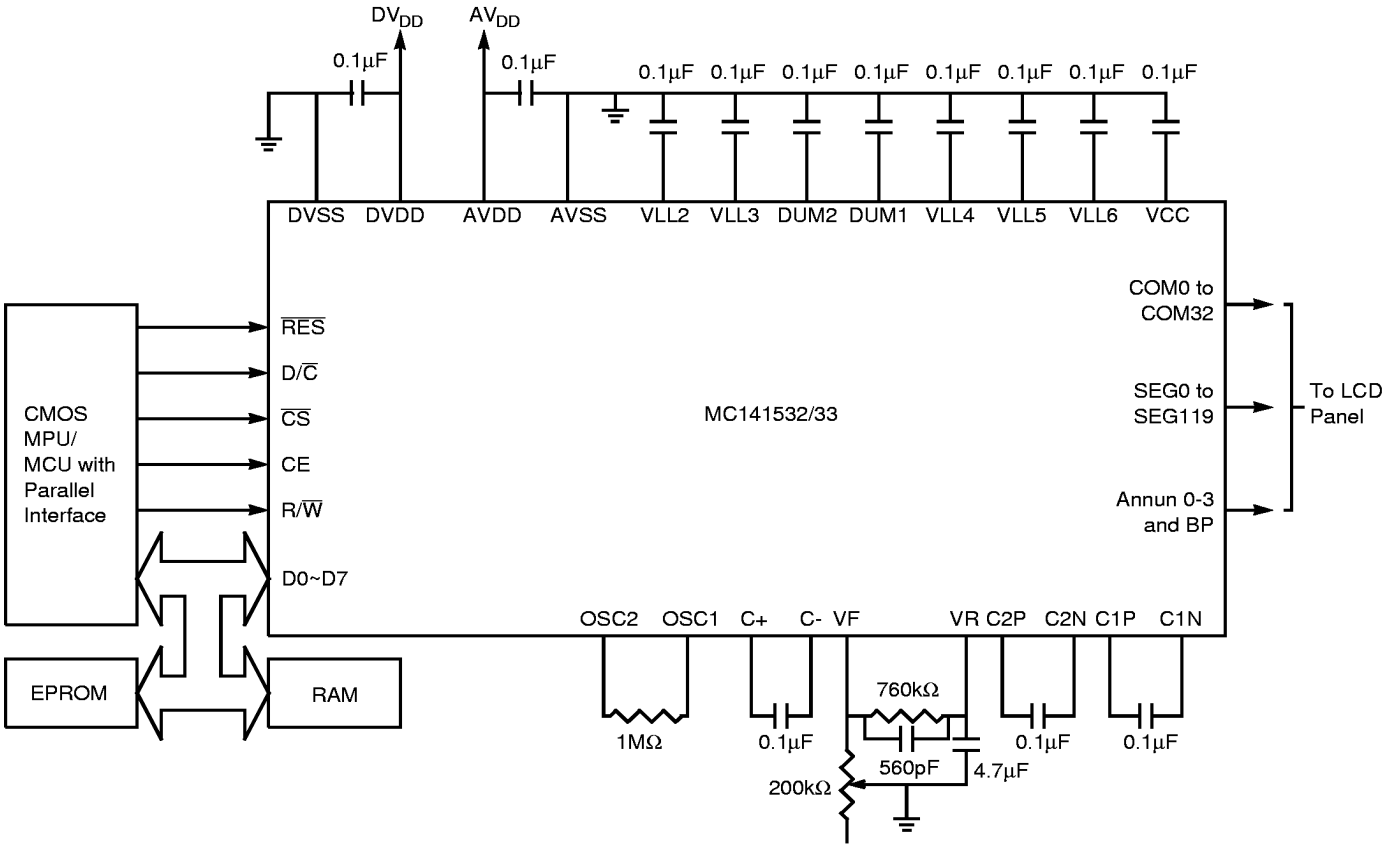


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**Application Circuit**

**32/33 MUX Display with Analog Circuitry enabled, Tripler enabled and 1/7 bias**



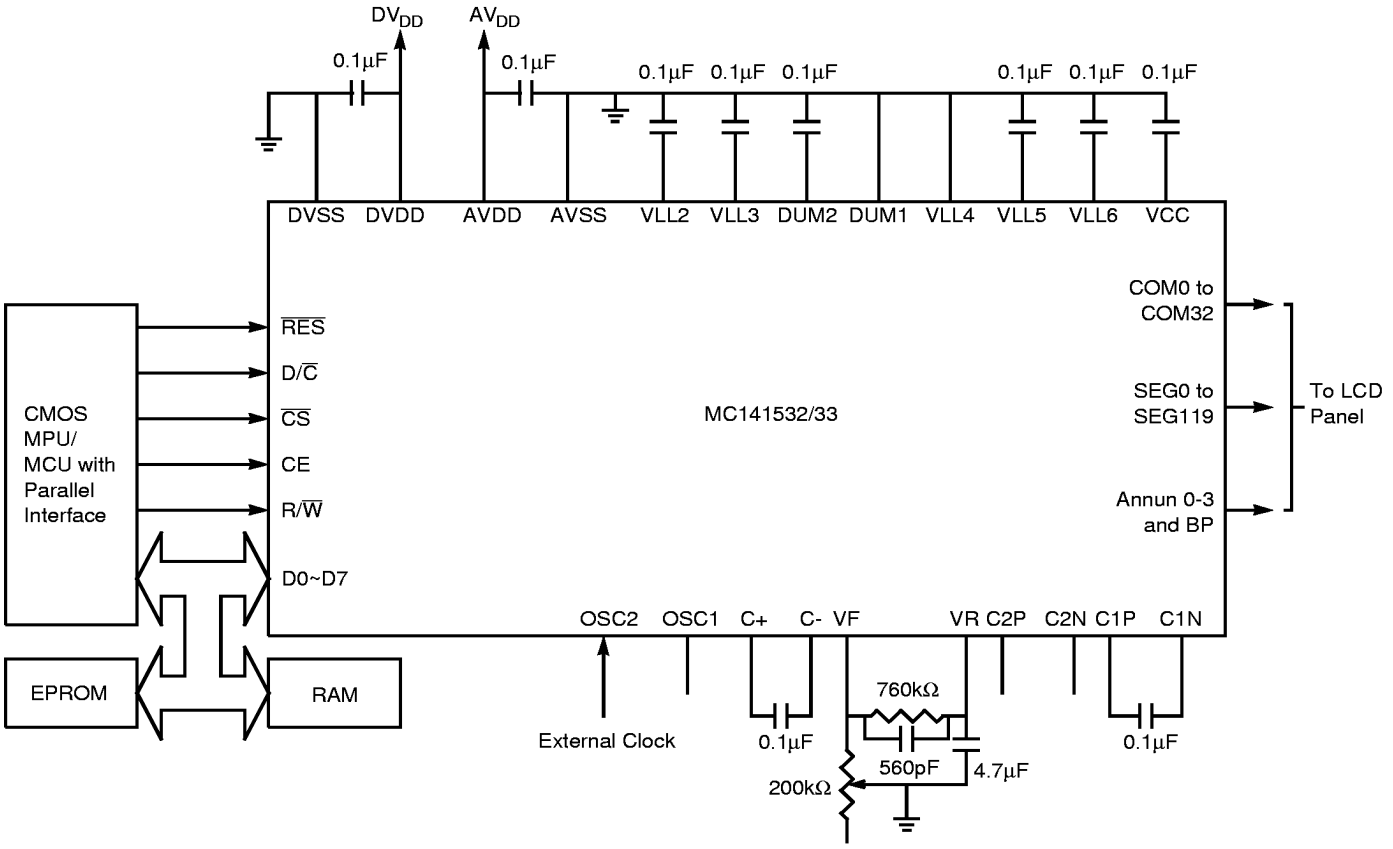

Remark :
1. VR and VF can be left open for Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.



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**Application Circuit**

**16 MUX Display with Analog Circuitry enabled, Tripler Disabled and 1/5 bias**



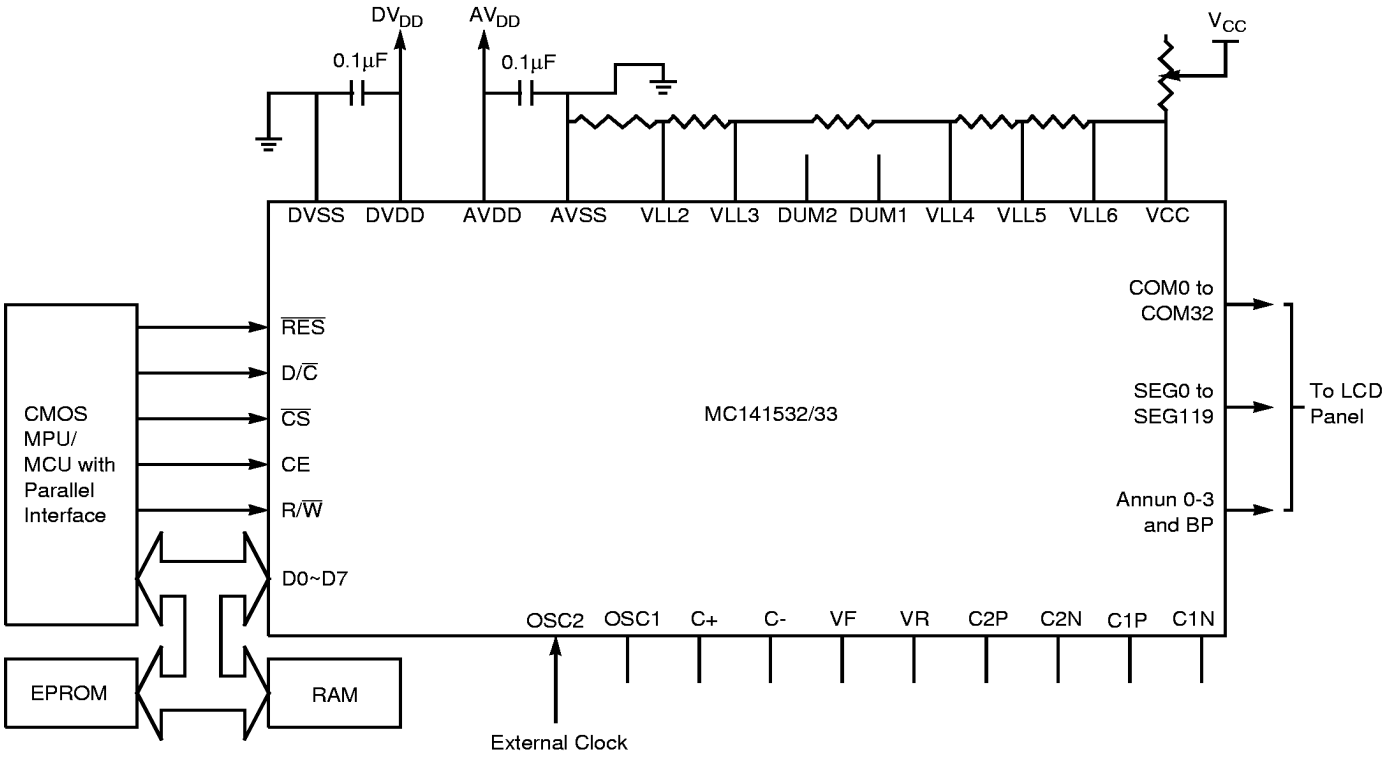

Remark :
1. VR and VF can be left open for Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.




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**Application Circuit**

**16/32/33 MUX Display with Analog Circuitry disabled**




Remark :
1. VR and VF can be left open for Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.



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**Die Pad Co-ordinate for MC141532**

| Pad | Name | X (µm) | Y (µm) | Pad | Name | X (µm) | Y (µm) | Pad | Name | X (µm) | Y (µm) | Pad | Name | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Ann0 | -4803.6 | -526.6 | 61 | DVss | 2472.8 | -530.4 | 122 | Seg0 | 3217.4 | 492.7 | 181 | Seg59 | -1266.6 | 492.7 |
| 2 | Ann1 | -4702.0 | -526.6 | 62 | C+ | 2574.4 | -530.4 | 123 | Seg1 | 3141.4 | 492.7 | 182 | Seg60 | -1342.6 | 492.7 |
| 3 | Ann2 | -4600.4 | -526.6 | 63 | DVss | 2676.0 | -530.4 | 124 | Seg2 | 3065.4 | 492.7 | 183 | Seg61 | -1418.6 | 492.7 |
| 4 | Ann3 | -4498.8 | -526.6 | 64 | C- | 2777.6 | -530.4 | 125 | Seg3 | 2989.4 | 492.7 | 184 | Seg62 | -1494.6 | 492.7 |
| 5 | BP | -4397.2 | -526.6 | 65 | DVss | 2879.2 | -530.4 | 126 | Seg4 | 2913.4 | 492.7 | 185 | Seg63 | -1570.6 | 492.7 |
| 6 | DVdd | -4295.6 | -526.6 | 66 | VCC | 2980.8 | -530.4 | 127 | Seg5 | 2837.4 | 492.7 | 186 | Seg64 | -1646.6 | 492.7 |
| 7 | RES | -4194.0 | -526.6 | 67 | DVss | 3082.4 | -530.4 | 128 | Seg6 | 2761.4 | 492.7 | 187 | Seg65 | -1722.6 | 492.7 |
| 8 | DVss | -4092.4 | -526.6 | 68 | VF | 3184.0 | -530.4 | 129 | Seg7 | 2685.4 | 492.7 | 188 | Seg66 | -1798.6 | 492.7 |
| 9 | D/C | -3990.8 | -526.6 | 69 | DVss | 3285.6 | -530.4 | 130 | Seg8 | 2609.4 | 492.7 | 189 | Seg67 | -1874.6 | 492.7 |
| 10 | R/W | -3889.2 | -526.6 | 70 | VR | 3387.2 | -530.4 | 131 | Seg9 | 2533.4 | 492.7 | 190 | Seg68 | -1950.6 | 492.7 |
| 11 | CS(CLK) | -3787.6 | -526.6 | 71 | AVss | 3488.8 | -530.4 | 132 | Seg10 | 2457.4 | 492.7 | 191 | Seg69 | -2026.6 | 492.7 |
| 12 | DVss | -3686.0 | -526.6 | 72 | OSC1 | 3590.4 | -530.4 | 133 | Seg11 | 2381.4 | 492.7 | 192 | Seg70 | -2102.6 | 492.7 |
| 13 | D0 | -3584.4 | -526.6 | 73 | DVss | 3692.0 | -530.4 | 134 | Seg12 | 2305.4 | 492.7 | 193 | Seg71 | -2178.6 | 492.7 |
| 14 | D1 | -3482.8 | -526.6 | 74 | DVss | 3793.6 | -530.4 | 135 | Seg13 | 2229.4 | 492.7 | 194 | Seg72 | -2254.6 | 492.7 |
| 15 | D2 | -3381.2 | -526.6 | 75 | DVss | 3869.6 | -530.4 | 136 | Seg14 | 2153.4 | 492.7 | 195 | Seg73 | -2330.6 | 492.7 |
| 16 | D3 | -3279.6 | -526.6 | 76 | DVss | 3945.6 | -530.4 | 137 | Seg15 | 2077.4 | 492.7 | 196 | Seg74 | -2406.6 | 492.7 |
| 17 | D4 | -3178.0 | -526.6 | 77 | DVss | 4021.6 | -530.4 | 138 | Seg16 | 2001.4 | 492.7 | 197 | Seg75 | -2482.6 | 492.7 |
| 18 | D5 | -3076.4 | -526.6 | 78 | DVss | 4097.6 | -530.4 | 139 | Seg17 | 1925.4 | 492.7 | 198 | Seg76 | -2558.6 | 492.7 |
| 19 | D6 | -2974.8 | -526.6 | 79 | DVss | 4173.6 | -530.4 | 140 | Seg18 | 1849.4 | 492.7 | 199 | Seg77 | -2634.6 | 492.7 |
| 20 | D7 | -2873.2 | -526.6 | 80 | DVss | 4249.6 | -530.4 | 141 | Seg19 | 1773.4 | 492.7 | 200 | Seg78 | -2710.6 | 492.7 |
| 21 | CE | -2771.6 | -526.6 | 81 | DVss | 4325.6 | -530.4 | 142 | Seg20 | 1697.4 | 492.7 | 201 | Seg79 | -2786.6 | 492.7 |
| 22 | DVss | -2670.0 | -526.6 | 82 | DVss | 4401.6 | -530.4 | 143 | Seg21 | 1621.4 | 492.7 | 202 | Seg80 | -2862.6 | 492.7 |
| 23 | DVss | -2498.3 | -526.6 | 83 | DVss | 4477.6 | -530.4 | 144 | Seg22 | 1545.4 | 492.7 | 203 | Seg81 | -2938.6 | 492.7 |
| 24 | DVss | -873.6 | -591.8 | 84 | DVss | 4553.6 | -530.4 | 145 | Seg23 | 1469.4 | 492.7 | 204 | Seg82 | -3014.6 | 492.7 |
| 25 | DVss | -797.6 | -591.8 | 85 | DVss | 4629.6 | -530.4 | 146 | Seg24 | 1393.4 | 492.7 | 205 | Seg83 | -3090.6 | 492.7 |
| 26 | DVss | -721.6 | -591.8 | 86 | Test1 | 4705.6 | -551.0 | 147 | Seg25 | 1317.4 | 492.7 | 206 | Seg84 | -3166.6 | 492.7 |
| 27 | DVss | -645.6 | -591.8 | 87 | Test2 | 4835.2 | -550.6 | 148 | Seg26 | 1241.4 | 492.7 | 207 | Seg85 | -3242.6 | 492.7 |
| 28 | DVss | -569.6 | -591.8 | 88 | Com32 | 5174.4 | -484.8 | 149 | Seg27 | 1165.4 | 492.7 | 208 | Seg86 | -3318.6 | 492.7 |
| 29 | DVss | -493.6 | -591.8 | 89 | Com0 | 5174.4 | -408.8 | 150 | Seg28 | 1089.4 | 492.7 | 209 | Seg87 | -3394.6 | 492.7 |
| 30 | DVss | -417.6 | -591.8 | 90 | Com1 | 5174.4 | -332.8 | 151 | Seg29 | 1013.4 | 492.7 | 210 | Seg88 | -3470.6 | 492.7 |
| 31 | DVss | -341.6 | -591.8 | 91 | Com2 | 5174.4 | -256.8 | 152 | Seg30 | 937.4 | 492.7 | 211 | Seg89 | -3546.6 | 492.7 |
| 32 | DVss | -265.6 | -591.8 | 92 | Com3 | 5174.4 | -180.8 | 153 | Seg31 | 861.4 | 492.7 | 212 | Seg90 | -3622.6 | 492.7 |
| 33 | DVss | -189.6 | -591.8 | 93 | Com4 | 5174.4 | -104.8 | 154 | Seg32 | 785.4 | 492.7 | 213 | Seg91 | -3698.6 | 492.7 |
| 34 | DVss | -113.6 | -591.8 | 94 | Com5 | 5174.4 | -28.8 | 155 | Seg33 | 709.4 | 492.7 | 214 | Seg92 | -3774.6 | 492.7 |
| 35 | DVss | -37.6 | -591.8 | 95 | Com6 | 5174.4 | 47.2 | 156 | Seg34 | 633.4 | 492.7 | 215 | Seg93 | -3850.6 | 492.7 |
| 36 | DVss | 38.4 | -591.8 | 96 | Com7 | 5174.4 | 123.2 | 157 | Seg35 | 557.4 | 492.7 | 216 | Seg94 | -3926.6 | 492.7 |
| 37 | DVss | 114.4 | -591.8 | 97 | Com8 | 5174.4 | 199.2 | 158 | Seg36 | 481.4 | 492.7 | 217 | Seg95 | -4002.6 | 492.7 |
| 38 | DVss | 190.4 | -591.8 | 98 | Com9 | 5174.4 | 275.2 | 159 | Seg37 | 405.4 | 492.7 | 218 | Seg96 | -4078.6 | 492.7 |
| 39 | DVss | 266.4 | -591.8 | 99 | Com10 | 5174.4 | 351.2 | 160 | Seg38 | 329.4 | 492.7 | 219 | Seg97 | -4154.6 | 492.7 |
| 40 | DVss | 342.4 | -591.8 | 100 | Com11 | 5174.4 | 427.2 | 161 | Seg39 | 253.4 | 492.7 | 220 | Seg98 | -4230.6 | 492.7 |
| 41 | DVss | 418.4 | -591.8 | 101 | Com12 | 5174.4 | 503.2 | 162 | Seg40 | 177.4 | 492.7 | 221 | Seg99 | -4306.6 | 492.7 |
| 42 | DVss | 494.4 | -591.8 | 102 | Com13 | 4771.2 | 492.7 | 163 | Seg41 | 101.4 | 492.7 | 222 | Seg100 | -4382.6 | 492.7 |
| 43 | AVdd | 644.0 | -530.4 | 103 | Com14 | 4695.2 | 492.7 | 164 | Seg42 | 25.4 | 492.7 | 223 | Seg101 | -4458.6 | 492.7 |
| 44 | AVdd | 745.6 | -530.4 | 104 | Com15 | 4619.2 | 492.7 | 165 | Seg43 | -50.6 | 492.7 | 224 | Seg102 | -4534.6 | 492.7 |
| 45 | C1P | 847.2 | -530.4 | 105 | Com16 | 4518.0 | 492.7 | 166 | Seg44 | -126.6 | 492.7 | 225 | Seg103 | -4619.2 | 492.7 |
| 46 | C1N | 948.8 | -530.4 | 106 | Com17 | 4442.0 | 492.7 | 167 | Seg45 | -202.6 | 492.7 | 226 | Seg104 | -4695.2 | 492.7 |
| 47 | C2P | 1050.4 | -530.4 | 107 | Com18 | 4366.0 | 492.7 | 168 | Seg46 | -278.6 | 492.7 | 227 | Seg105 | -4771.2 | 492.7 |
| 48 | C2N | 1152.0 | -530.4 | 108 | Com19 | 4290.0 | 492.7 | 169 | Seg47 | -354.6 | 492.7 | 228 | Seg106 | -5174.4 | 503.2 |
| 49 | VLL2 | 1253.6 | -530.4 | 109 | Com20 | 4214.0 | 492.7 | 170 | Seg48 | -430.6 | 492.7 | 229 | Seg107 | -5174.4 | 427.2 |
| 50 | VLL3 | 1355.2 | -530.4 | 110 | Com21 | 4138.0 | 492.7 | 171 | Seg49 | -506.6 | 492.7 | 230 | Seg108 | -5174.4 | 351.2 |
| 51 | DVss | 1456.8 | -530.4 | 111 | Com22 | 4062.0 | 492.7 | 172 | Seg50 | -582.6 | 492.7 | 231 | Seg109 | -5174.4 | 275.2 |
| 52 | DVss | 1558.4 | -530.4 | 112 | Com23 | 3986.0 | 492.7 | 173 | Seg51 | -658.6 | 492.7 | 232 | Seg110 | -5174.4 | 199.2 |
| 53 | VLL4 | 1660.0 | -530.4 | 113 | Com24 | 3910.0 | 492.7 | 174 | Seg52 | -734.6 | 492.7 | 233 | Seg111 | -5174.4 | 123.2 |
| 54 | VLL5 | 1761.6 | -530.4 | 114 | Com25 | 3834.0 | 492.7 | 175 | Seg53 | -810.6 | 492.7 | 234 | Seg112 | -5174.4 | 47.2 |
| 55 | VLL6 | 1863.2 | -530.4 | 115 | Com26 | 3758.0 | 492.7 | 176 | Seg54 | -886.6 | 492.7 | 235 | Seg113 | -5174.4 | -28.8 |
| 56 | DUM1 | 1964.8 | -530.4 | 116 | Com27 | 3682.0 | 492.7 | 177 | Seg55 | -962.6 | 492.7 | 236 | Seg114 | -5174.4 | -104.8 |
| 57 | DVss | 2066.4 | -530.4 | 117 | Com28 | 3606.0 | 492.7 | 178 | Seg56 | -1038.6 | 492.7 | 237 | Seg115 | -5174.4 | -180.8 |
| 58 | OSC2 | 2168.0 | -530.4 | 118 | Com29 | 3530.0 | 492.7 | 179 | Seg57 | -1114.6 | 492.7 | 238 | Seg116 | -5174.4 | -256.8 |
| 59 | DVss | 2269.6 | -530.4 | 119 | Com30 | 3454.0 | 492.7 | 180 | Seg58 | -1190.6 | 492.7 | 239 | Seg117 | -5174.4 | -332.8 |
| 60 | DUM2 | 2371.2 | -530.4 | 120 | Com31 | 3378.0 | 492.7 | | | | | 240 | Seg118 | -5174.4 | -408.8 |
| | | | | 121 | Com32 | 3302.0 | 492.7 | | | | | 241 | Seg119 | -5174.4 | -484.8 |

**Gold Bump Size**

| Pad | Bump Size X (µm) | Bump Size Y (µm) |
|---|---|---|
| 1-23 | 66.5 | 66.5 |
| 24-42 | 49.0 | 39.8 |
| 43-74 | 66.5 | 66.5 |
| 75-85 | 49.0 | 66.5 |
| 86 | 49.0 | 107.0 |
| 87 | No Gold Bump | |
| 88-101 | 107.0 | 49.0 |
| 102-227 | 49.0 | 107.0 |
| 228-241 | 107.0 | 49.0 |

**Die Size**

| X (µm) | Y (µm) |
|---|---|
| 10881.0 | 1522.0 |



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**Die Pad Co-ordinate for MC141533**

| Pad | Name | X (µm) | Y (µm) | Pad | Name | X (µm) | Y (µm) | Pad | Name | X (µm) | Y (µm) | Pad | Name | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Ann0 | -4803.6 | -526.6 | 61 | DVss | 2472.8 | -530.4 | 122 | Seg17 | 3217.4 | 492.7 | 181 | Seg76 | -1266.6 | 492.7 |
| 2 | Ann1 | -4702.0 | -526.6 | 62 | C+ | 2574.4 | -530.4 | 123 | Seg18 | 3141.4 | 492.7 | 182 | Seg77 | -1342.6 | 492.7 |
| 3 | Ann2 | -4600.4 | -526.6 | 63 | DVss | 2676.0 | -530.4 | 124 | Seg19 | 3065.4 | 492.7 | 183 | Seg78 | -1418.6 | 492.7 |
| 4 | Ann3 | -4498.8 | -526.6 | 64 | C- | 2777.6 | -530.4 | 125 | Seg20 | 2989.4 | 492.7 | 184 | Seg79 | -1494.6 | 492.7 |
| 5 | BP | -4397.2 | -526.6 | 65 | DVss | 2879.2 | -530.4 | 126 | Seg21 | 2913.4 | 492.7 | 185 | Seg80 | -1570.6 | 492.7 |
| 6 | DVdd | -4295.6 | -526.6 | 66 | VCC | 2980.8 | -530.4 | 127 | Seg22 | 2837.4 | 492.7 | 186 | Seg81 | -1646.6 | 492.7 |
| 7 | RES | -4194.0 | -526.6 | 67 | DVss | 3082.4 | -530.4 | 128 | Seg23 | 2761.4 | 492.7 | 187 | Seg82 | -1722.6 | 492.7 |
| 8 | DVss | -4092.4 | -526.6 | 68 | VF | 3184.0 | -530.4 | 129 | Seg24 | 2685.4 | 492.7 | 188 | Seg83 | -1798.6 | 492.7 |
| 9 | D/C | -3990.8 | -526.6 | 69 | DVss | 3285.6 | -530.4 | 130 | Seg25 | 2609.4 | 492.7 | 189 | Seg84 | -1874.6 | 492.7 |
| 10 | R/W | -3889.2 | -526.6 | 70 | VR | 3387.2 | -530.4 | 131 | Seg26 | 2533.4 | 492.7 | 190 | Seg85 | -1950.6 | 492.7 |
| 11 | CS(CLK) | -3787.6 | -526.6 | 71 | AVss | 3488.8 | -530.4 | 132 | Seg27 | 2457.4 | 492.7 | 191 | Seg86 | -2026.6 | 492.7 |
| 12 | DVss | -3686.0 | -526.6 | 72 | OSC1 | 3590.4 | -530.4 | 133 | Seg28 | 2381.4 | 492.7 | 192 | Seg87 | -2102.6 | 492.7 |
| 13 | D0 | -3584.4 | -526.6 | 73 | DVss | 3692.0 | -530.4 | 134 | Seg29 | 2305.4 | 492.7 | 193 | Seg88 | -2178.6 | 492.7 |
| 14 | D1 | -3482.8 | -526.6 | 74 | DVss | 3793.6 | -530.4 | 135 | Seg30 | 2229.4 | 492.7 | 194 | Seg89 | -2254.6 | 492.7 |
| 15 | D2 | -3381.2 | -526.6 | 75 | DVss | 3869.6 | -530.4 | 136 | Seg31 | 2153.4 | 492.7 | 195 | Seg90 | -2330.6 | 492.7 |
| 16 | D3 | -3279.6 | -526.6 | 76 | DVss | 3945.6 | -530.4 | 137 | Seg32 | 2077.4 | 492.7 | 196 | Seg91 | -2406.6 | 492.7 |
| 17 | D4 | -3178.0 | -526.6 | 77 | DVss | 4021.6 | -530.4 | 138 | Seg33 | 2001.4 | 492.7 | 197 | Seg92 | -2482.6 | 492.7 |
| 18 | D5 | -3076.4 | -526.6 | 78 | DVss | 4097.6 | -530.4 | 139 | Seg34 | 1925.4 | 492.7 | 198 | Seg93 | -2558.6 | 492.7 |
| 19 | D6 | -2974.8 | -526.6 | 79 | DVss | 4173.6 | -530.4 | 140 | Seg35 | 1849.4 | 492.7 | 199 | Seg94 | -2634.6 | 492.7 |
| 20 | D7 | -2873.2 | -526.6 | 80 | DVss | 4249.6 | -530.4 | 141 | Seg36 | 1773.4 | 492.7 | 200 | Seg95 | -2710.6 | 492.7 |
| 21 | CE | -2771.6 | -526.6 | 81 | DVss | 4325.6 | -530.4 | 142 | Seg37 | 1697.4 | 492.7 | 201 | Seg96 | -2786.6 | 492.7 |
| 22 | DVss | -2670.0 | -526.6 | 82 | DVss | 4401.6 | -530.4 | 143 | Seg38 | 1621.4 | 492.7 | 202 | Seg97 | -2862.6 | 492.7 |
| 23 | DVss | -2498.3 | -526.6 | 83 | DVss | 4477.6 | -530.4 | 144 | Seg39 | 1545.4 | 492.7 | 203 | Seg98 | -2938.6 | 492.7 |
| 24 | DVss | -873.6 | -591.8 | 84 | DVss | 4553.6 | -530.4 | 145 | Seg40 | 1469.4 | 492.7 | 204 | Seg99 | -3014.6 | 492.7 |
| 25 | DVss | -797.6 | -591.8 | 85 | DVss | 4629.6 | -530.4 | 146 | Seg41 | 1393.4 | 492.7 | 205 | Seg100 | -3090.6 | 492.7 |
| 26 | DVss | -721.6 | -591.8 | 86 | Test2 | 4705.6 | -551.0 | 147 | Seg42 | 1317.4 | 492.7 | 206 | Seg101 | -3166.6 | 492.7 |
| 27 | DVss | -645.6 | -591.8 | 87 | Test1 | 4835.2 | -550.6 | 148 | Seg43 | 1241.4 | 492.7 | 207 | Seg102 | -3242.6 | 492.7 |
| 28 | DVss | -569.6 | -591.8 | 88 | Com32 | 5174.4 | -484.8 | 149 | Seg44 | 1165.4 | 492.7 | 208 | Seg103 | -3318.6 | 492.7 |
| 29 | DVss | -493.6 | -591.8 | 89 | Com0 | 5174.4 | -408.8 | 150 | Seg45 | 1089.4 | 492.7 | 209 | Seg104 | -3394.6 | 492.7 |
| 30 | DVss | -417.6 | -591.8 | 90 | Com1 | 5174.4 | -332.8 | 151 | Seg46 | 1013.4 | 492.7 | 210 | Seg105 | -3470.6 | 492.7 |
| 31 | DVss | -341.6 | -591.8 | 91 | Com2 | 5174.4 | -256.8 | 152 | Seg47 | 937.4 | 492.7 | 211 | Seg106 | -3546.6 | 492.7 |
| 32 | DVss | -265.6 | -591.8 | 92 | Com3 | 5174.4 | -180.8 | 153 | Seg48 | 861.4 | 492.7 | 212 | Seg107 | -3622.6 | 492.7 |
| 33 | DVss | -189.6 | -591.8 | 93 | Com4 | 5174.4 | -104.8 | 154 | Seg49 | 785.4 | 492.7 | 213 | Seg108 | -3698.6 | 492.7 |
| 34 | DVss | -113.6 | -591.8 | 94 | Com5 | 5174.4 | -28.8 | 155 | Seg50 | 709.4 | 492.7 | 214 | Seg109 | -3774.6 | 492.7 |
| 35 | DVss | -37.6 | -591.8 | 95 | Com6 | 5174.4 | 47.2 | 156 | Seg51 | 633.4 | 492.7 | 215 | Seg110 | -3850.6 | 492.7 |
| 36 | DVss | 38.4 | -591.8 | 96 | Com7 | 5174.4 | 123.2 | 157 | Seg52 | 557.4 | 492.7 | 216 | Seg111 | -3926.6 | 492.7 |
| 37 | DVss | 114.4 | -591.8 | 97 | Com8 | 5174.4 | 199.2 | 158 | Seg53 | 481.4 | 492.7 | 217 | Seg112 | -4002.6 | 492.7 |
| 38 | DVss | 190.4 | -591.8 | 98 | Com9 | 5174.4 | 275.2 | 159 | Seg54 | 405.4 | 492.7 | 218 | Seg113 | -4078.6 | 492.7 |
| 39 | DVss | 266.4 | -591.8 | 99 | Com10 | 5174.4 | 351.2 | 160 | Seg55 | 329.4 | 492.7 | 219 | Seg114 | -4154.6 | 492.7 |
| 40 | DVss | 342.4 | -591.8 | 100 | Com11 | 5174.4 | 427.2 | 161 | Seg56 | 253.4 | 492.7 | 220 | Seg115 | -4230.6 | 492.7 |
| 41 | DVss | 418.4 | -591.8 | 101 | Com12 | 5174.4 | 503.2 | 162 | Seg57 | 177.4 | 492.7 | 221 | Seg116 | -4306.6 | 492.7 |
| 42 | DVss | 494.4 | -591.8 | 102 | Com13 | 4771.2 | 492.7 | 163 | Seg58 | 101.4 | 492.7 | 222 | Seg117 | -4382.6 | 492.7 |
| 43 | AVdd | 644.0 | -530.4 | 103 | Com14 | 4695.2 | 492.7 | 164 | Seg59 | 25.4 | 492.7 | 223 | Seg118 | -4458.6 | 492.7 |
| 44 | AVdd | 745.6 | -530.4 | 104 | Com15 | 4619.2 | 492.7 | 165 | Seg60 | -50.6 | 492.7 | 224 | Seg119 | -4534.6 | 492.7 |
| 45 | C1P | 847.2 | -530.4 | 105 | Seg0 | 4518.0 | 492.7 | 166 | Seg61 | -126.6 | 492.7 | 225 | Com32 | -4619.2 | 492.7 |
| 46 | C1N | 948.8 | -530.4 | 106 | Seg1 | 4442.0 | 492.7 | 167 | Seg62 | -202.6 | 492.7 | 226 | Com31 | -4695.2 | 492.7 |
| 47 | C2P | 1050.4 | -530.4 | 107 | Seg2 | 4366.0 | 492.7 | 168 | Seg63 | -278.6 | 492.7 | 227 | Com30 | -4771.2 | 492.7 |
| 48 | C2N | 1152.0 | -530.4 | 108 | Seg3 | 4290.0 | 492.7 | 169 | Seg64 | -354.6 | 492.7 | 228 | Com29 | -5174.4 | 503.2 |
| 49 | VLL2 | 1253.6 | -530.4 | 109 | Seg4 | 4214.0 | 492.7 | 170 | Seg65 | -430.6 | 492.7 | 229 | Com28 | -5174.4 | 427.2 |
| 50 | VLL3 | 1355.2 | -530.4 | 110 | Seg5 | 4138.0 | 492.7 | 171 | Seg66 | -506.6 | 492.7 | 230 | Com27 | -5174.4 | 351.2 |
| 51 | DVss | 1456.8 | -530.4 | 111 | Seg6 | 4062.0 | 492.7 | 172 | Seg67 | -582.6 | 492.7 | 231 | Com26 | -5174.4 | 275.2 |
| 52 | DVss | 1558.4 | -530.4 | 112 | Seg7 | 3986.0 | 492.7 | 173 | Seg68 | -658.6 | 492.7 | 232 | Com25 | -5174.4 | 199.2 |
| 53 | VLL4 | 1660.0 | -530.4 | 113 | Seg8 | 3910.0 | 492.7 | 174 | Seg69 | -734.6 | 492.7 | 233 | Com24 | -5174.4 | 123.2 |
| 54 | VLL5 | 1761.6 | -530.4 | 114 | Seg9 | 3834.0 | 492.7 | 175 | Seg70 | -810.6 | 492.7 | 234 | Com23 | -5174.4 | 47.2 |
| 55 | VLL6 | 1863.2 | -530.4 | 115 | Seg10 | 3758.0 | 492.7 | 176 | Seg71 | -886.6 | 492.7 | 235 | Com22 | -5174.4 | -28.8 |
| 56 | DUM1 | 1964.8 | -530.4 | 116 | Seg11 | 3682.0 | 492.7 | 177 | Seg72 | -962.6 | 492.7 | 236 | Com21 | -5174.4 | -104.8 |
| 57 | DVss | 2066.4 | -530.4 | 117 | Seg12 | 3606.0 | 492.7 | 178 | Seg73 | -1038.6 | 492.7 | 237 | Com20 | -5174.4 | -180.8 |
| 58 | OSC2 | 2168.0 | -530.4 | 118 | Seg13 | 3530.0 | 492.7 | 179 | Seg74 | -1114.6 | 492.7 | 238 | Com19 | -5174.4 | -256.8 |
| 59 | DVss | 2269.6 | -530.4 | 119 | Seg14 | 3454.0 | 492.7 | 180 | Seg75 | -1190.6 | 492.7 | 239 | Com18 | -5174.4 | -332.8 |
| 60 | DUM2 | 2371.2 | -530.4 | 120 | Seg15 | 3378.0 | 492.7 | | | | | 240 | Com17 | -5174.4 | -408.8 |
| | | | | 121 | Seg16 | 3302.0 | 492.7 | | | | | 241 | Com16 | -5174.4 | -484.8 |

**Gold Bump Size**

| Pad | Bump Size X (µm) | Bump Size Y (µm) |
|---|---|---|
| 1-23 | 66.5 | 66.5 |
| 24-42 | 49.0 | 39.8 |
| 43-74 | 66.5 | 66.5 |
| 75-85 | 49.0 | 66.5 |
| 86 | 49.0 | 107.0 |
| 87 | No Gold Bump | |
| 88-101 | 107.0 | 49.0 |
| 102-227 | 49.0 | 107.0 |
| 228-241 | 107.0 | 49.0 |

**Die Size**

| X (µm) | Y (µm) |
|---|---|
| 10881.0 | 1522.0 |



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