General Description

The WST3401A is the highest performance trench P-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications .

The WST3401A meet the RoHS and Green Product requirement , with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

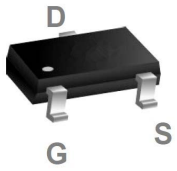
Product Summery

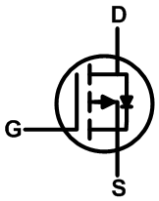
BVDSS	RDSON	ID
-30V	48mΩ	-5.0A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23-3L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V_{DS}	Drain-Source Voltage	-30		V
V_{GS}	Gate-Source Voltage	±12		V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-5.7	-5.0	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ -10V[1]	-4.5	-4.0	A
I_{DM}	Pulsed Drain Current[2]	-17		A
P_D@T_A=25℃	Total Power Dissipation[3]	1.32	1	W
P_D@T_A=70℃	Total Power Dissipation[3]	0.84	0.64	W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	125	℃/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1] (t ≤10s)	---	95	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	80	℃/W

Electrical Characteristics (T_J=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.023	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-3A	---	48	57	mΩ
		V_{GS}=-4.5V , I_D=-2A	---	55	64	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.6	---	-1.2	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-3A	---	11	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-3A	---	6.2	9.0	nC
Q_{gs}	Gate-Source Charge		---	2.2	3.2	
Q_{gd}	Gate-Drain Charge		---	1.8	2.7	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω, I_D=-3A	---	2.7	5.6	ns
T_r	Rise Time		---	8.3	15.1	
$T_{d(off)}$	Turn-Off Delay Time		---	38	78.0	
T_f	Fall Time		---	6	12.0	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	580	816	pF
C_{oss}	Output Capacitance		---	98	140	
C_{rss}	Reverse Transfer Capacitance		---	77	112	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-4.0	A
I_{SM}	Pulsed Source Current[2,4]		---	---	-14	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
t_{rr}	Reverse Recovery Time	I_F=-3A , dI/dt=100A/μs , T_J=25℃	---	7.6	---	nS
Q_{rr}	Reverse Recovery Charge		---	2.4	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec,t<10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

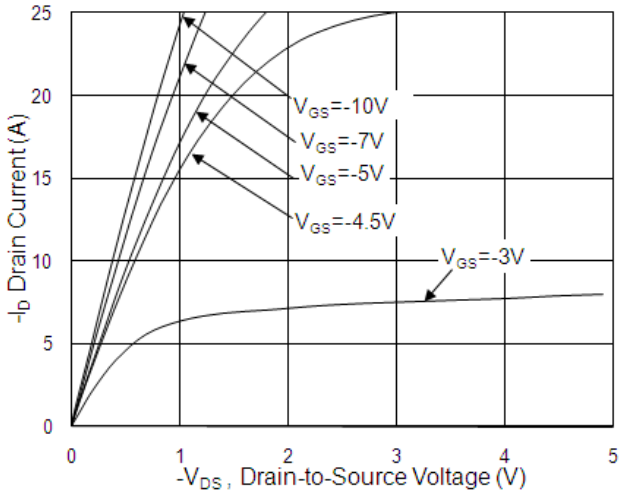


Fig.1 Typical Output Characteristics

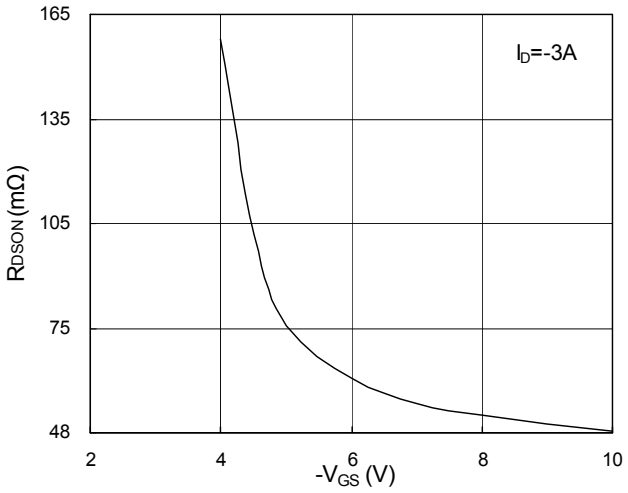


Fig.2 On-Resistance v.s Gate-Source

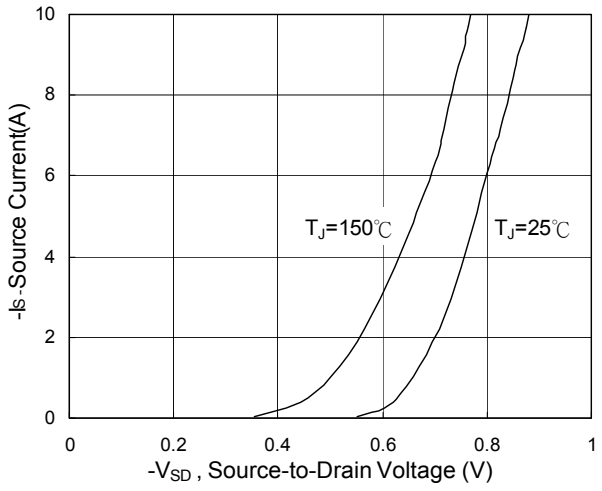


Fig.3 Forward Characteristics of Reverse

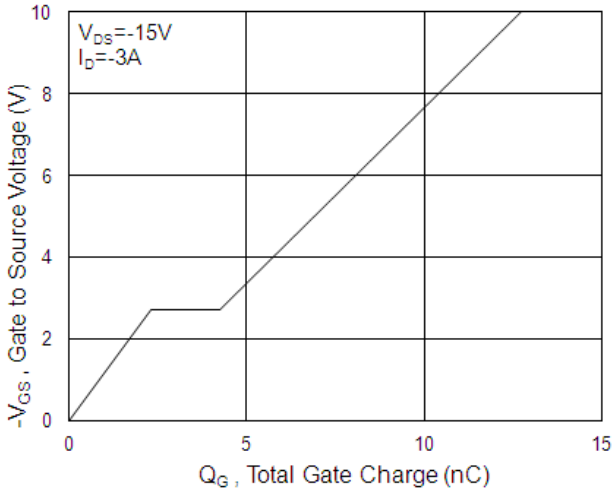


Fig.4 Gate-Charge Characteristics

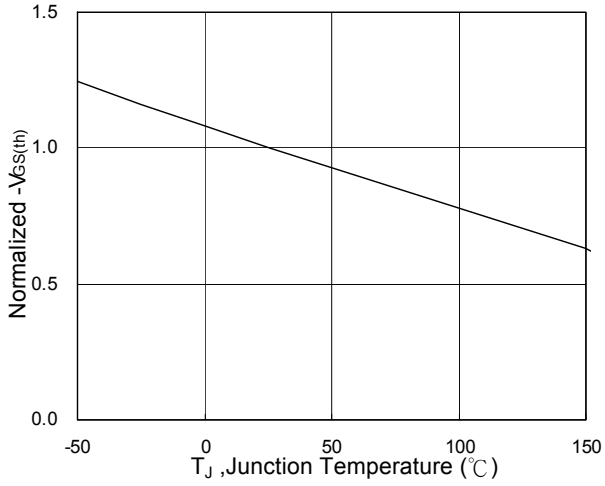


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

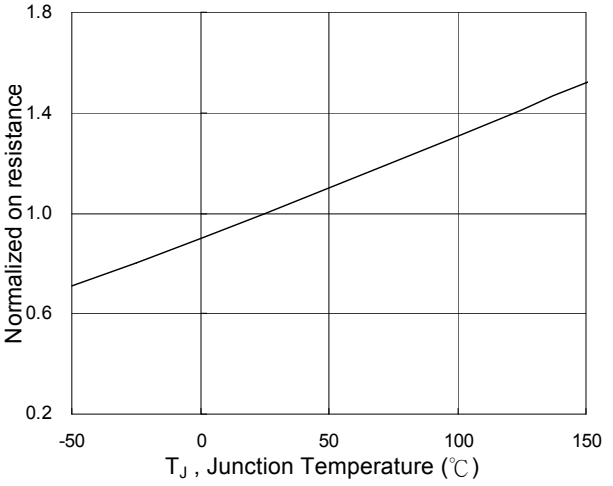


Fig.6 Normalized R_{DSON} vs T_J

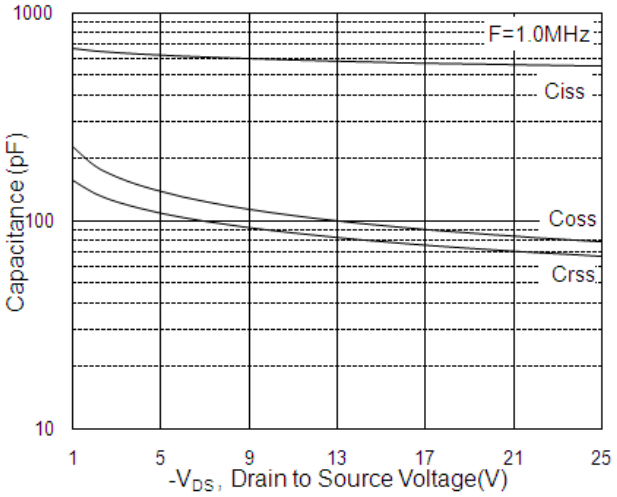


Fig.7 Capacitance

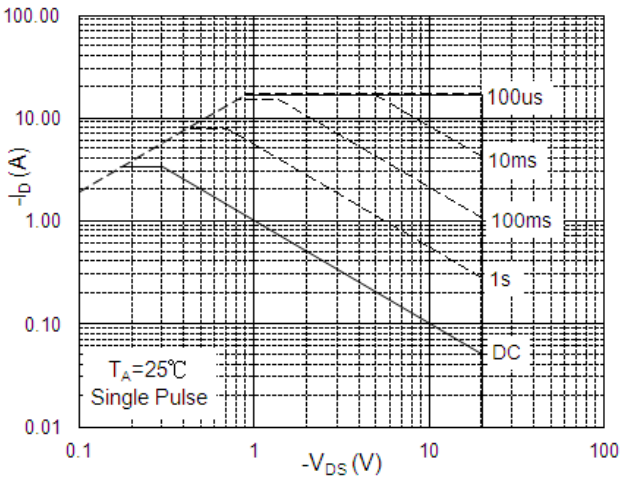


Fig.8 Safe Operating Area

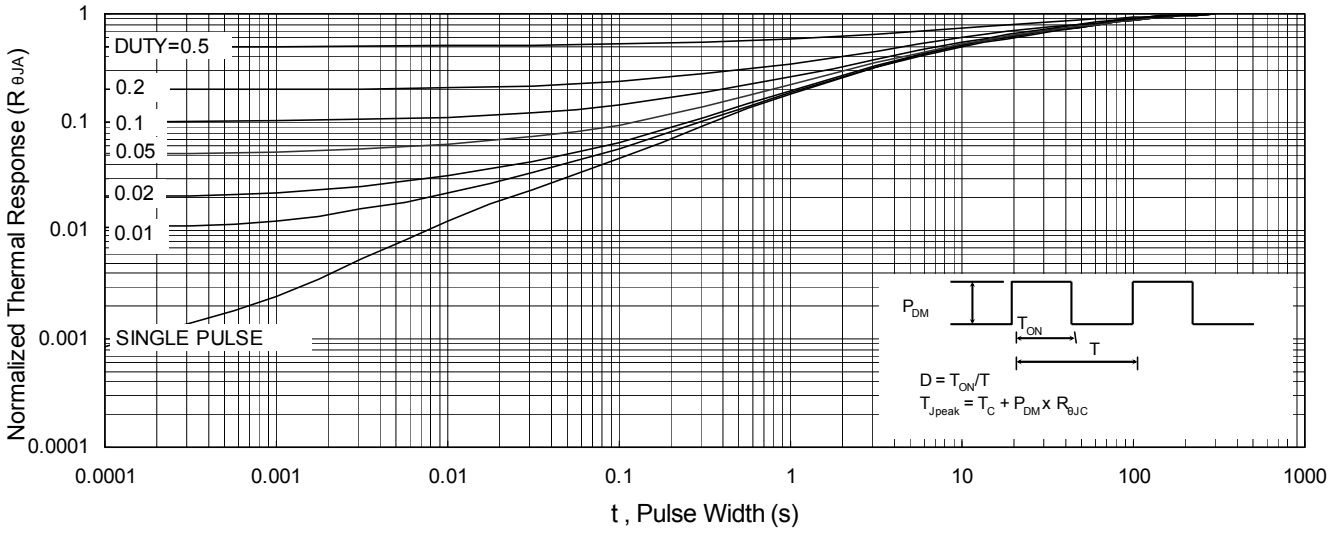


Fig.9 Normalized Maximum Transient Thermal Impedance

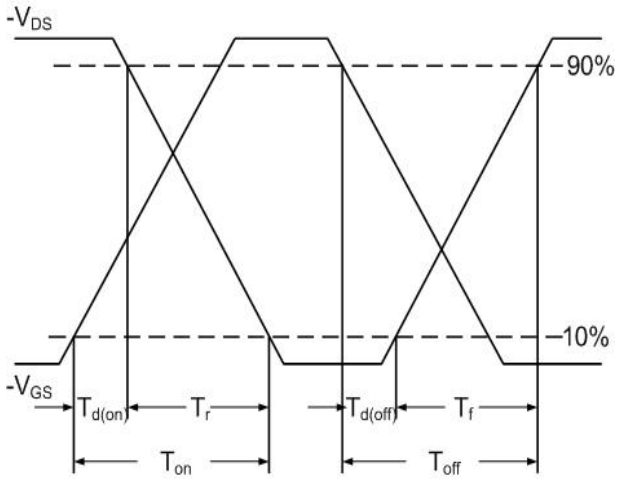


Fig.10 Switching Time Waveform

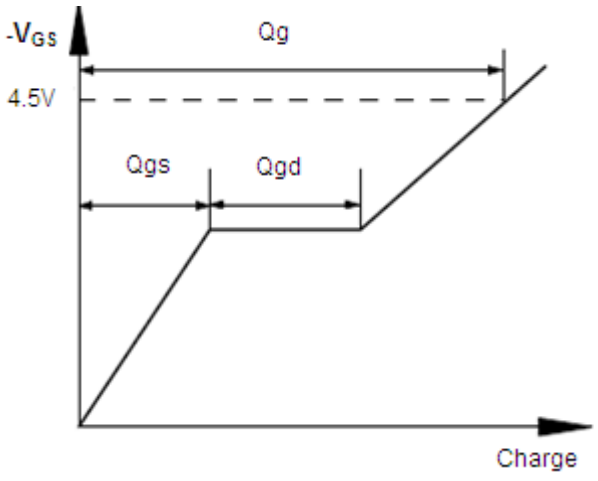


Fig.11 Gate Charge Waveform

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