LH1687

240-output TFT-LCD Source Driver IC

DESCRIPTION

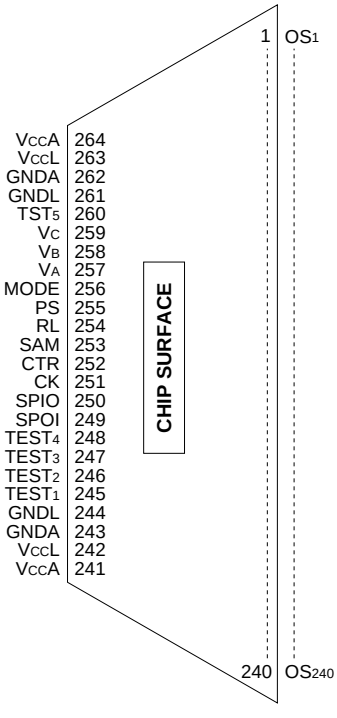
The LH1687 is a 240-output TFT-LCD source driver IC used in such products as TV sets. The LH1687 samples and holds three video signals of R, G and B by sample and hold circuits synchronized with the CK, and simultaneously outputs the LCD drive voltage from all output pins.

FEATURES

- Number of LCD drive outputs : 240
- Output circuit form : Push pull output
- Power save function : By setting the LCD drive output in a high-impedance condition, the current source of the LCD drive output circuit is cut off, which makes low power operation possible
- Sampling timing : Normal sampling operation and 3-point simultaneous sampling operation can be selected
- Video signal setting : Available for stripe pixel array panels and delta pixel array panels using mode setting circuit
- Sampling clock frequency : 25 MHz (MAX.)
- Cascade connection
- Sampling sequence :
  Output shift direction can be selected
  $OS_1 \rightarrow OS_{240}$ or $OS_{240} \rightarrow OS_1$
- Output amplitude voltage :
  4.8 Vp-p (at 5.0 V supply voltage)
- Supply voltages
  – $V_{CC}L$ (for logic system) : +3.0 to +5.5 V
  – $V_{CC}A$ (for LCD drive system) : +3.0 to +5.5 V
- Operating temperature : –30 to + 85 ˚C
- Package : 264-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

264-PIN TCP TOP VIEW



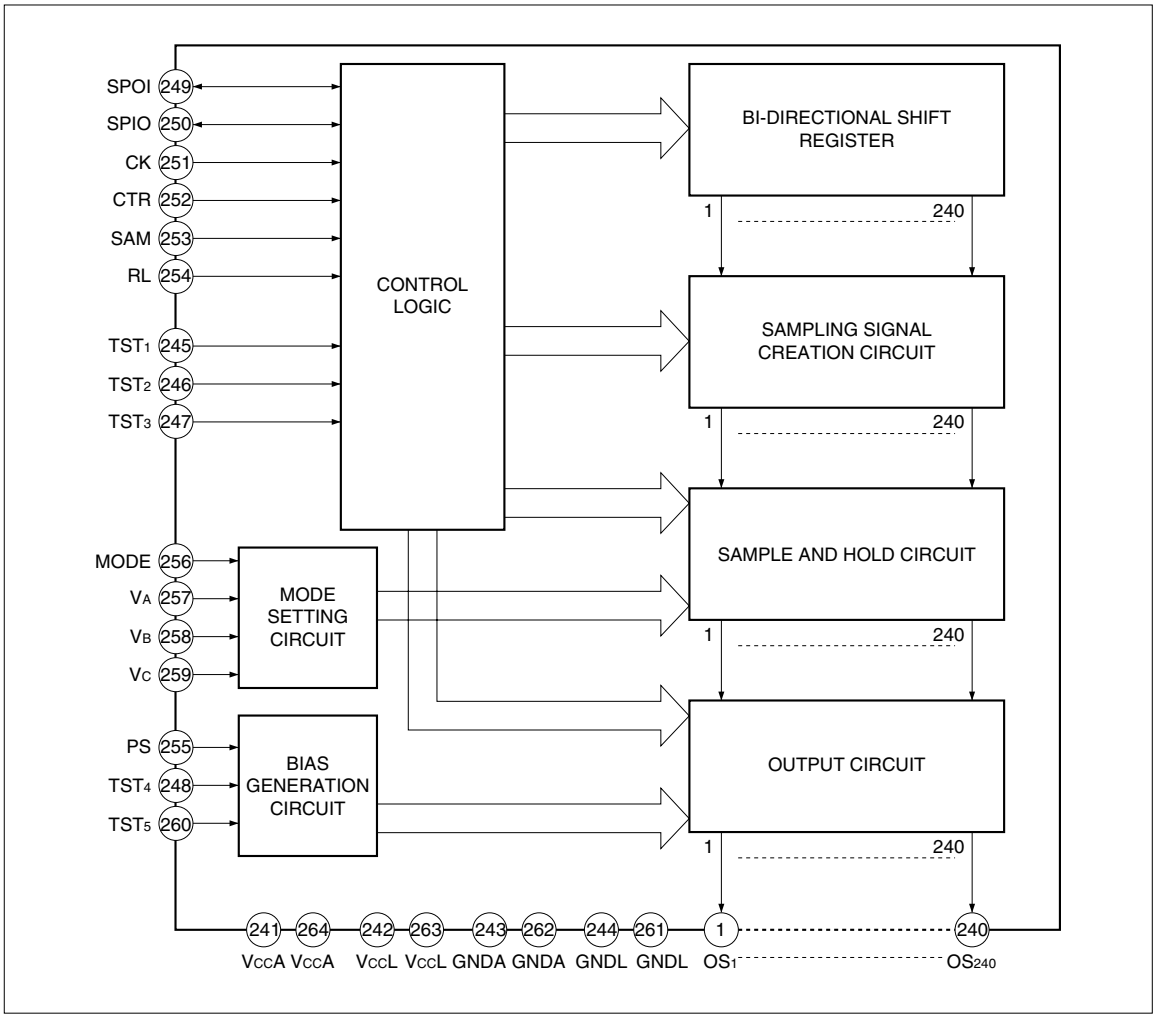
NOTE :
Doesn't prescribe TCP outline.

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PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 240	OS_1-OS_{240}	O	LCD drive output pins
241, 264	$V_{CC}A$	–	Power supply pins for LCD drive circuit
242, 263	$V_{CC}L$	–	Power supply pins for logic circuit
243, 262	GNDA	–	Ground pins for LCD drive system
244, 261	GNDL	–	Ground pins for logic system
245 to 248	TST_1-TST_4	I	IC test pins
249	SPOI	I/O	Start pulse input/cascade output pin
250	SPIO	I/O	Start pulse input/cascade output pin
251	CK	I	Horizontal shift clock input pin
252	CTR	I	LCD drive circuit operation selection pin
253	SAM	I	Sampling mode selection pin
254	RL	I	Sampling sequence selection pin
255	PS	I	Power save mode setting pin
256	MODE	I	Video signals form setting pin
257 to 259	V_A, V_B, V_C	I	Video signal input pins
260	TST_5	I	IC test pin

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Control Logic	Used to create signals necessary for each operation mode setting and sampling signal creation circuits, etc.
Bi-directional Shift Register	Used as transfer circuit of video sampling start signals. It is possible to set the direction of sampling start signal sequence $OS_1 \rightarrow OS_{240}$ or $OS_{240} \rightarrow OS_1$ by setting the R/L pin.
Sampling Signal Creation Circuit	Used to create the sampling signals corresponding to each output pin based on the sampling start signals transferred by the bi-directional shift register.
Mode Setting Circuit	Used to set the form of the video signals to be sent to the sample and hold circuits.
Sample and Hold Circuit	Used to sample the video signals input from the mode setting circuit at the timing of the sampling signals and hold the sampling data until the next sampling operation.
Bias Generation Circuit	Used to generate bias voltage necessary for output circuits.
Output Circuit	The circuit consists of a push-pull output operational amplifier and outputs the voltage corresponding to the data held in the sample and hold circuits.

INPUT/OUTPUT CIRCUITS

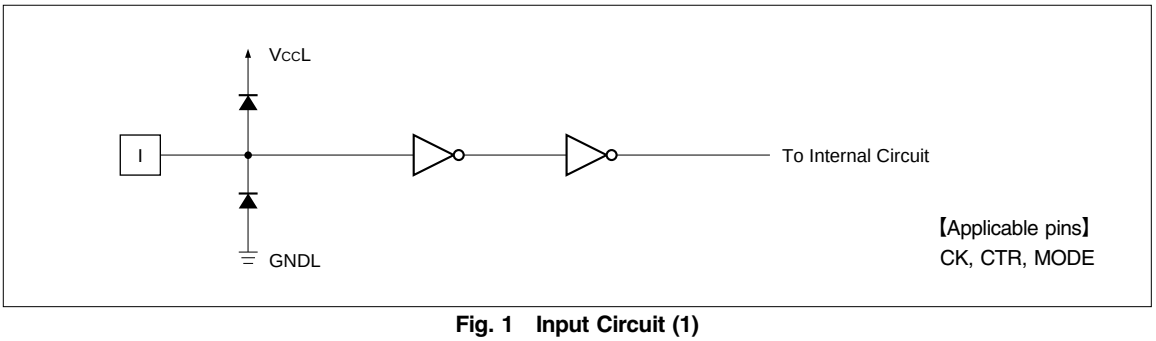


Fig. 1 Input Circuit (1)

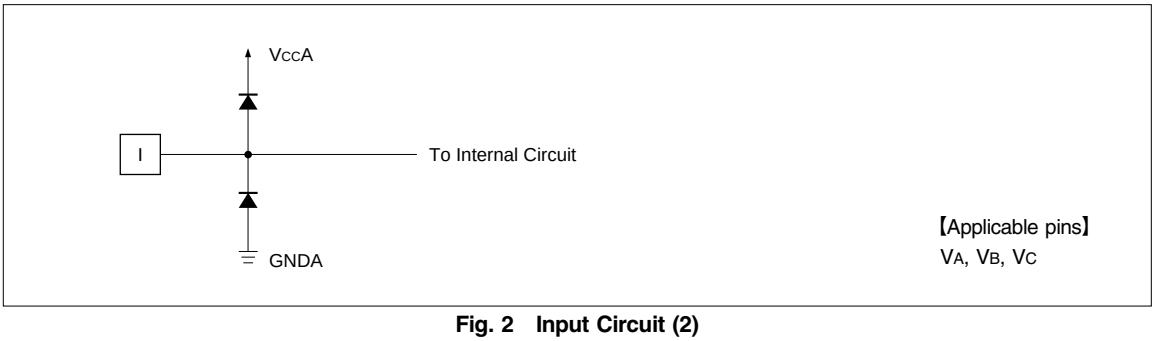


Fig. 2 Input Circuit (2)

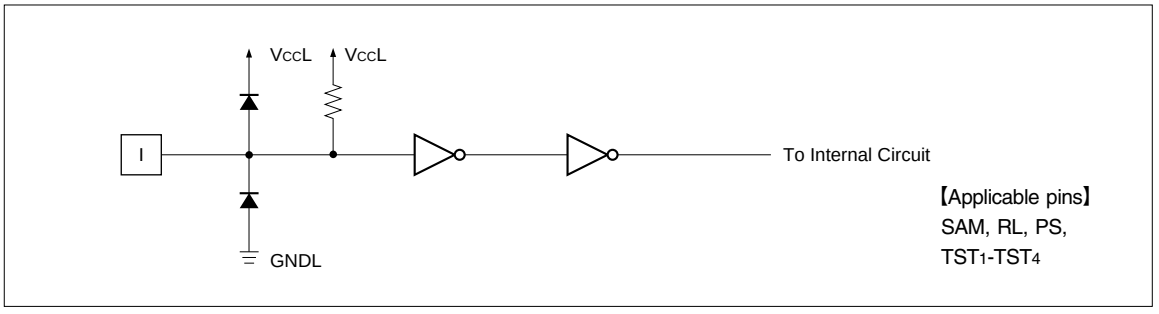


Fig. 3 Input Circuit (3)

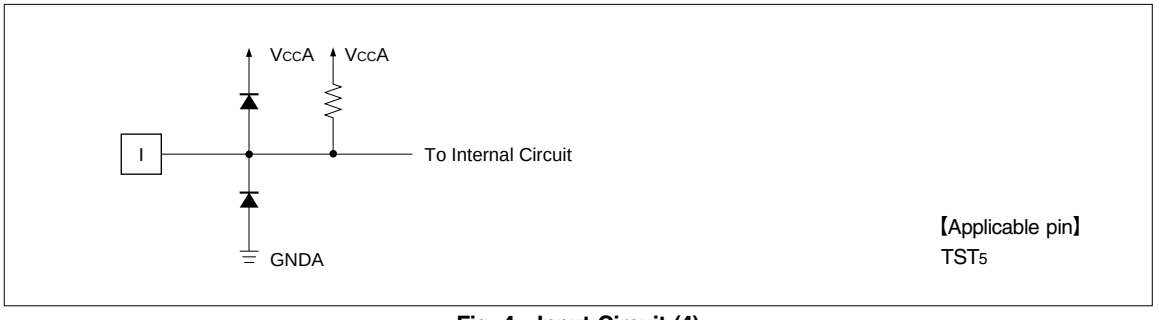


Fig. 4 Input Circuit (4)

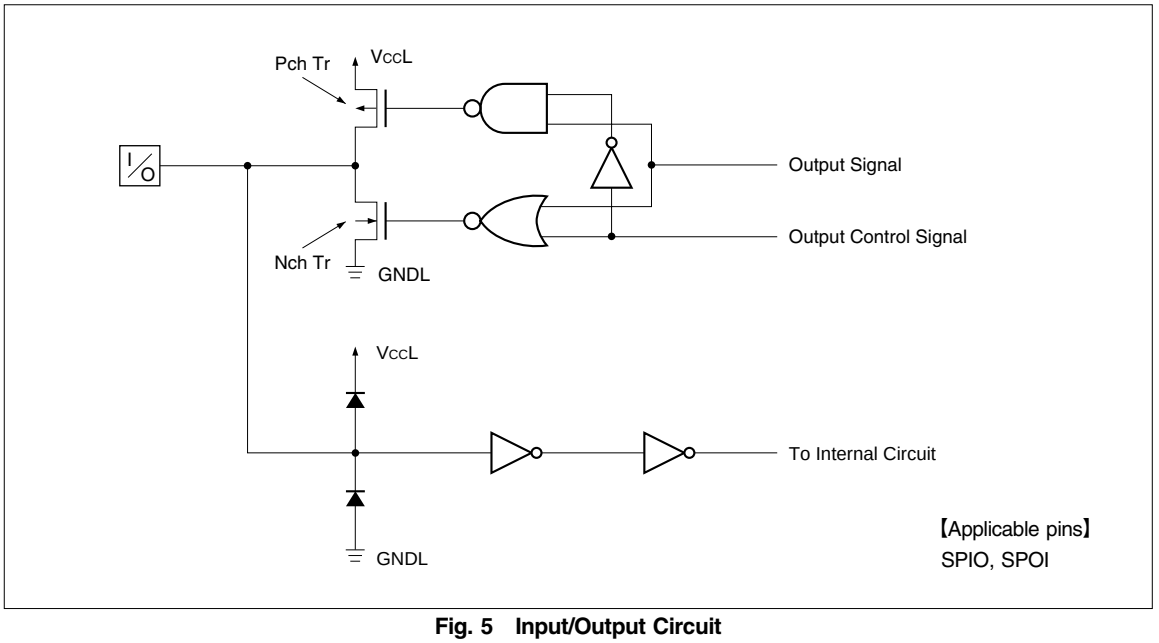


Fig. 5 Input/Output Circuit

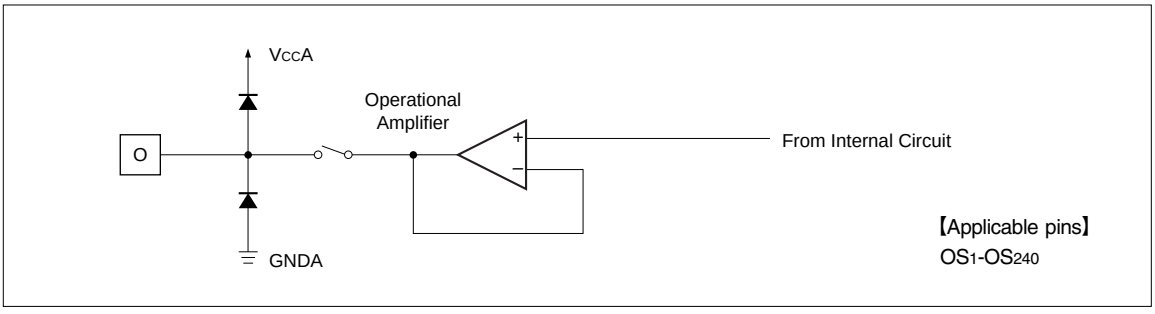


Fig. 6 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

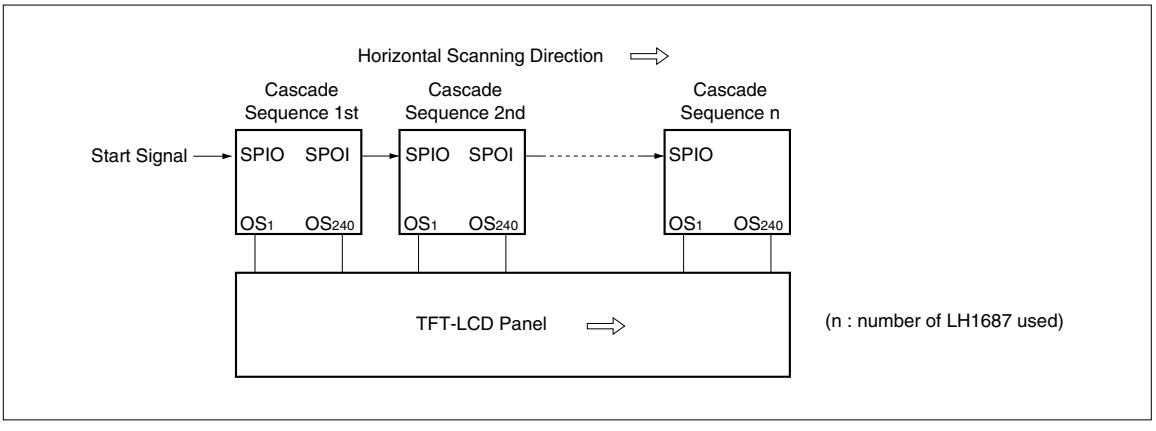
SYMBOL	FUNCTION
VccL	Used as power supply pin for logic circuit, connected to +3.0 to +5.0 V.
VccA	Used as power supply pin for LCD drive circuit, connected to +3.0 to +5.0 V. Must be set to VccL ≤ VccA.
GNDL	Used as ground pin for logic circuit, connected to 0 V.
GNDA	Used as ground pin for LCD drive circuit, connected to 0 V.
TST1-TST4	Used as input pins for IC testing, connected to VccL (high level).
TST5	Used as input pins for IC testing, connected to VccA (high level).
SPIO SPOI	Used as input/output pins of cascade operation start signal. SPIO becomes input pin of operation start signal and SPOI becomes output pin of operation start signal of next IC when set to R/L = "H". SPOI becomes input pin of operation start signal and SPIO becomes output pin of operation start signal of next IC when set to R/L = "L".
CK	Used as horizontal shift clock input pin. Video signals are sampled in order at the rising and falling edge of CK.
CTR	Used as input pin of selecting video signal sampling circuits and selecting input signal of output operational amplifiers.
SAM	Used as input pin for setting the selecting of normal sampling operation or 3-point simultaneous sampling operation. For normal sampling operation, video signals are sampled into sample and hold circuits every 1 LCD drive output. For 3-point simultaneous sampling operation, video signals are sampled into sample and hold circuits every 3 LCD drive outputs simultaneously. For either operation, sampling signals are shifted at every rising and falling edge of horizontal shift clock of CK pin (half clock), and their sampling period is equal to the period of one clock.

SYMBOL	FUNCTION
RL	Used as input pin for setting the shift direction of video signal sampling sequence and the selecting input/output of SPIO/SPOI pins. Video signals are sampled in order of $OS_1 \rightarrow OS_{240}$, set SPIO to input of operation start signal and set SPOI to output of operation start signal of next IC when set RL to "H". Video signals are sampled in order of $OS_{240} \rightarrow OS_1$, set SPOI to input of operation start signal and set SPIO to output of operation start signal of next IC when set RL to "L".
PS	Used as input pin for setting of power save mode. LCD drive output pins output voltage corresponding to video signals held in the sample and hold circuits when set PS to "H". The LH1687 is set low power mode by setting high-impedance condition and cutting off current source of LCD drive outputs when set PS to "L".
MODE	Used as input pin for setting video signals for sampling in the sample and hold circuits. By mode setting circuit, video signals are sampled and output in order of V_B, V_A, and V_C when set to "H" and in order of V_C, V_B, and V_A when set to "L" with respect to OS_1 to OS_{240} .
V_A V_B V_C	Used as input pins of video signals. V_B, V_A, V_C, ··· V_B, V_A, V_C or V_C, V_B, V_A, ··· V_C, V_B, V_A are input with respect to LCD drive outputs OS_1, OS_2, OS_3, ··· OS_{238}, OS_{239}, OS_{240} by MODE pin setting condition.
OS_1-OS_{240}	Used as LCD drive output pins. Voltage corresponding to video signals held in the sample and hold circuits is output when set to PS = "H", and becomes high-impedance condition when set to PS = "L".

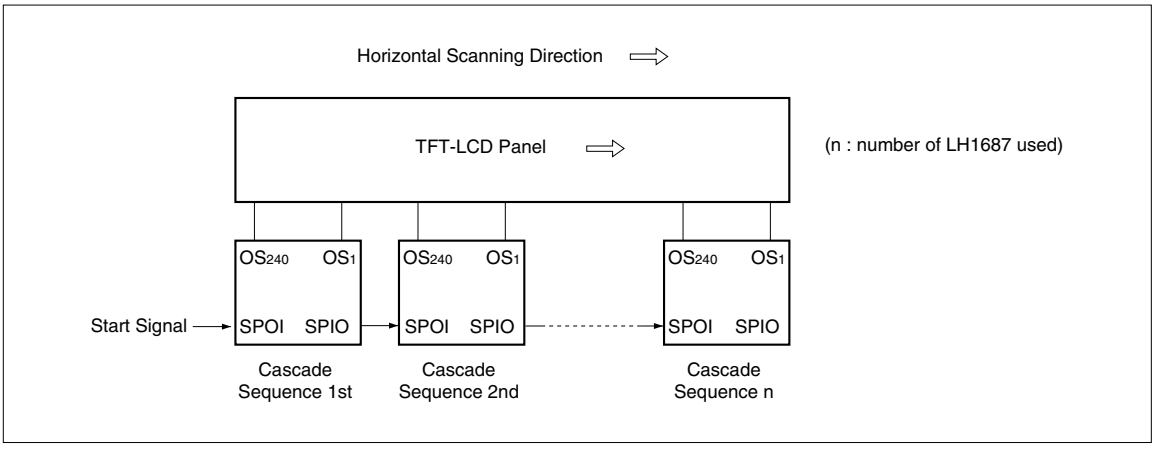
Functional Operations

(1) Examples of Cascade Sequence

When RL = "H"



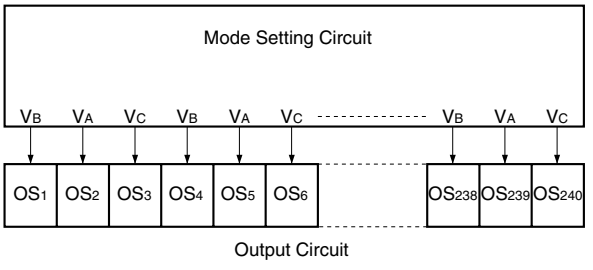
When RL = "L"



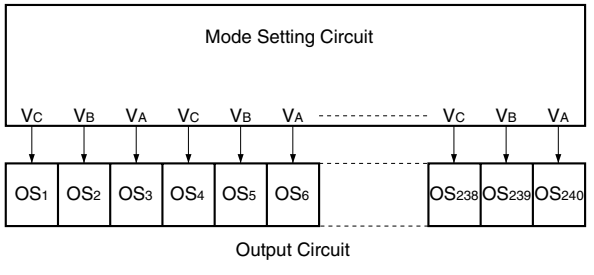
(2) Video Signal Mode Setting Function

With MODE pin condition, it is possible to set the form of video signals corresponding to each output pin by selecting the mode setting circuit.

When MODE = "H"



When MODE = "L"



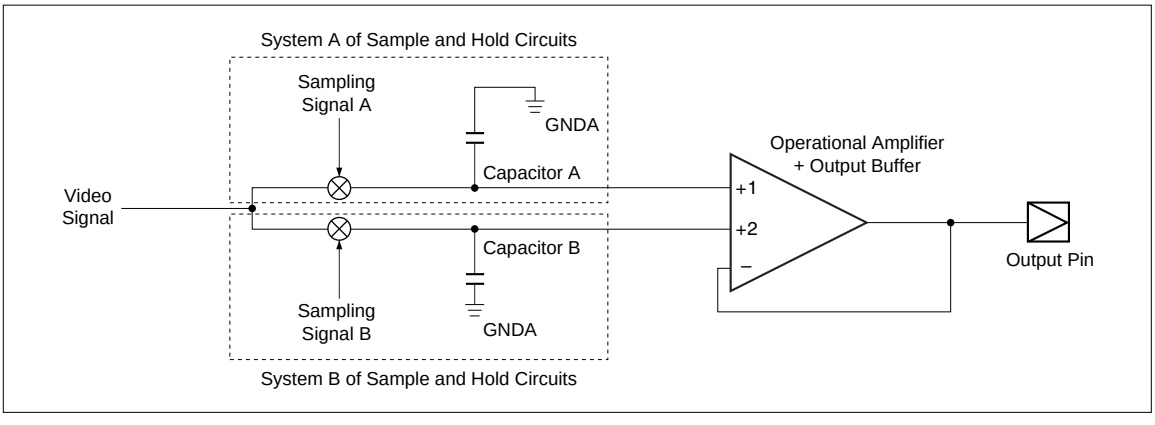
(3) Output Circuit Type

The LH1687 samples video signals by the sample and hold circuits of 2 systems and outputs the voltage corresponding to the sampled data by the input switching operational amplifiers with push-pull output buffer.

Sample and hold circuits and output circuits are as shown in the diagram below.

When CTR = "H", the LH1687 samples the data to system A of the sample and hold circuits and outputs the voltage corresponding to the voltage sampled by capacitor B of system B.

When CTR = "L", the LH1687 samples the data to system B of the sample and hold circuits and outputs the voltage corresponding to the voltage sampled by capacitor A of system A.

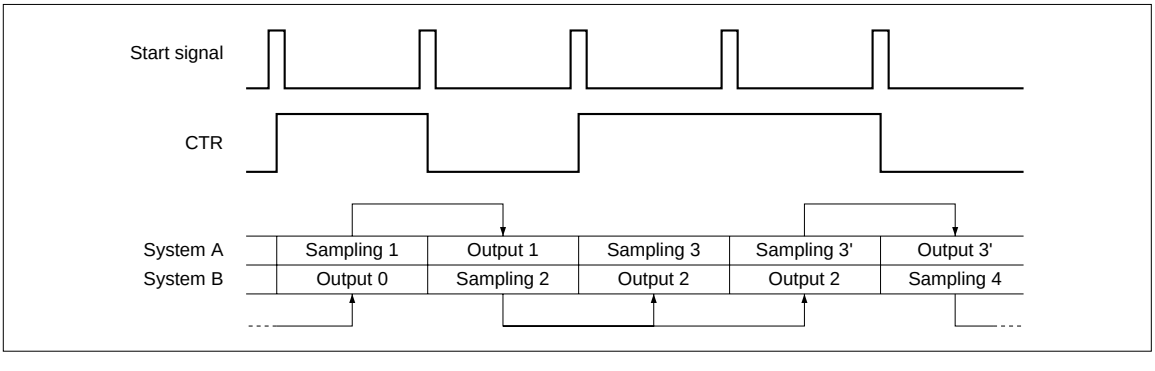


Therefore, it is usually necessary to repeat the sampling operation and output operation by exchanging CTR signal ("H" to "L" or "L" to "H") for every start signal.

While CTR signal is set to "H" or "L" several times for start signal, the same voltage is output continuously.

The output voltage corresponds to the data sampled by the previous sampling operation.

Timing of operation is as follows.

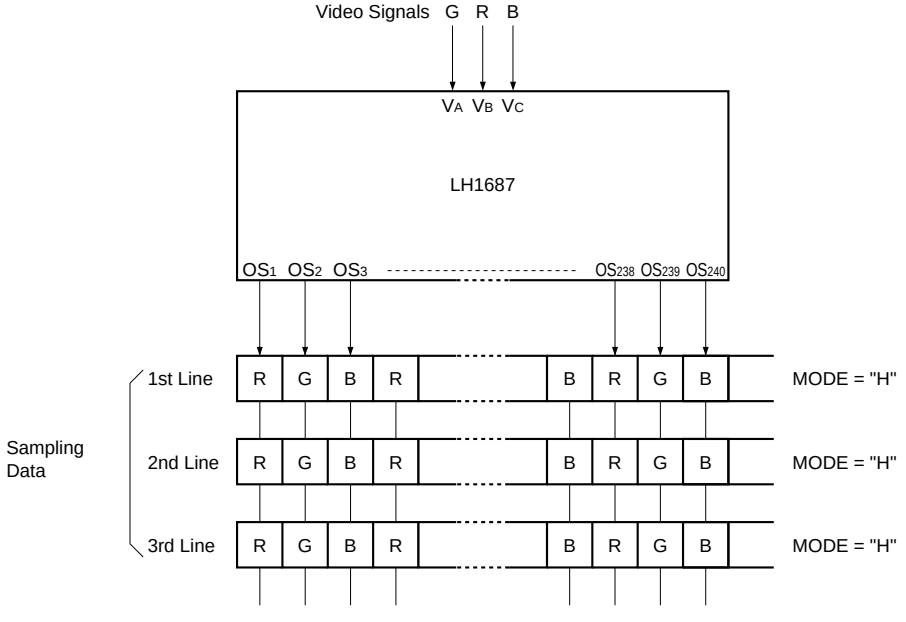


Also, there is a power save function which makes high-impedance of the output pin and a reduction in the current of operational amplifiers possible when set to PS = "L", but careful attention must be paid to the displaying quality etc. when using it.

(4) Examples of LCD Panel Connection

With the video signal mode setting function of (2), it is possible to connect LCD panel to the stripe pixel array panel and delta pixel array panel as shown in the following examples.

(a) Example of Stripe Pixel Array Panel Connection



Connection of video signal input pins

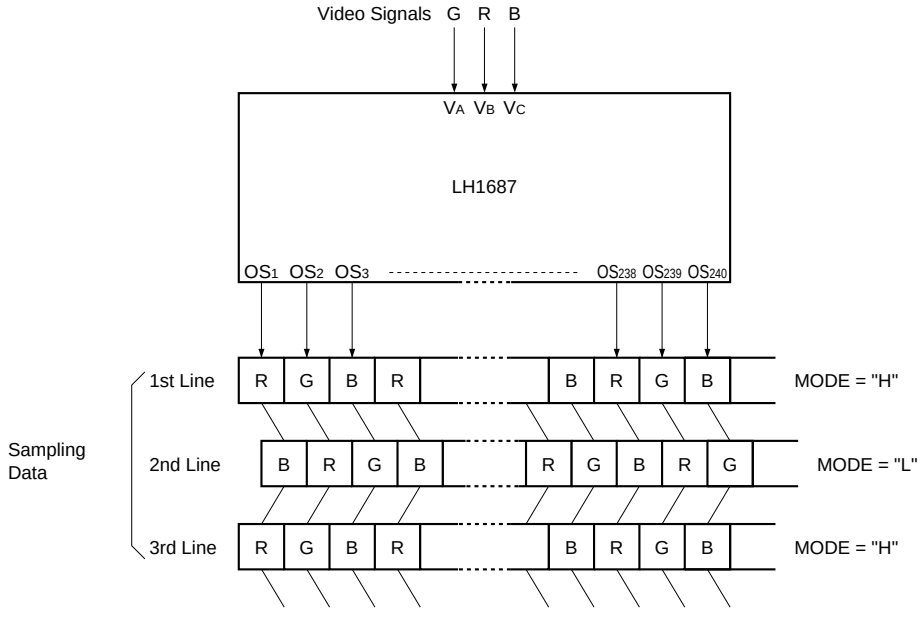
Video signal input pin	V_A	V_B	V_C
Video signal	G	R	B

Setting of video signals that are to be sampled by output circuits and MODE pin condition

	1st LINE	2nd LINE	3rd LINE	AFTER 4th LINE
OS (3n + 1)	R	R	R	R
OS (3n + 2)	G	G	G	G
OS (3n + 3)	B	B	B	B
MODE pin setting	"H"	"H"	"H"	"H"

(n = 0, 1, 2, ···, 79)

(b) Example of Delta Pixel Array Panel Connection



Connection of video signal input pins

Video signal input pin	V_A	V_B	V_C
Video signal	G	R	B

Setting of video signals that are to be sampled by output circuits and MODE pin condition

	1st LINE	2nd LINE	3rd LINE	AFTER 4th LINE
OS (3n + 1)	R	B	R	B and R are alternately selected.
OS (3n + 2)	G	R	G	R and G are alternately selected.
OS (3n + 3)	B	G	B	G and B are alternately selected.
MODE pin setting	"H"	"L"	"H"	"L" and "H" are alternately selected.

(n = 0, 1, 2, ···, 79)

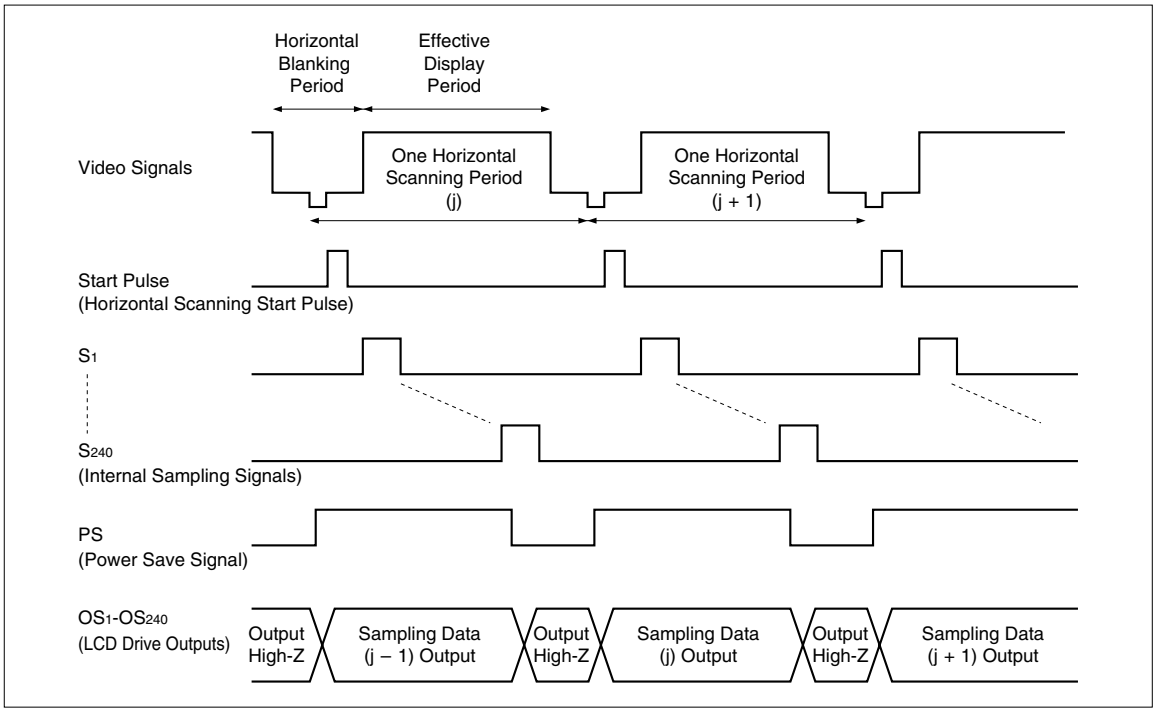
NOTES :

- Set the MODE pin condition during blanking period.
- Input the horizontal shift clock signal of CK pin by shifting the phase for each line according to the shift of the pixels connected to the same source bus line.
  If the pixels connected to the same source bus line are shifted by half the pixels, change the clock phase 90 degrees. Clock phase must be changed during blanking period.

Outline of Operation Timing

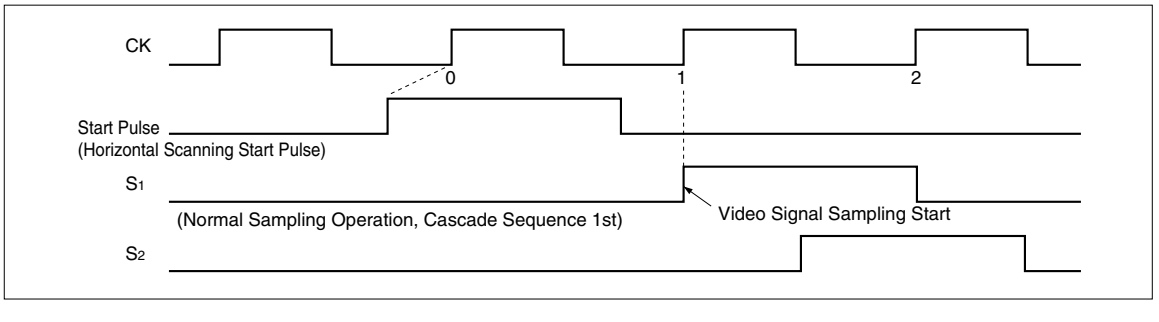
(1) Overall Operation Timing

Video signals of one horizontal scanning period are sampled into the sample and hold circuits at the timing of the internal sampling pulses of each output circuit, and data corresponding to the sampled data are output.



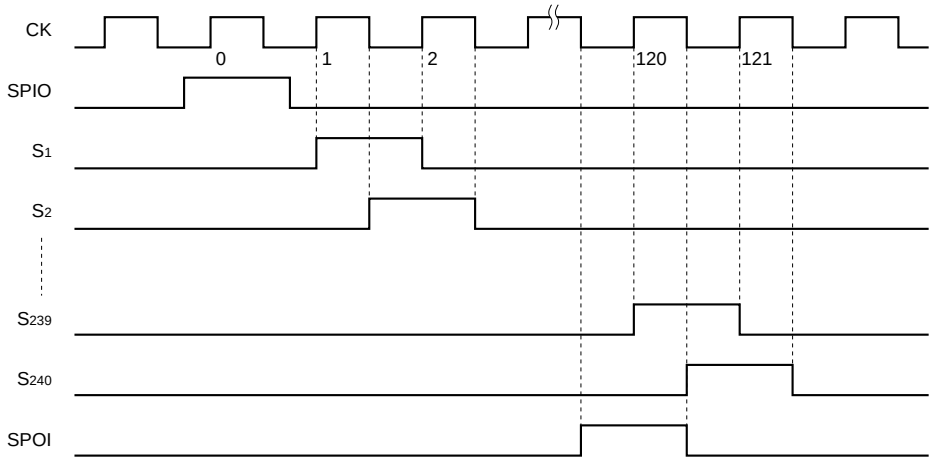
(2) Timing of Video Signal Sampling

If the normal sampling operation and cascade sequence is 1st, the video signal sampling (internal sampling signal Sn (n = 1, 2, ···, 240)) is started at the rising edge of first clock after falling edge of start pulse.



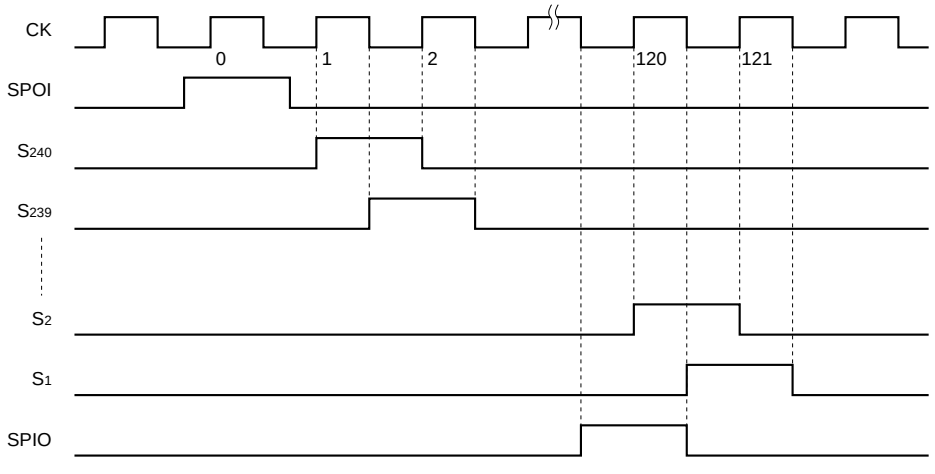
Timing Chart for Normal Sampling Operation

(1) When RL = "H"



NOTE : S_1 to S_{240} are internal sampling signals of video signal.

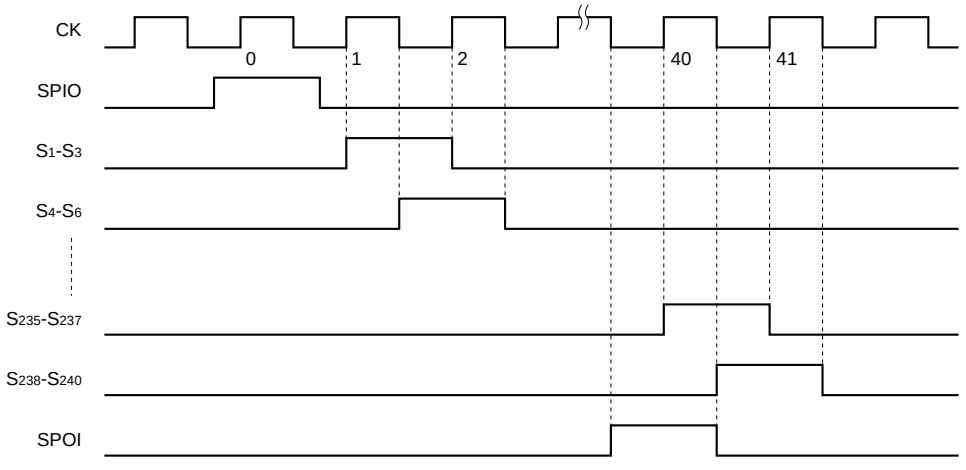
(2) When RL = "L"



NOTE : S_1 to S_{240} are internal sampling signals of video signal.

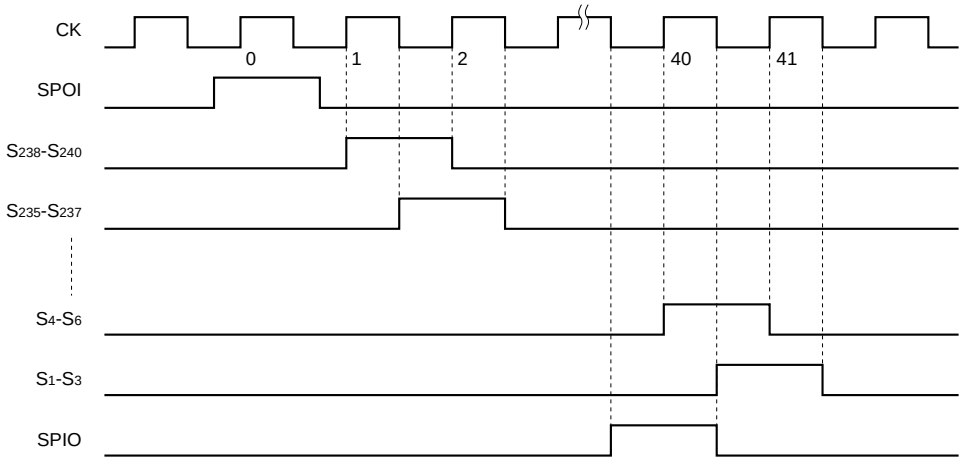
Timing Chart for 3-point Simultaneous Sampling Operation

(1) When RL = "H"



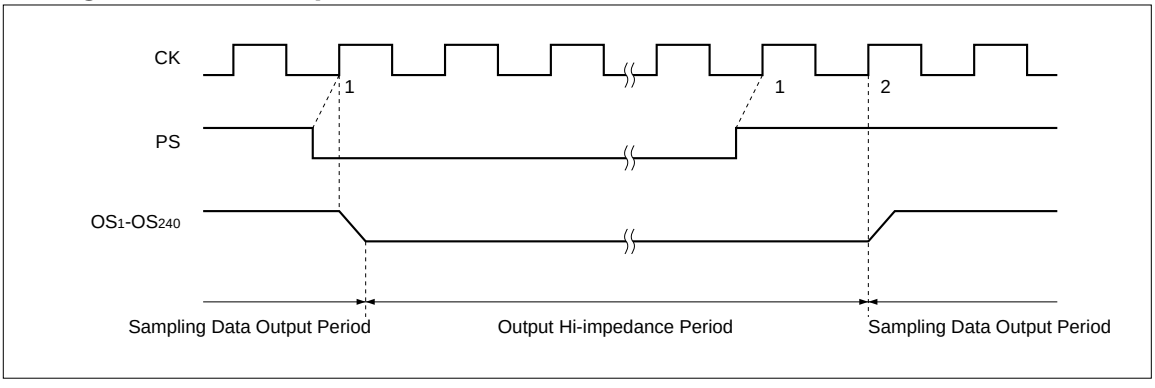
NOTE : S_1 to S_{240} are internal sampling signals of video signal.

(2) When RL = "L"

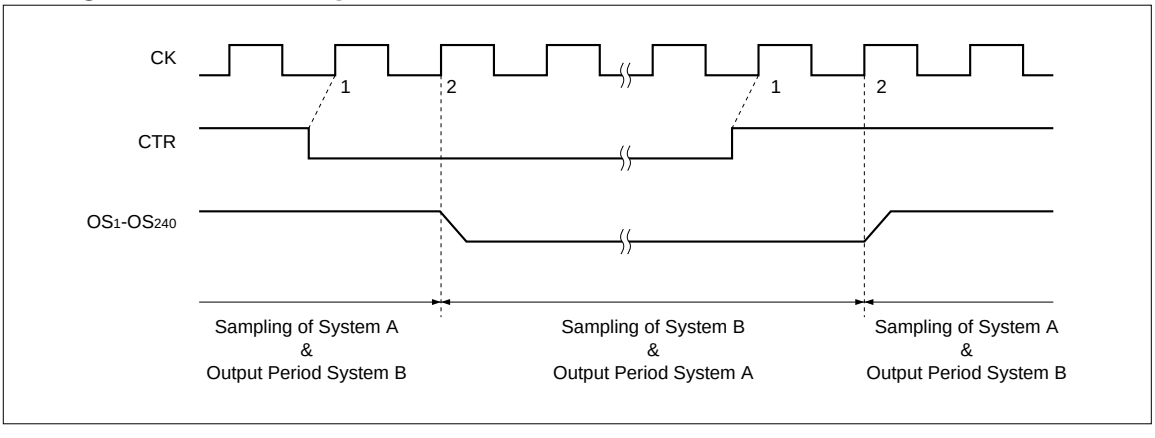


NOTE : S_1 to S_{240} are internal sampling signals of video signal.

Timing Chart for PS Operation



Timing Chart for CTR Operation



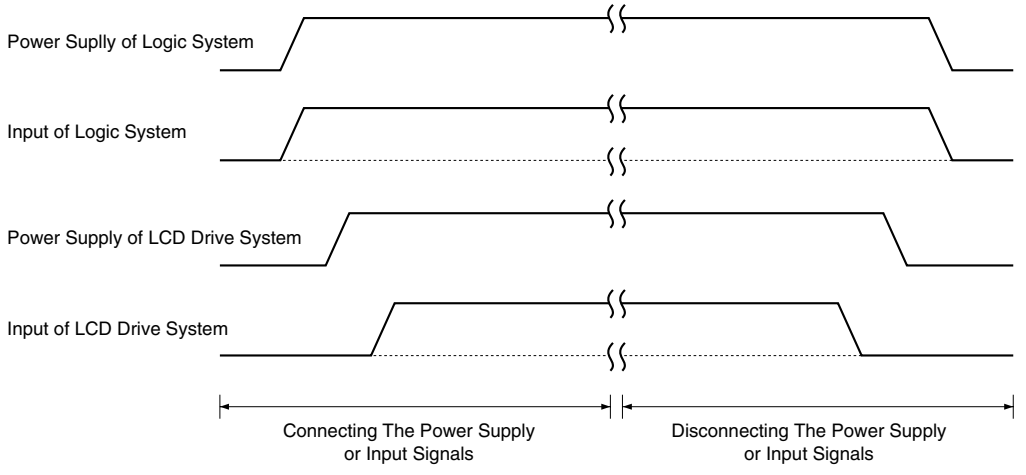
PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, set the logic system input pins (SPIO, SPOI, CK, CTR, MODE, SAME, RL, PS, TST_1, TST_2, TST_3, TST_4) after supplying the voltage to the logic system power supply pin ($V_{CC}L$), and next supplying the voltage to the LCD drive system power supply pin ($V_{CC}A$). Finally, set the LCD drive system input pins (V_A, V_B, V_C, TST_5).

When disconnecting the power supply, follow the reverse sequence.

When connecting or disconnecting the power supply follow the recommended sequence shown here.



Setting of Input pins

Since 5 pins of SPIO, SPOI, CK, CTR, and MODE of the input pins are not pulled up or pulled down in the IC, never use these 5 pins in the "OPEN" condition.

Since V_A, V_B, and V_C pins are for inputting video signals, necessary video signals must always be input.

Except for V_A, V_B, V_C, SPIO, SPOI, CK, CTR, and MODE, all other input pins are pulled up in the IC. However, to preventing malfunction due to noise etc., avoid using the "OPEN" condition whenever possible, and set to "H" level or "L" level.

Input video signals

Input video signals are target for analog signals (continuous signals).

The input band of video signals is applicable up to the maximum of 12.5 MHz.

Bypass capacitor

If the noise of a logic system is superposed on analog circuits such as the sample and hold circuits, analog characteristics (such as output voltage deviation and dynamic range, etc.) may deteriorate. For this reason, insert bypass capacitors of about 1 µF between V_{CC}L and GNDL, V_{CC}A and GNDA.

Fully evaluate and determine the value of bypass capacitors with them actually mounted on the LCD module.

Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	$V_{CC}L$	$V_{CC}L$	−0.3 to +7.0	V	1, 2
	$V_{CC}A$	$V_{CC}A$	−0.3 to +7.0	V	
Input voltage	$V_{IN}L$	CK, CTR, SPIO, SPOI, MODE, RL, SAM, PS, TST_1-TST_4	−0.3 to $V_{CC}L$ + 0.3	V	
	$V_{IN}A$	TST_5, V_A, V_B, V_C	−0.3 to $V_{CC}A$ + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to GNDL and GNDA (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	$V_{CC}L$	$V_{CC}L$	+3.0 to +5.5	V	1, 2
	$V_{CC}A$	$V_{CC}A$	+3.0 to +5.5	V	
Input voltage	$V_{IN}L$	CK, CTR, SPIO, SPOI, MODE, RL, SAM, PS, TST_1-TST_4	0 to $V_{CC}L$	V	
	$V_{IN}A$	TST_5, V_A, V_B, V_C	0 to $V_{CC}A$	V	
Operating temperature	T_{OPR}		−30 to +85	°C	

NOTES :

1. The applicable voltage on any pin with respect to GNDL and GNDA (0 V).
2. Ensure that voltages are set such that $V_{CC}L \leq V_{CC}A$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Unless otherwise specified, GNDL = GNDA = 0 V, V_{CCL} = +3.3 V, V_{CCA} = +5.0 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT.	NOTE
Input "Low" voltage	V_{IL}		CK, CTR, SPIO, SPOI,	0		0.3V_{CCL}	V	
Input "High" voltage	V_{IHL}		MODE, RL, SAM, PS	0.7V_{CCL}		V_{CCL}	V	
Input voltage	V_{INA}		V_A, V_B, V_C	0		V_{CCA}	V	
Input "Low" current	I_{IL1}	V_{IN} = 0 V	CK, CTR, SPIO, SPOI, MODE, V_A, V_B, V_C			10	µA	
	I_{IL2}		RL, SAM, PS			400	µA	
Input "High" current	I_{IHL}	V_{IN} = V_{CCL}	CK, CTR, SPIO, SPOI, MODE, RL, SAM, PS			10	µA	
	I_{IHA}	V_{IN} = V_{CCA}	V_A, V_B, V_C			10	µA	
Dynamic range	Vp-p		V_A, V_B, V_C	0.1		V_{CCA} − 0.1	V	
Deviations between output voltage pins	V_{OD}		OS_1-OS_{240}	−20		20	mV	1
Supply current (In operation mode)	I_{CCA1}		V_{CCA}		6.0		mA	2
Supply current (In power save mode)	I_{CCA2}					100	µA	3
Supply current	I_{CCL1}		V_{CCL}		1.5		mA	2

NOTES :

1. Start signal :
   Cycle t_{SP} = 63.5 µs, "H" period width t_{WSP} = 80 ns.
   CTR signal :
   Cycle t_{CTR} = 127.0 µs, "H" period width t_{WCTR} = 63.5 µs.
   Change from "H" to "L" or "L" to "H" is synchronized with start pulse during blanking period.
   CK signal :
   Frequency f_{CK} = 12.5 MHz (duty = 50%)
   V_A = V_B = V_C = 0.1 V to V_{CCA} − 0.1 V
   Connect all other pins to high level.
   Voltage difference between the average voltage of all OS output pins in the chip and the output voltage of each OS output pin. T_A = 25 °C
2. Start signal :
   Cycle t_{SP} = 63.5 µs, "H" period width t_{WSP} = 80 ns.
   CTR signal :
   Cycle t_{CTR} = 127.0 µs, "H" period width t_{WCTR} = 63.5 µs.
   Change from "H" to "L" or "L" to "H" is synchronized with start pulse during blanking period.
   CK signal :
   Frequency f_{CK} = 12.5 MHz (duty = 50%)
   Connect V_A, V_B, and V_C pins to V_{CCA}.
   Connect all other pins to high level.
3. Start signal :
   Cycle t_{SP} = 63.5 µs, "H" period width t_{WSP} = 80 ns.
   CTR signal :
   Cycle t_{CTR} = 127.0 µs, "H" period width t_{WCTR} = 63.5 µs.
   Change from "H" to "L" or "L" to "H" is synchronized with start pulse during blanking period.
   CK signal :
   Frequency f_{CK} = 12.5 MHz (duty = 50%)
   Pin to be set to GND : PS
   Connect V_A, V_B, and V_C pins to V_{CCA}.
   Connect all other pins to high level.

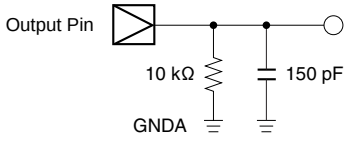
AC Characteristics

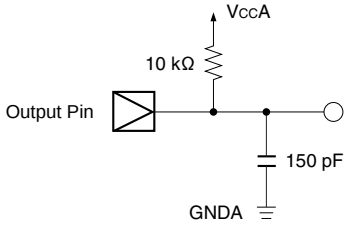
(Unless otherwise specified, GNDL = GNDA = 0 V, $V_{CC}L$ = +3.3 V, $V_{CC}A$ = +5.0 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Clock frequency	f_{CK}	SAM = "H"	CK			12.5	MHz	
		SAM = "L"				7.0	MHz	
"H" level clock width	t_{WHC}	SAM = "H"		30.0			ns	
		SAM = "L"		50.0			ns	
"L" level clock width	t_{WLC}	SAM = "H"		30.0			ns	
		SAM = "L"		50.0			ns	
Input rise time	t_{RC}	SAM = "H"	SPIO, SPOI, CK			10.0	ns	
		SAM = "L"				20.0	ns	
Input fall time	t_{FC}	SAM = "H"				10.0	ns	
		SAM = "L"				20.0	ns	
Start pulse width	t_{WSP}		SPIO, SPOI	$\frac{1}{f_{CK}}$			ns	
Start pulse setup time	t_{SUSP}		SPIO, SPOI, CK	10.0			ns	
Start pulse hold time	t_{HSP}			15.0			ns	
Start pulse output delay time	t_{DSP}	C_L = 15 pF				20.0	ns	
PS signal setup time	t_{SUPS}		PS	$\frac{1}{2f_{CK}}$			µs	
CTR signal setup time	t_{SUCTR}		CTR	$\frac{1}{2f_{CK}}$			µs	
Output transfer delay time	t_{DO}		OS_1-OS_{240}			5.0	µs	
Output rise time	t_R					5.0	µs	1
Output fall time	t_F					5.0	µs	
Power save delay time	t_{DOP}					3.0	µs	
Power save rise time	t_{ROP}					5.0	µs	2
Power save fall time	t_{FOP}					5.0	µs	

NOTES :

1. Start signal :
   Cycle t_{SP} = 63.5 µs, "H" period width t_{WSP} = 80 ns.
   CTR signal :
   Cycle t_{CTR} = 127.0 µs, "H" period width t_{WCTR} = 63.5 µs.
   Change from "H" to "L" or "L" to "H" is synchronized with start pulse during blanking period.
   CK signal :
   Frequency f_{CK} = 12.5 MHz (duty = 50%)
   Connect V_A, V_B, and V_C pins to $V_{CC}A$.
   Connect all other pins to $V_{CC}L$.
   Capacity of output load C_L = 150 pF
2. Add load resistor (10 kΩ) to NOTE 1.
   Load resistor is connected to GNDA or $V_{CC}A$ level as follows.





Timing Chart

