SC4611
Wide Input Range High Performance Synchronous Buck Switching Regulator

POWER MANAGEMENT

Description

SC4611 is a high performance synchronous buck controller that can be configured for a wide range of applications. The SC4611 utilizes synchronous rectified buck topologies where high efficiency is the primary consideration. It is optimized for applications involving multiple and redundant convertors connected together. The startup is asynchronous, which keeps the lower side FET off during soft start. This is a desired feature when a convertor is turned on with a preset external voltage or pre-bias voltage already present across its output. With the lower FET off, external bus is not discharged which avoids latch-up of modern ASIC circuits.

SC4611 comes with a rich set of features like regulated Vcc supply, soft start, power-good signaling, high current gate drivers, bootstrapped supply for driving high side N-channel MOSFETs, shoot through protection, frequency synchronization and the option for overvoltage crowbar. It also features multi mode overload protection that includes continuous current limiting, hiccup mode followed by latch off. The user has the option of bypassing the hiccup mode and latch off the output if required.

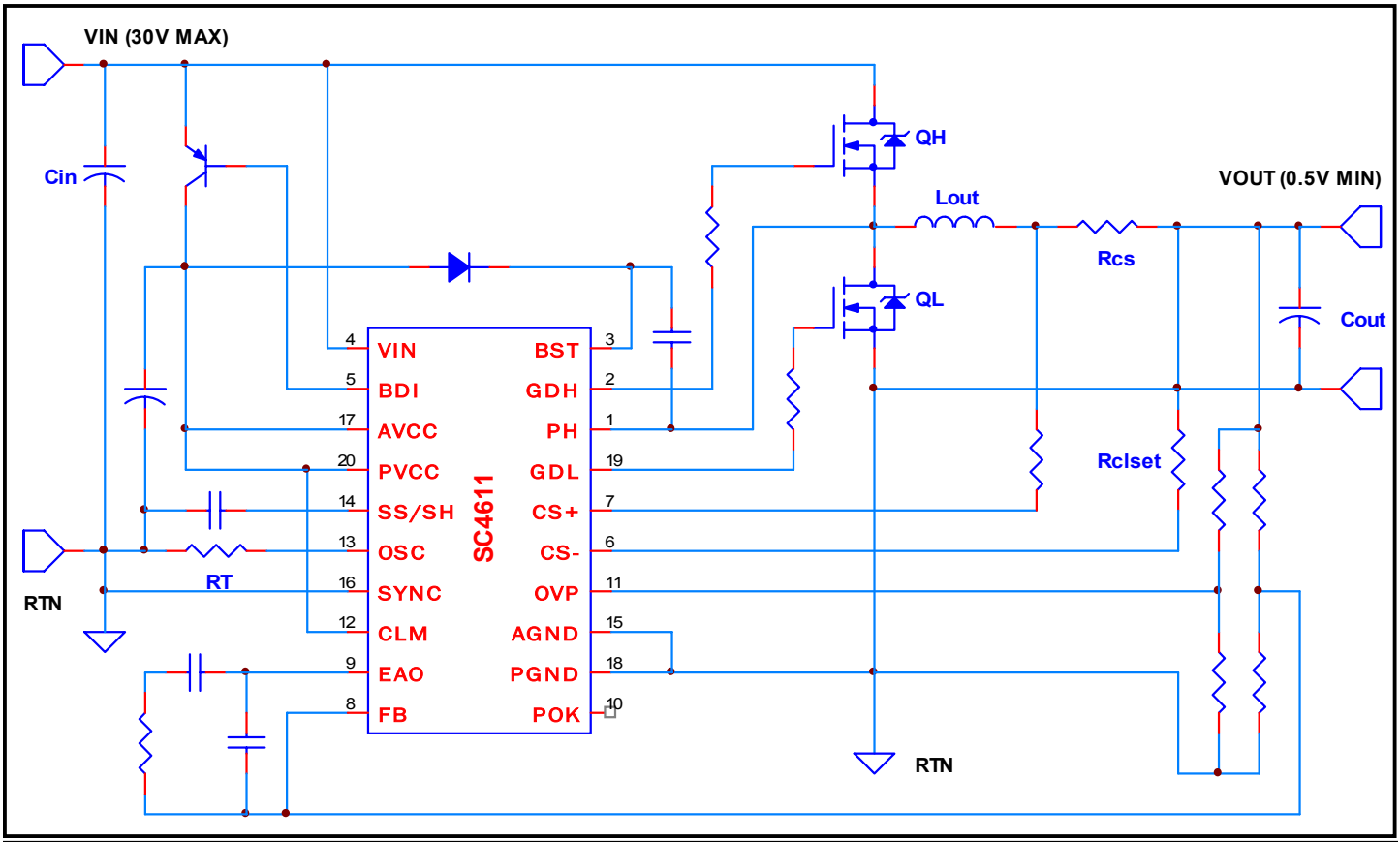
Features

- Wide input range, 4.5 to 30V
- Output voltage as low as 0.5V
- 2A output drive capability
- Asynchronous start up mode
- Multimode overcurrent protection with current limit, hiccup mode and latched shutdown
- Overvoltage crowbar protection
- Power OK signal
- Programmable frequency up to 1 MHz with external synchronization
- –40 to +85 degree C operating temperature
- Thermal shutdown
- Small package TSSOP-20

Applications

- Distributed power architectures
- Telecommunication equipment
- Servers/work stations
- Mixed signal applications
- Paralleled synchronous buck convertors
- Base station power management

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
BST to PGND	V_{BSTMAX}	37	V
VIN and BDI to PGND	V_{INMAX}	30	V
PVCC, AVCC to PGND	$AVCC_{MAX}$	7	V
PGND to AGND		±0.3	V
BST to PH		-0.3 to 7	V
GDH to PH, GDL to PGND	V_{GDHMAX}, V_{GDLMAX}	PVCC +0.3	V
All Other Pins to AGND		AVCC +0.3	V
GDH, GDL Source or Sink Current	I_{GDHMAX}, I_{GDLMAX}	2	A
Storage Temperature Range	T_{STGMAX}	-60 to +150	°C
Junction Temperature	T_{JMAX}	-40 to +125	°C
Lead Temperature (Soldering) 10 Sec.		260	°C

Electrical Characteristics

Unless specified: $T_A = T_J$ = -40 to +85°C, Vin = 12V, PVCC = AVCC = 6V, Fsw = 625 kHz, SS/SH = 5V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
AVCC	AVCC	VIN > 5.5V	4.5	6	6.5	V
PVCC	PVCC	VIN > 5.5V	4.5	6	6.5	V
Operating Current	I_{SUPPLY}	No load on GDH and GDL pins		7	10	mA
Quiescent Current	I_{QUI}	SS/SH = 0V		4	6	mA
Undervoltage Lockout						
Start Threshold	V_{UVLO}	AVCC Rising	4.0	4.2	4.4	V
UVLO Hysteresis				0.16		V
Soft Start/Shut Down						
Charge Current	I_{SSC}		4	7	10	µA
Discharge Current	I_{SSD}			0.5		mA
Disable Threshold Voltage				0.5		V
Disable Low to Shut Down (1)				50		nS

Electrical Characteristics (Cont.)

Unless specified: $T_A = T_J$ = -40 to +85°C, Vin = 12V, PVCC = AVCC = 6V, Fsw = 625 kHz, SS/SH = 5V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Frequency Range	Fsw		150		1000	kHz
Frequency	Fsw	R_T = 15K	550	625	700	kHz
Peak to Peak Ramp Voltage(1)	V_{RAMP}			3.0		V
SYNC Input High Pulse Width	T_{SYNC}		100			nS
SYNC Rise/Fall Time					50	nS
SYNC Frequency Range			Fsw		Fsw +15%	kHz
SYNC High/Low Threshold	V_{SYNC}			2.0		V
Error Amplifier						
Feedback Voltage	V_{FB}	T_A = 25 Deg C	0.493	0.5	0.507	V
Input Bias Current (1)				0.2		µA
Unity Gain Bandwidth (1)				3		MHz
Open Loop DC Gain (1)				90		dB
Output Source/Sink Current	I_{EAO}			+ 10		mA
Current Sense Comparator						
CS- pin offset current (ILIM ADJ)	I_{CS-}	RT = 15K Rclset = 1K	66	82	98	µA
Current limit sense threshold	V_{CL}		66	82	98	mV
Current limit hysteresis				30		%
Power Good and Overvoltage Protection						
FB Level for Output High Sense	V_{LTH}		0.52	0.55	0.58	V
Hysteresis (1)				6		mV
FB Level for Output Low Sense	V_{HTH}		0.42	0.45	0.48	V
Hysteresis (1)				6		mV
PWR OK Output Low Level	V_{POK}	I_{POK} = 0		0.2		V
OVP Trip Reference	V_{OVP}		0.475	0.5	0.525	V

(1) Guaranteed by design. Not tested in production.

Electrical Characteristics (Cont.)

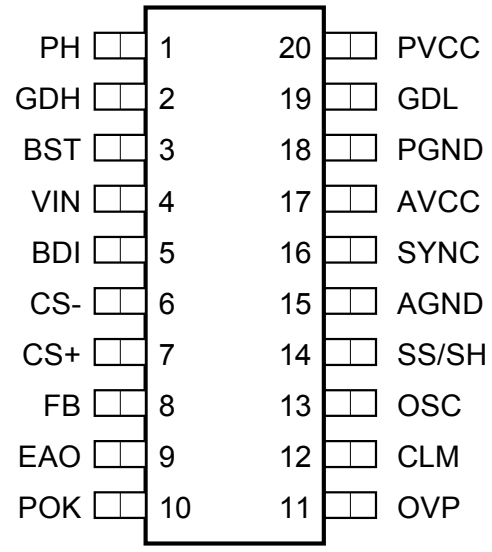
Unless specified: $T_A = T_J$ = -40 to +85°C, Vin = 12V, PVCC = AVCC = 6V, Fsw = 625 kHz, SS/SH = 5V

Parameter	Symbol	Test Conditions	Min	Typ	Min	Units
Duty Cycle						
Maximum Duty Cycle	Dmax	Fsw = 150 kHz		90		%
		Fsw = 1 MHz		80		%
Minimum Pulse Width (1)	Tpulsemin			150		nS
Output						
Gate Drive ON-Resistance (H)	R_{ONGDH}	I_{SOURCE} = 20 mA		2		Ω
Gate Drive OFF-Resistance (H)	R_{OFFGDH}	I_{SINK} = 20 mA		1		Ω
Gate Drive ON-Resistance (L)	R_{ONGDL}	I_{SOURCE} = 20 mA		2		Ω
Gate Drive OFF-Resistance (L)	R_{OFFGDL}	I_{SINK} = 20 mA		1		Ω
Rise Time	Trise	C_{OUT} = 2000 pF		15		nS
Fall Time	Tfall	C_{OUT} = 2000 pF		15		nS
Dead Time Between Drive Signals (1)				30		nS

NOTES:
(1) Guaranteed by design. Not tested in production.
(2) This device is ESD sensitive. Use of standard ESD handling precautions is required

Pin Configuration

TOP VIEW



(20 Pin TSSOP)

Ordering Information

Part Number	Package	Temp. Range
SC4611ITSTRT (2)	TSSOP-20 (1)	-40°C to +85°C

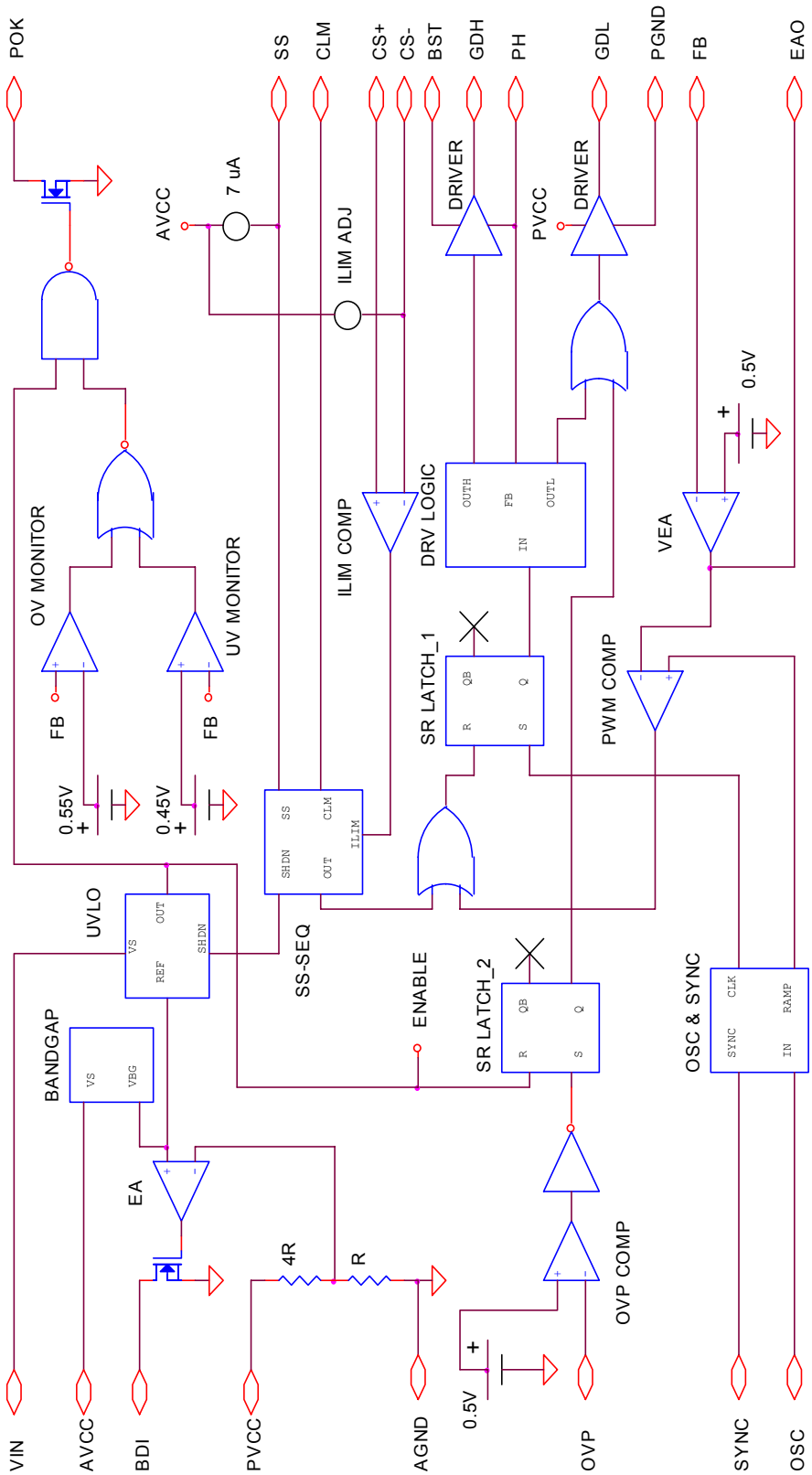
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) Lead free device. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	PH	Switching junction of high side Mosfet source and low side Mosfet drain.
2	GDH	Gate drive output for high side N-Channel MOSFET.
3	BST	Boost capacitor connection for the high side gate drive. Connect an external capacitor and a diode as shown in the Typical Application Circuit.
4	VIN	Input supply voltage.
5	BDI	Base drive for AVCC/PVCC regulator.
6	CS-	Inverting input for the current sense comparator
7	CS+	Non inverting input for the current sense comparator
8	FB	Feedback input pin.The reference level is 0.5V
9	EAO	Error amplifier output for compensation.
10	POK	Open drain of power good output.
11	OVP	Overvoltage protection input. The reference level is 0.5V
12	CLM	Current Limit Mode select input. Connect to AVCC to enable hiccup or connect to AGND to bypass hiccup mode.
13	OSC	Connect a resistor to AGND for programming the oscillator frequency.
14	SS/SH	Soft start pin. Hold low to shutdown the device.
15	AGND	Analog signal ground.
16	SYNC	Oscillator synchronization pin. Connect to AGND if not used.
17	AVCC	Supply voltage for analog circuitry.
18	PGND	Power ground.
19	GDL	Gate drive output for the low side N-Channel MOSFET.
20	PVCC	Supply voltage for output drivers.

Block Diagram - SC4611



Applications Information

INTRODUCTION

The SC4611 is designed to control and drive N-Channel MOSFET synchronous rectified buck convertors. The switching frequency is programmable to optimize design. The SC4611 switching regulator section features external current sensing and provides a hiccup mode overcurrent protection followed by a latched shutdown. It is also optimized for multiple convertors operating in parallel redundant mode.

POWERING THE CONTROLLER

Supplies VIN, PVCC and AVCC from the input source are used to power the SC4611. The VIN supply provides the bias for the internal reference and UVLO circuitry. The AVCC supply provides the bias for the oscillator, PWM switcher, voltage feedback, current sense and the Power OK circuitry. PVCC is used to drive the low and high side MOSFET gates.

An external PNP transistor can be set up as a linear regulator to generate well regulated AVCC and PVCC as shown in the Typical Application Circuit. The maximum current into the BDI pin should be limited to 5 mA under all conditions. For example if an external PNP transistor is used with Vin less than 7V, the BDI pin will saturate and pull down the Vin input. A series resistor between the base of the external PNP transistor and the BDI should be used to limit the current into the BDI pin.

The VCC pins have an absolute maximum rating of 7V. If maximum VIN is less than 7V it may be connected directly to AVCC and PVCC, leaving the BDI pin open.

START UP SEQUENCE

Start up is inhibited until AVCC input reaches its UVLO threshold. The UVLO limit is 4.2V typical. The power up sequence is initiated by a 7 uA current source charging the soft start capacitor connected to the SS pin. When the SS pin reaches 1V, the converter will start switching. The reference input of the error amplifier is ramped up with the soft-start signal, level shifted down by 1V. Initially only the high side driver is enabled. Keeping the low side MOSFET off during start up is useful where multiple convertors are operating in parallel. It prevents forward conduction in the freewheeling MOSFET which might otherwise cause a dip in the common output bus.

When the SS pin reaches 2V, the low side MOSFET will begin to switch and the convertor is fully operational in the synchronous mode. The reference input of the error amplifier is released and the SS pin is pulled up to AVCC. The soft start duration is controlled by the value of the SS cap. If the SS pin is pulled below 0.5V, the device is disabled and draws only 4 mA current.

Note that the SS pin threshold for soft-start is supply dependant and defined above for AVCC = 6V. If AVCC is lower, the threshold should be reduced proportionately, i.e. SS enable threshold will be 0.375V when AVCC = 4.5V.

GATE DRIVERS

The low side gate driver is supplied from PVCC and provides a peak source/sink current of 2A. The high side gate drive is also capable of sourcing and sinking peak currents of 2A. Protection logic provides a 30 nS dead time to ensure both the upper and lower MOSFETs will not turn on simultaneously and cause a shoot through condition.

The high side MOSFET gate drive can be provided by an external 12V supply that is connected from BST to GND. The actual gate to source voltage of the upper MOSFET will approximately equal 6V (12V-VCC). If the external 12V supply is not available, a classical bootstrap technique can be implemented from the PVCC supply. A bootstrap capacitor is connected from BST to Phase while PVCC is connected through a diode (Low V_F Schottky or ultrafast diode) to the BST. This will provide a gate to source voltage approximately equal to the VCC-Vdiode drop.

OSCILLATOR

The switching frequency fsw of the SC4611 is set by an external resistor using the following formula:

$$RT = \frac{9375}{Fsw}$$

R_T is in kOhm and fsw is in kHz. This relation is a first order approximation of the more complex relationship between RT and Fsw. The oscillator can be synchronised to an external clock that is nominally *faster* than the internal frequency set by $R_{OSC.}$ The external voltage level applied should be lower than AVCC of the device.

OVERCURRENT PROTECTION

SC4611 includes a precision current sense comparator for maximum flexibility. The current feedback can be taken either from the output inductor for lossless sensing and better efficiency, or from a series resistor for improved accuracy. An offset current of $1.225/R_T$ pulls up on the CS- pin, providing an offset voltage across a resistance on the input to this pin. The offset voltage should be set to > 50 mV. A voltage across the current sense resistor of greater than this value will produce a current limit pulse. There is 30% hysteresis on the offset current. Since the offset current into CS- is set by R_T, the current limit needs to be adjusted if the frequency setting is changed. Note that the operational limit for CS- and CS+ inputs is 0.5V below the AVCC supply.

The first stage of protection against overloads is peak current limiting on a pulse by pulse basis. Once an overload is sensed, the high side FET is turned off and held low for the rest of the cycle. This provides peak current limiting on a pulse by pulse basis. The final response of the device to a severe overload can be programmed using the CLM pin. If the CLM pin is connected to AVCC, the hiccup mode is enabled. A soft-start/hiccup cycle is initiated if 64 current limit pulses are detected in any counting period of 128 oscillator cycles. The SS capacitor is discharged with a 0.6 mA sink current. There will be 3 dummy soft-starts, i.e. the SS pin will be pulled up to 2V and then discharged to < 1V. This will be repeated 7 times, and if the overload persists the part will be latched off on the eighth attempt. Reset is by recycling the input power. During the hiccups, the device will operate in asynchronous mode, just as in the power-up sequence.

In some cases the repeated soft start cycling may not be desirable, depending on the nature of load. If the CLM is taken low to AGND, the hiccup mode will be skipped. When an overcurrent event occurs a comparator detects it and puts out a signal into a latch counter. The counter keeps track of the number of current-limit pulses and is reset after every 128 oscillator cycles. If 64 current-limit pulses are detected in any counting period of 128 cycles, the SS pin will be pulled low. The device is latched off until power is recycled. The CLM pin should be connected to either AGND or AVCC at all times and should not be left open.

POWER OK MONITOR

The power OK circuitry monitors the FB input of the error amplifier. If the voltage on this input goes above 0.55V or below 0.45V the POK pin is pulled low. The POK is an open drain output and is held low until the end of the startup sequence i.e. till the SS pin reaches 2V or more.

OVERVOLTAGE AND THERMAL PROTECTION

The overvoltage input can be connected to OVP pin with a low reference of 0.5V. If this feedback exceeds the reference the low side FET is continuously gated on to crowbar the input VIN. This feature may be used to protect the load from possible overvoltage in case the high side FET fails and shorts. The crowbar current in the power devices is limited only by the source of VIN.

SC4611 also incorporates thermal protection. If the chip temperature exceeds approximately 150 Deg C, the outputs are shutdown.

ERROR AMPLIFIER DESIGN

SC4611 is a voltage mode buck controller that utilizes an externally compensated high bandwidth error amplifier to regulate output voltage. The power stage of the synchronous rectified buck converter control-to-output transfer function is as shown below:

$$G_{VD}(s) = \frac{V_{IN}}{V_S} \times \left(\frac{1 + sESR_C C}{1 + s\frac{L}{R_L} + s^2 LC} \right)$$

where,

V_{IN} – Input voltage
R_L – Load resistance
L – Output inductance
C – Output capacitance
ESR_C – Output capacitor ESR
V_S – Peak to peak ramp voltage

Applications Information (Cont.)

The classical Type III compensation network can be built around the error amplifier as shown below

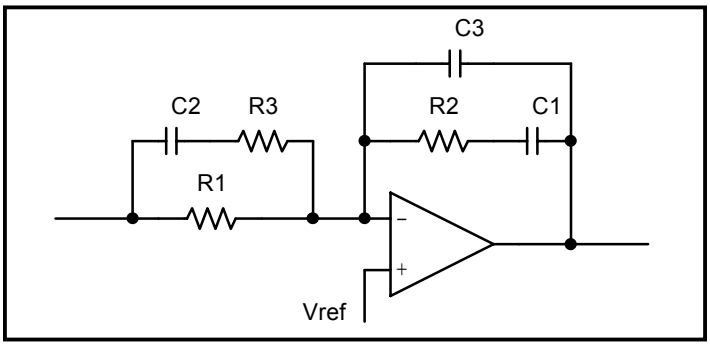


Figure 1. Voltage Mode Buck Converter Compensation Network

The transfer function of the compensation network is as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{(1+\frac{s}{\omega_{Z1}})(1+\frac{s}{\omega_{Z2}})}{(1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_{P2}})}$$

where,

$$\omega_{Z1} = \frac{1}{R_2 C_1}, \quad \omega_{Z2} = \frac{1}{(R_1+R_3)C_2}$$

$$\omega_I = \frac{1}{R_1(C_1+C_3)}, \quad \omega_{P1} = \frac{1}{R_3 C_2}, \quad \omega_{P2} = \frac{1}{R_2 \frac{C_1 C_3}{C_1+C_3}}$$

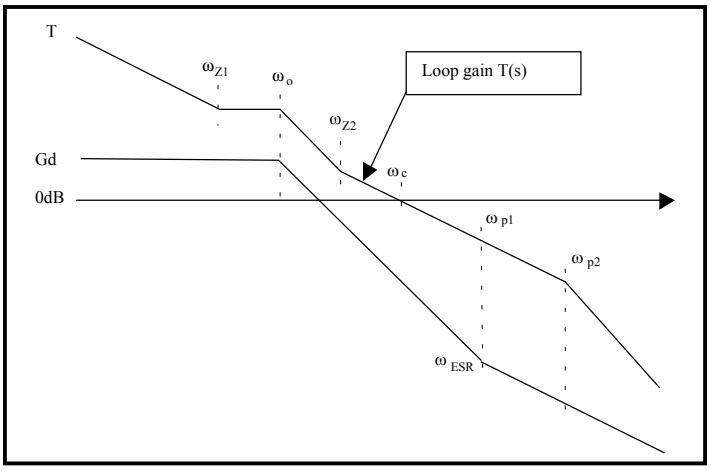


Figure 2. Simplified asymptotic diagram of buck power stage and its compensated loop gain.

The design guidelines are as following:

1. Set the loop gain crossover frequency w_c for given switching frequency.

2. Place an integrator in the origin to increase DC and low frequency gains.

3. Select w_{Z1} and w_{Z2} such that they are placed near w_0 to dampen peaking; the loop gain has –20 dB rate to go across the 0 dB line for obtaining a wide bandwidth.

4. Cancel w_{ESR} with compensation pole w_{P1} ($w_{P1} = w_{ESR}$).

5. Place a high frequency compensation pole w_{P2} at half the switching frequency to get the maximum attenuation of the switching ripple and the high frequency noise with the adequate phase lag at w_c.

PCB LAYOUT FOR SC4611

Careful attention to layout requirements is necessary for successful implementation of the SC4611 PWM controller. High switching currents with fast rise and fall times are present in the application and their effect on ground plane voltage differentials must be understood and minimized. A good layout with minimum parasitic loop areas will

a) reduce EMI

b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and

c) minimize source ringing, resulting in more reliable gate switching signals.

LAYOUT GUIDELINES

In the following Q_T and Q_B denote the high side and low side MOSFETs respectively.

1) A ground plane should be used. The number and position of ground plane interruptions should be minimised so as not to compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents into particular paths, such as the output capacitor or the Q_B source.

Applications Information (Cont.)

2). The high power, high current parts of the circuit should be laid out first. The on time loop formed by the input capacitor Cin, the high side FET Q_T, the output inductor and the output capacitor bank Cout must be kept as small as possible. Another loop area to minimise is formed by low side FET Q_B, the output inductor and the output capacitor bank Cout during the off period. These loops contain all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance.

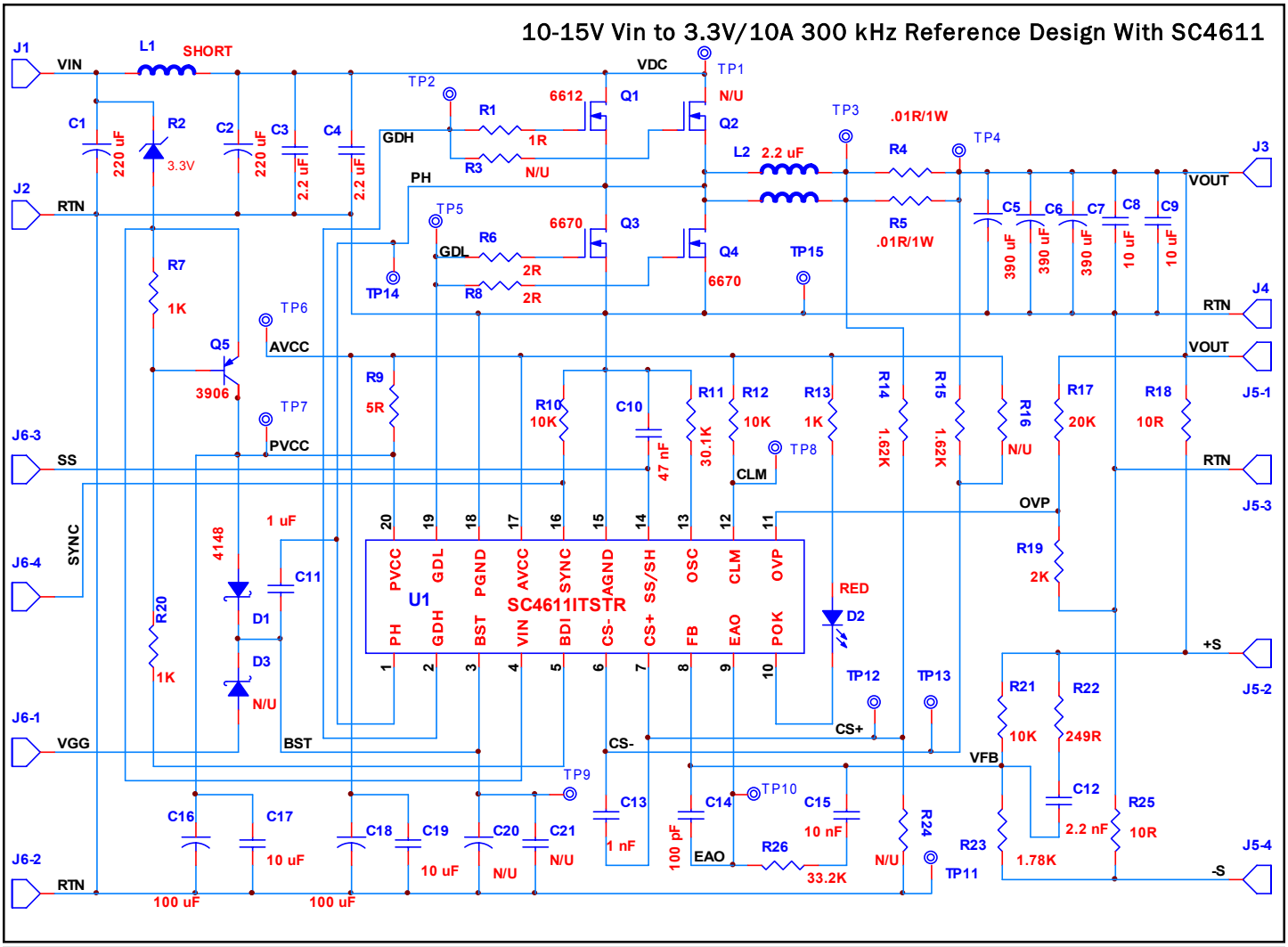
3). The connection between the junction of Q_T, Q_B and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short. The top FET gate charge currents flow in this trace.

4) The output capacitor Cout should be located as close to the load terminals as possible. Fast transient load currents are supplied by Cout and connections between Cout and the load must be kept short with wide copper areas to minimize inductance and resistance. This will improve the transient response to step loads.

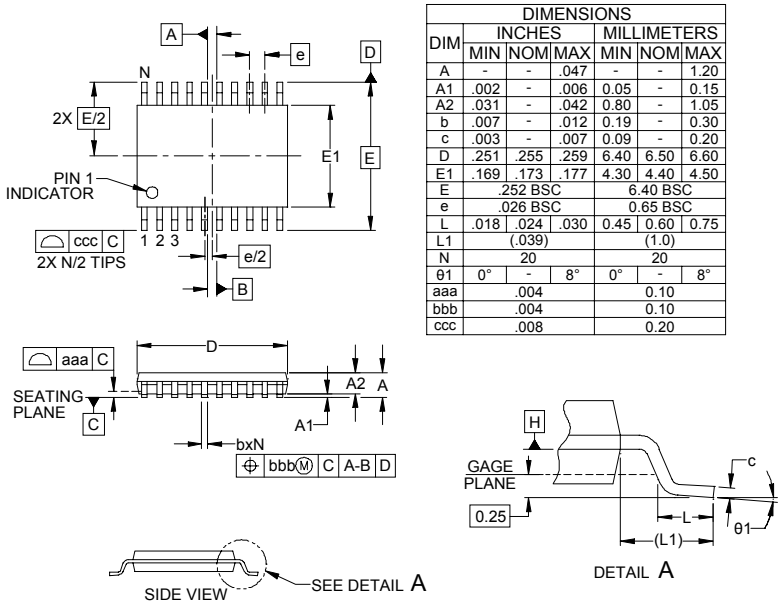
5) The SC4611 is best placed over a quiet ground plane area. Avoid pulse currents of the Cin, Q_T, Q_B loop flowing in this area. This analog ground plane should be connected to the power ground plane at a "quiet" point near the input capacitor. Under no circumstance should it be returned to a point inside the Cin, Q_T, Q_B, Cout power ground loops.

6) The SC4611 AGND pin is connected to the separate analog ground plane with minimum lead length . All analog grounding paths including decoupling capacitors, feedback resistors, compensation components, and current-limit setting resistors should be connected to the same plane.

3.3V/10A Evaluation Board Schematic



Outline Drawing - TSSOP-20

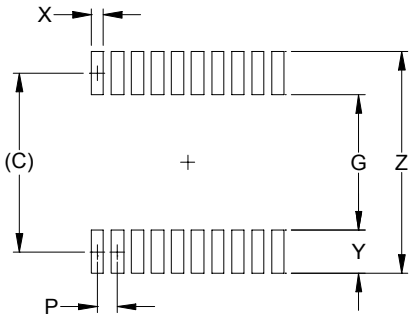


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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