NST489AMT1, NSVT489AMT1G

High Current Surface Mount NPN Silicon Low $V_{CE(sat)}$ Switching Transistor for Load Management in Portable Applications

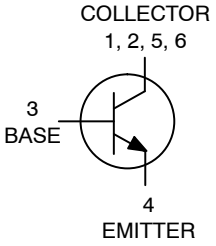
ON Semiconductor®

http://onsemi.com

30 VOLTS, 3.0 AMPS NPN TRANSISTOR



TSOP−6
CASE 318G
STYLE 6



Features

- AEC−Q101 Qualified and PPAP Capable
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- Pb−Free Packages are Available*

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	50	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current − Continuous	I_C	2.0	A
Collector Current − Peak	I_{CM}	3.0	A

THERMAL CHARACTERISTICS

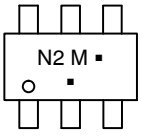
Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	 535 4.3	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	 234	 °C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	 1.180 9.4	 W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	 106	 °C/W
Thermal Resistance, Junction−to−Lead #1	$R_{\theta JL}$ (Note 1) $R_{\theta JL}$ (Note 2)	110 50	°C/W °C/W
Total Device Dissipation (Single Pulse < 10 s)	$P_{Dsingle}$ (Notes 2 and 3)	 1.75	 W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 with 1 oz and 3.9 mm^2 of copper area.
2. FR−4 with 1 oz and 645 mm^2 of copper area.
3. Refer to Figure 8.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DEVICE MARKING



N2 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NST489AMT1	TSSOP−6	3,000 / Tape & Reel
NST489AMT1G	TSSOP−6 (Pb−Free)	3,000 / Tape & Reel
NSVT489AMT1G	TSSOP−6 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2011

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector – Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)		$V_{(BR)CEO}$	30	–	–	V
Collector – Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	V
Emitter – Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)		$V_{(BR)EBO}$	5.0	–	–	V
Collector Cutoff Current (V_{CB} = 30 V, I_E = 0)		I_{CBO}	–	–	0.1	μA
Collector–Emitter Cutoff Current (V_{CES} = 30 V)		I_{CES}	–	–	0.1	μA
Emitter Cutoff Current (V_{EB} = 4.0 V)		I_{EBO}	–	–	0.1	μA
ON CHARACTERISTICS						
DC Current Gain (Note 4)	(I_C = 1.0 mA, V_{CE} = 5.0 V) (I_C = 0.5 A, V_{CE} = 5.0 V) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	300 300 200	– 500 –	– 900 –	
Collector – Emitter Saturation Voltage (Note 4)	(I_C = 1.0 A, I_B = 100 mA) (I_C = 0.5 A, I_B = 50 mA) (I_C = 0.1 A, I_B = 1.0 mA)	$V_{CE(sat)}$	– – –	0.10 0.06 0.05	0.200 0.125 0.075	V
Base – Emitter Saturation Voltage (Note 4) (I_C = 1.0 A, I_B = 0.1 A)		$V_{BE(sat)}$	–	–	1.1	V
Base – Emitter Turn–on Voltage (Note 4) (I_C = 1.0 A, V_{CE} = 2.0 V)		$V_{BE(on)}$	–	–	1.1	V
Cutoff Frequency (I_C = 100 mA, V_{CE} = 5.0 V, f = 100 MHz		f_T	200	300	–	MHz
Output Capacitance (f = 1.0 MHz)		C_{obo}	–	–	15	pF

4. Pulsed Condition: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

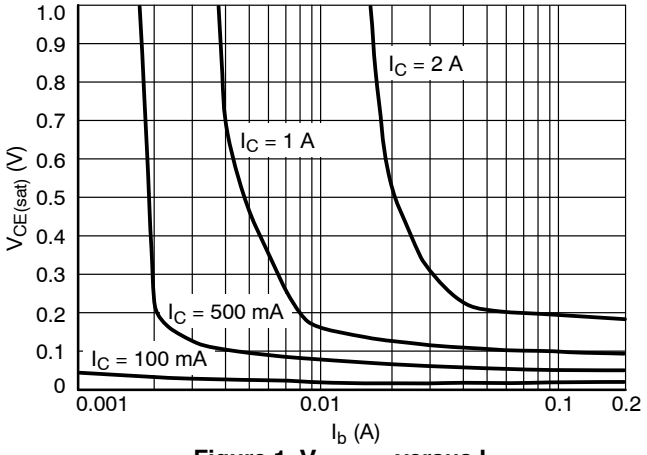


Figure 1. $V_{CE\ (sat)}$ versus I_b

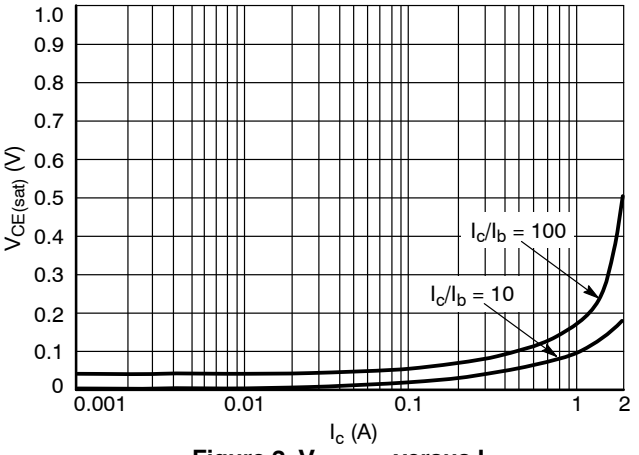


Figure 2. $V_{CE\ (sat)}$ versus I_c

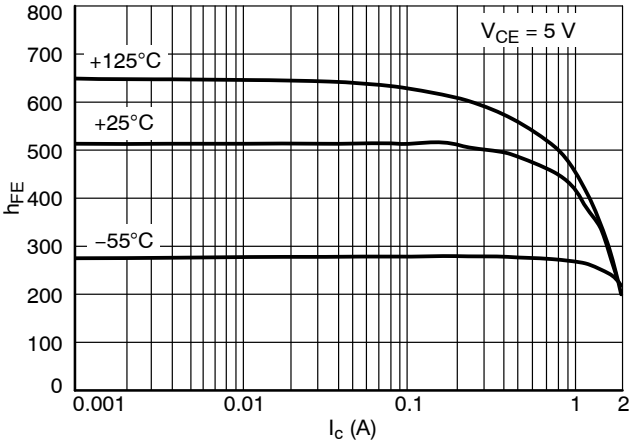


Figure 3. h_{FE} versus I_c

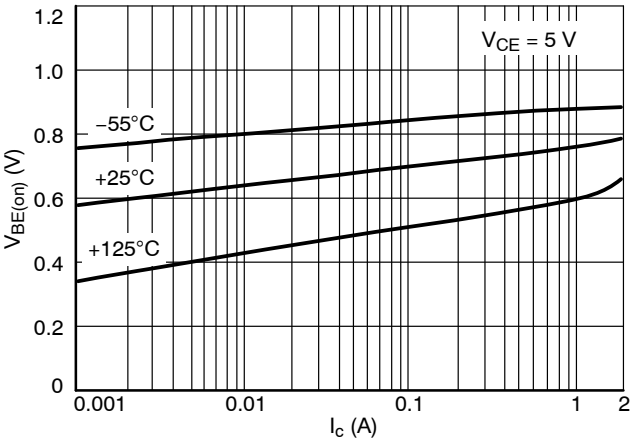


Figure 4. $V_{BE(on)}$ versus I_c

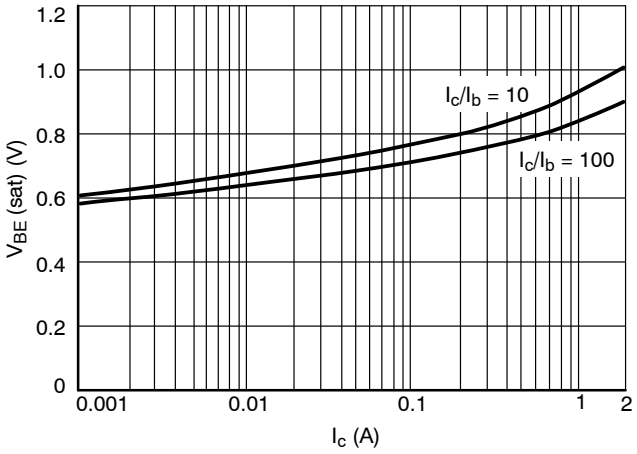


Figure 5. $V_{BE(sat)}$ versus I_c

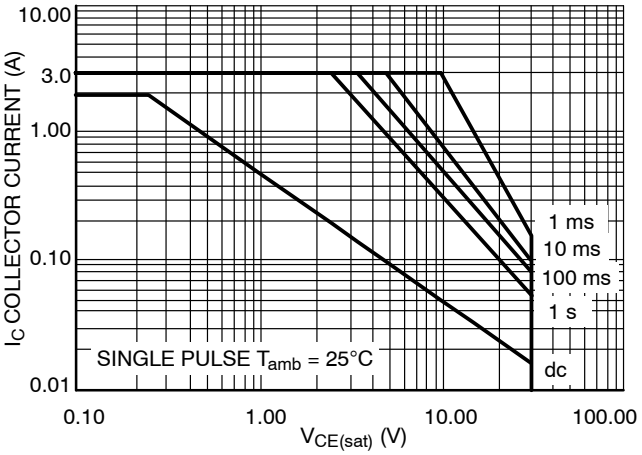


Figure 6. Safe Operating Area

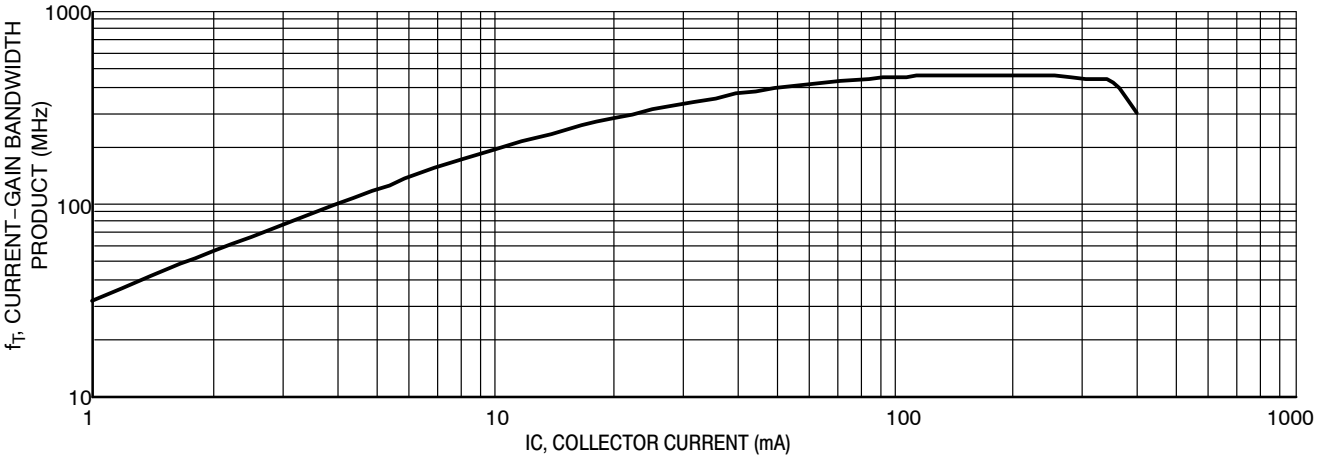


Figure 7. f_T (MHZ) versus I_C (mA) V_{CE} = 5.0 V

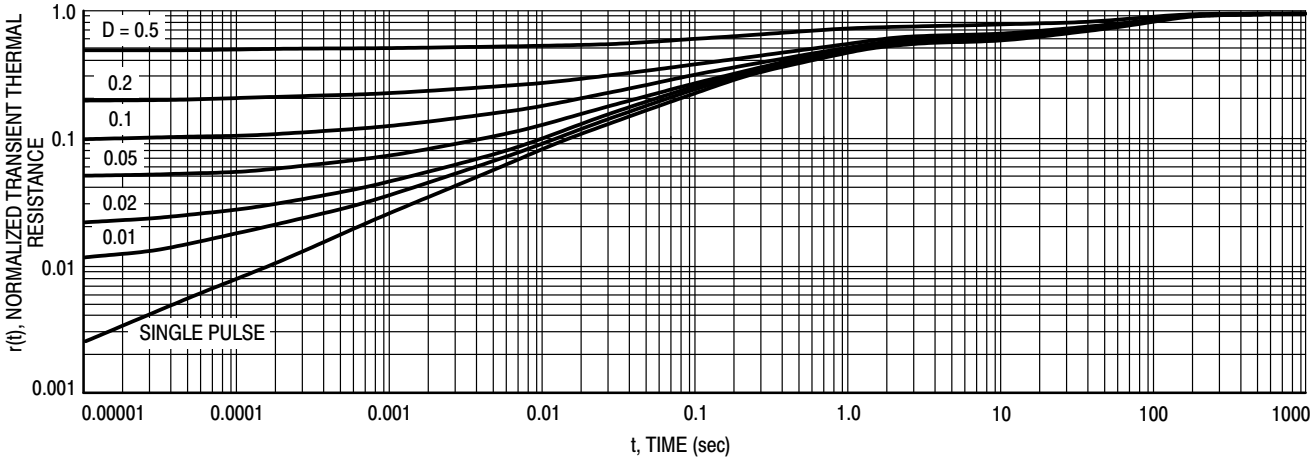
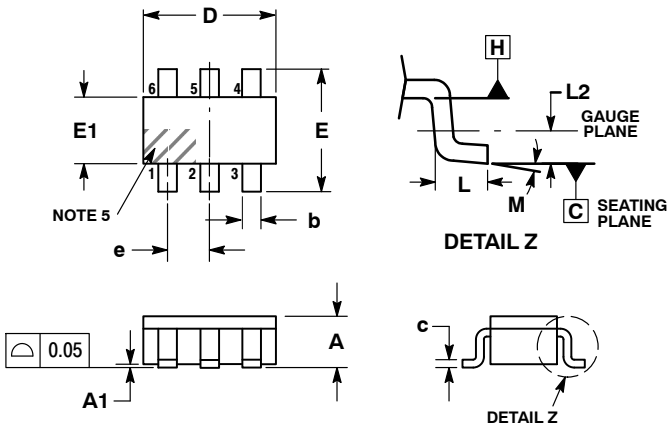


Figure 8. Normalized Thermal Response

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE U

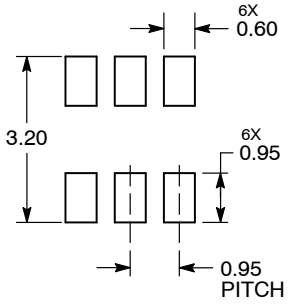


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NST489AMT1/D