MJD243 (NPN), MJD253 (PNP)

Complementary Silicon Plastic Power Transistor

DPAK−3 for Surface Mount Applications

Designed for low voltage, low−power, high−gain audio amplifier applications.

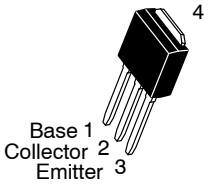
Features

- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 100 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain −
  h_{FE} = 40 (Min) @ I_C = 200 mAdc = 15 (Min) @ I_C = 1.0 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("−1" Suffix)
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc = 0.6 Vdc (Max) @ I_C = 1.0 Adc
- High Current−Gain − Bandwidth Product −
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage −
  I_{CBO} = 100 nAdc @ Rated V_{CB}
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- These are Pb−Free Packages

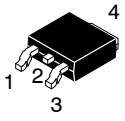
ON Semiconductor®

http://onsemi.com

4.0 A, 100 V, 12.5 W
POWER TRANSISTOR

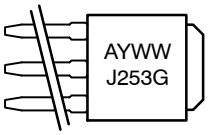


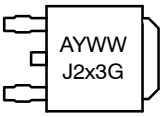
DPAK−3
CASE 369D
STYLE 1



DPAK−3
CASE 369C
STYLE 1

MARKING DIAGRAMS





A = Assembly Location
Y = Year
WW = Work Week
x = 4 or 5
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Base Voltage	V_{CB}	100	Vdc
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current −Continuous −Peak	I_C	4.0 8.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	W W/°C
Total Device Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	1.4 0.011	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted on minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	− −	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	−	100	nAdc
DC Current Gain (Note 3) (I_C = 200 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40 15	180 −	−
Collector−Emitter Saturation Voltage (Note 3) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	− −	0.3 0.6	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	−	1.8	Vdc
Base−Emitter On Voltage (Note 3) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 4) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	−	50	pF

2. When surface mounted on minimum pad sizes recommended.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$.

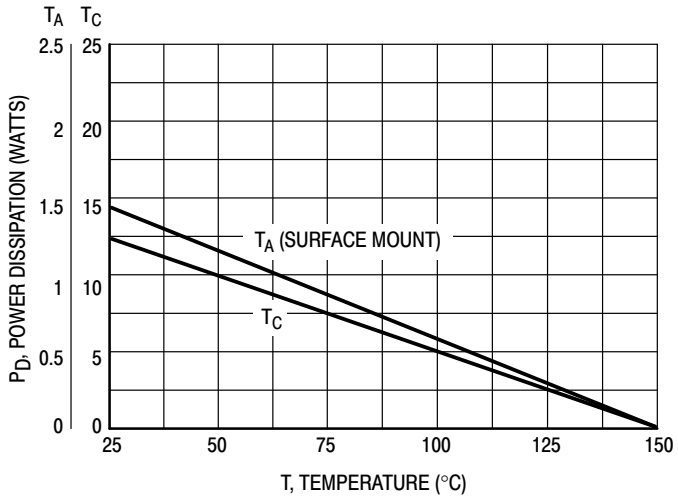


Figure 1. Power Derating

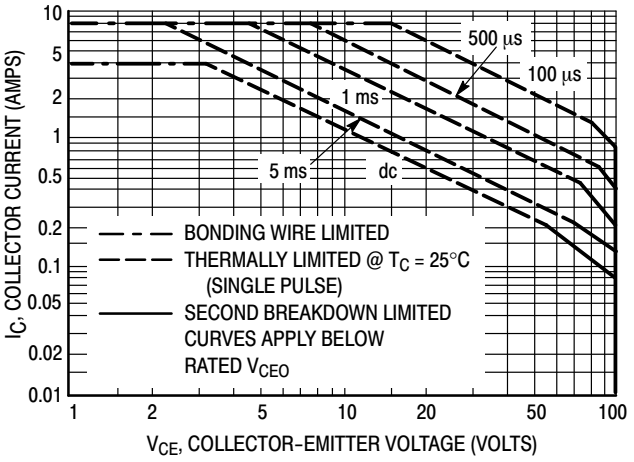


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

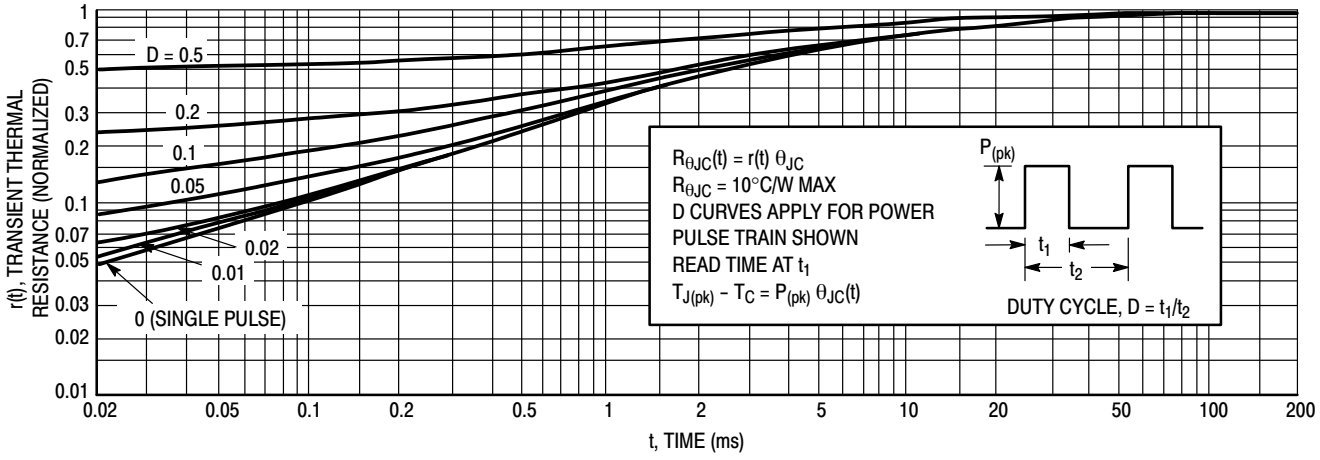
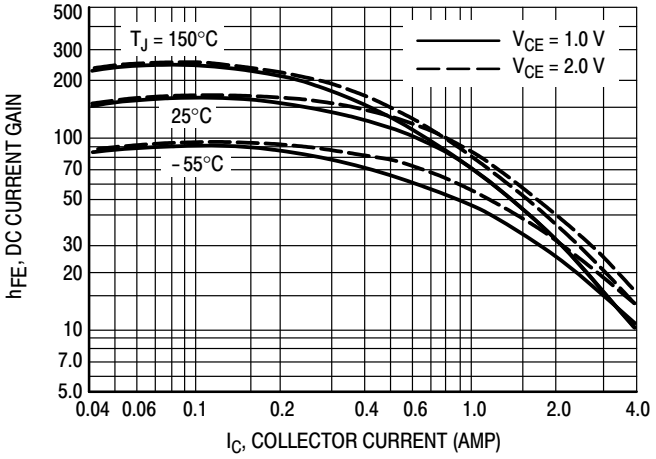


Figure 3. Thermal Response

NPN
MJD243



PNP
MJD253

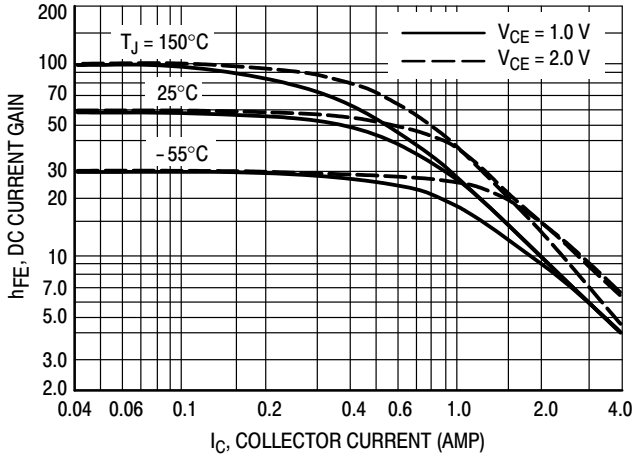
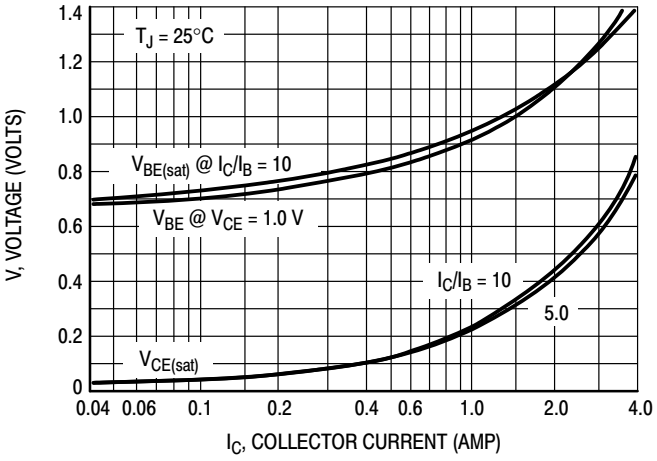


Figure 4. DC Current Gain



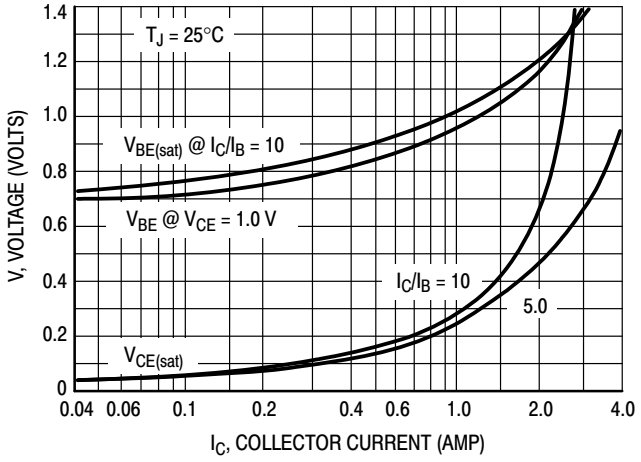
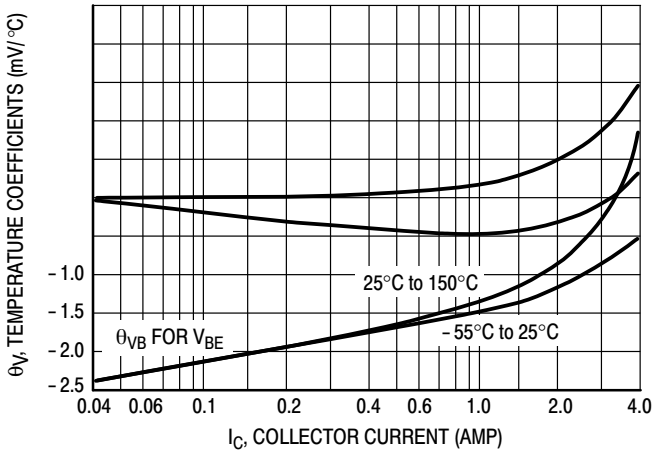


Figure 5. “On” Voltages



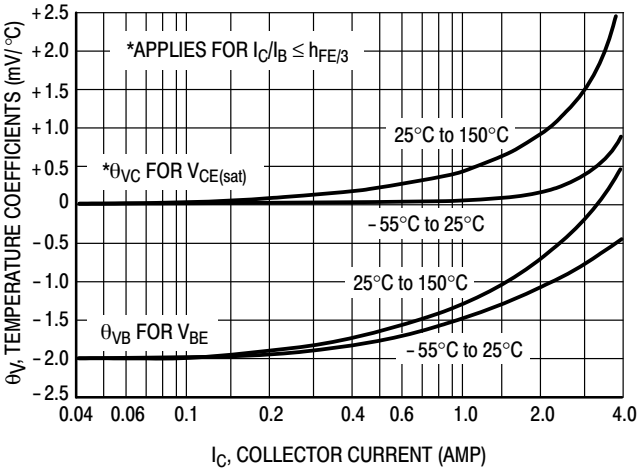
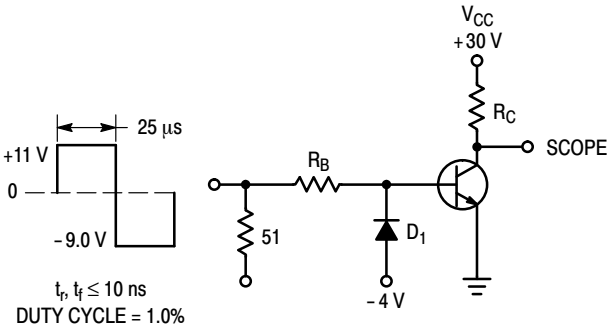


Figure 6. Temperature Coefficients



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 7. Switching Time Test Circuit

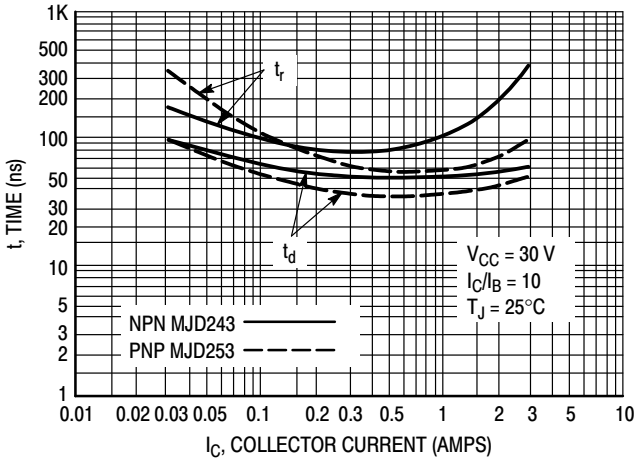


Figure 8. Turn−On Time

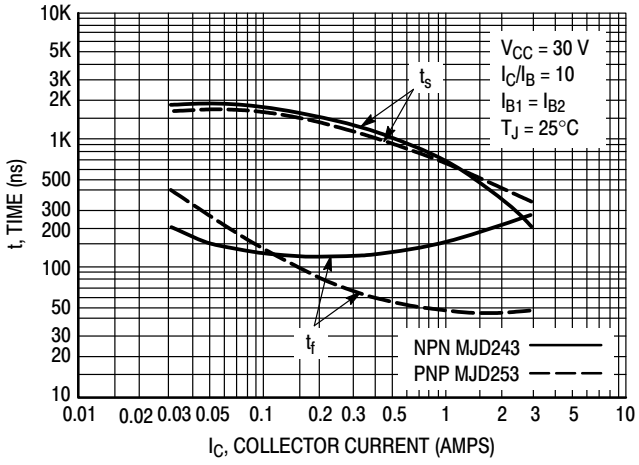


Figure 9. Turn−Off Time

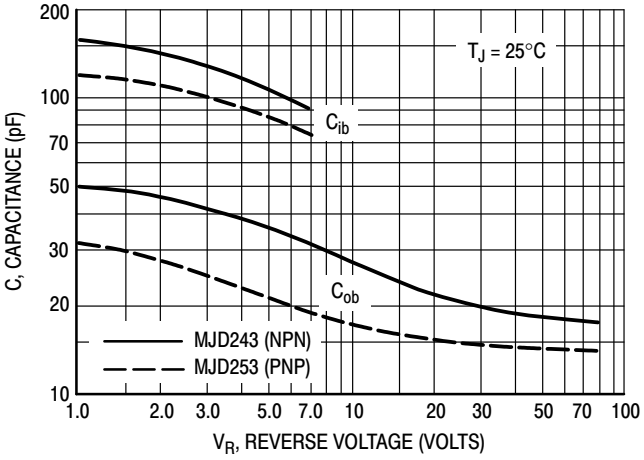


Figure 10. Capacitance

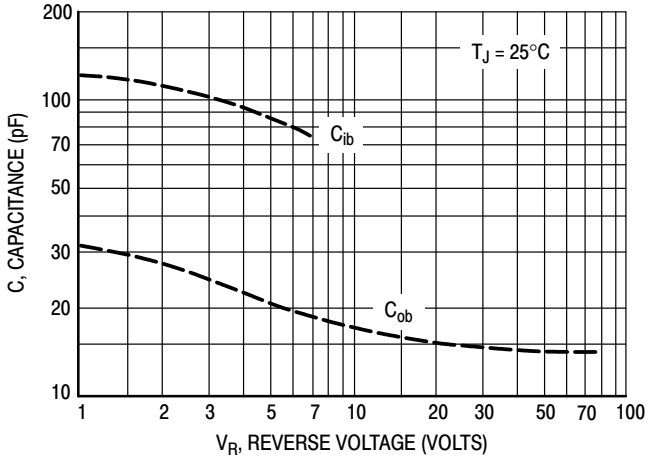


Figure 11. Capacitance

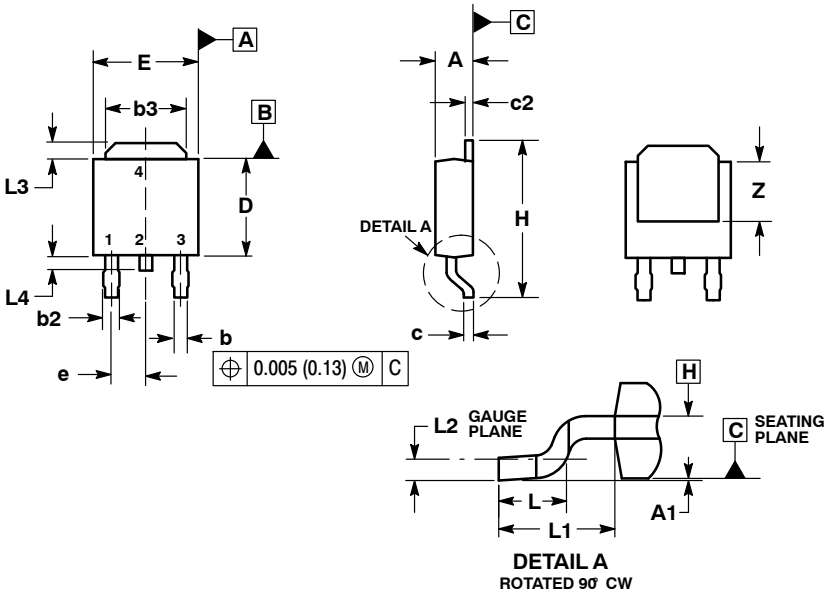
ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD243G	DPAK−3 (Pb−Free)	369C	75 Units / Rail
MJD243T4G	DPAK−3 (Pb−Free)	369C	2500 / Tape & Reel
MJD253−1G	DPAK−3 (Pb−Free)	369D	75 Units / Rail
MJD253T4G	DPAK−3 (Pb−Free)	369C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK−3
CASE 369C−01
ISSUE D

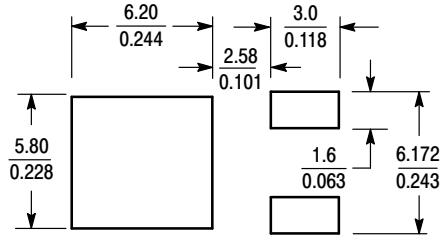


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	−−−	0.040	−−−	1.01
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*

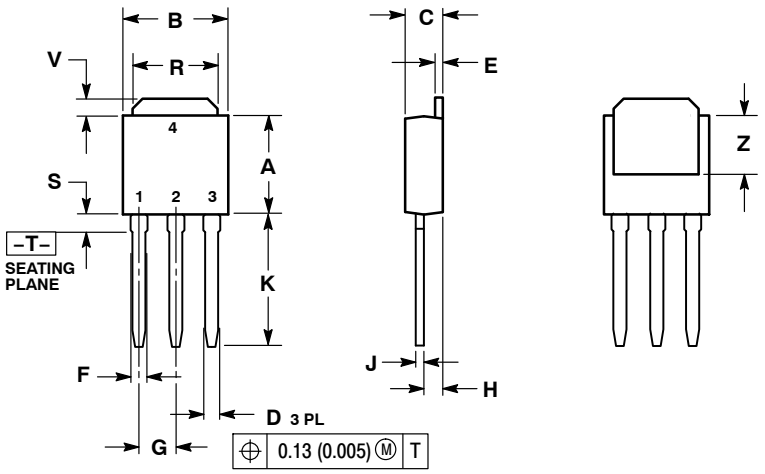


SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK−3 (SINGLE GAUGE)
CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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MJD243/D