Features

- **Operates Between 2.7V to 5.5V**
- **High Density, High-Performance Electrically Erasable Complex Programmable Logic Device**
  - **44-Pin, 32 I/O CPLD**
  - **12 ns Maximum Pin-to-Pin Delay**
  - **Registered Operation Up To 90.9 MHz**
  - **Fully Connected Input and Feedback Logic Array**
- **Flexible Logic Macrocell**
  - **D/T/Latch Configurable Flip Flops**
  - **Global and Individual Register Control Signals**
  - **Global and Individual Output Enable**
  - **Programmable Output Slew Rate**
- **Advanced Power Management Features**
  - **Automatic 3 mA Stand-By (ATF1500ABVL)**
  - **Pin-Controlled 5 µA Stand-By Mode (Typical)**
  - **Programmable Pin-Keeper Inputs and I/Os**
- **Available in Commercial and Industrial Temperature Ranges**
- **Available in 44-Pin PLCC and TQFP Packages**
- **Advanced Flash Technology**
  - **100% Tested**
  - **Completely Reprogrammable**
  - **100 Program/Erase Cycles**
  - **20 Year Data Retention**
  - **2000V ESD Protection**
  - **200 mA Latch-Up Immunity**
- **Supported By Popular 3rd Party Tools**
- **Security Fuse Feature**

Description

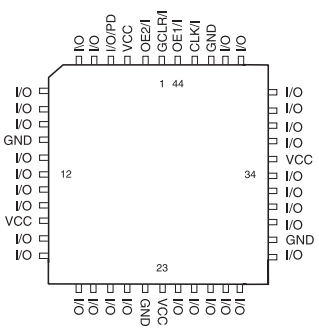
The ATF1500ABV is a high performance, high density Complex PLD. Built on an advanced Flash technology, it has maximum pin to pin delays of 12 ns and supports sequential logic operation at speeds up to 90.9 MHz. With 32 logic macrocells and up to 36 inputs, it easily integrates logic from several TTL, SSI, MSI and classic PLDs. The ATF1500ABV's global input and feedback architecture simplifies logic placement and eliminates pinout changes due to design changes.

(continued)

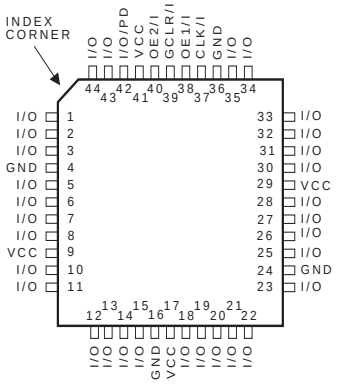
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
GCLR	Register Reset (active low)
OE1, OE2	Output Enable (active low)
V_{CC}	(+3V to 5.25V) Supply
PD	Power Down (active high)

PLCC
Top View



TQFP
Top View

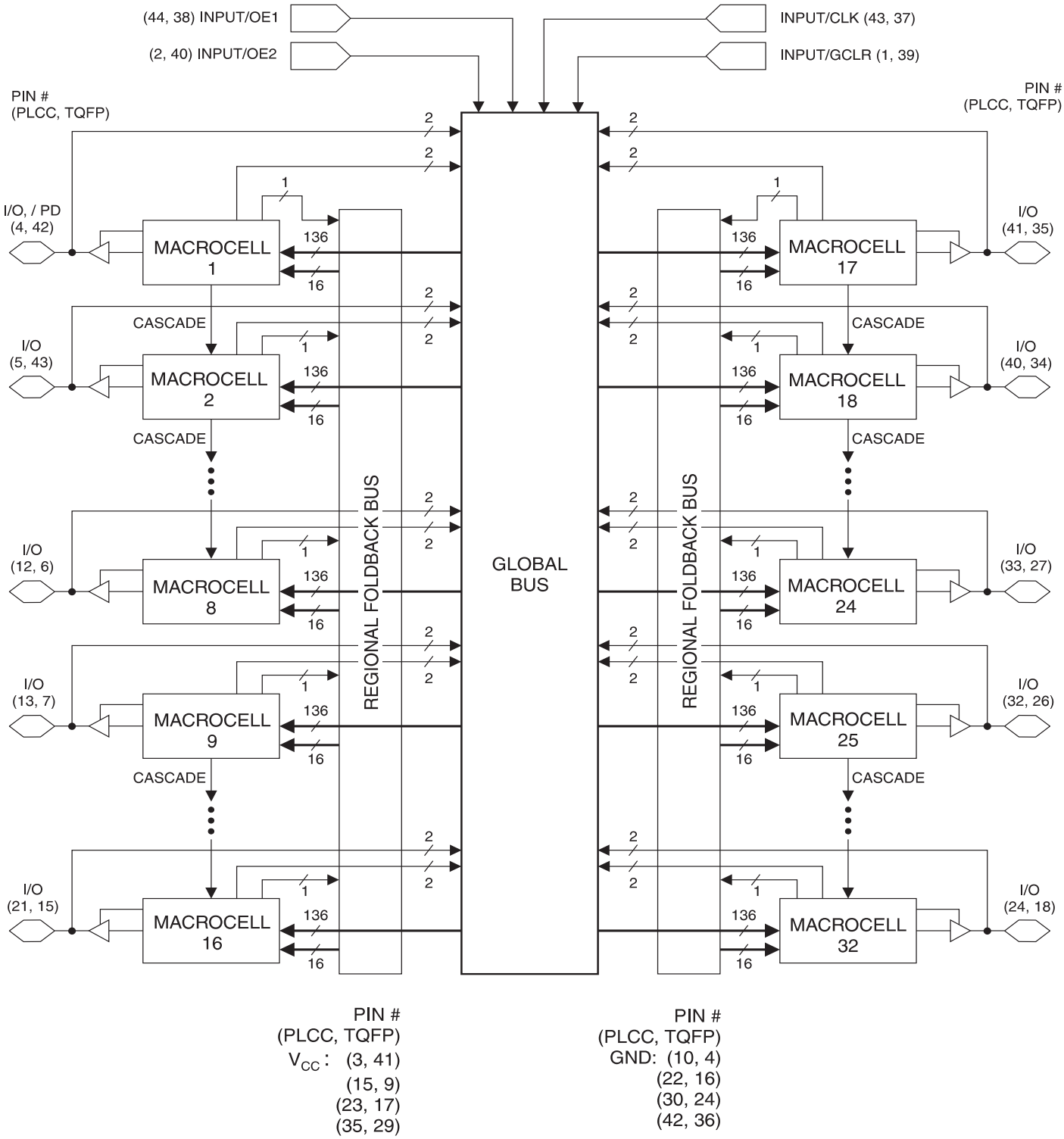


High-Performance EE PLD

ATF1500ABV
ATF1500ABVL

Rev. 0723D–6/98

Functional Logic Diagram(1)



Note: 1. Arrows connecting macrocells indicate direction and groupings of CASIN/CASOUT data flow.

The ATF1500ABV has 32 bi-directional I/O pins and 4 dedicated input pins. Each dedicated input pin can also serve as a global control signal: register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 32 logic macrocells generates a buried feedback, which goes to the global bus. Each input and I/O pin also feeds into the global bus. Because of this global bussing, each of these signals is always available to all 32 macrocells in the device.

Each macrocell also generates a foldback logic term, which goes to a regional bus. All signals within a regional bus are connected to all 16 macrocells within the region.

Cascade logic between macrocells in the ATF1500ABV allows fast, efficient generation of complex logic functions. The ATF1500ABV contains 4 such logic chains, each capable of creating sum term logic with a fan in of up to 40 product terms.

Bus Friendly Pin-Keeper Input and I/O'S

All Input and I/O pins on the ATF1500ABV have programmable "data keeper" circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

This circuitry prevents unused Input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Pin-keeper circuits can be disabled. Programming is controlled in the logic design file. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

Speed/Power Management

The ATF1500ABV has several built-in speed and power management features. The ATF1500ABV contains circuitry that automatically puts the device into a low power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides a proportional power savings for most applications running at system speeds below 10 MHz.

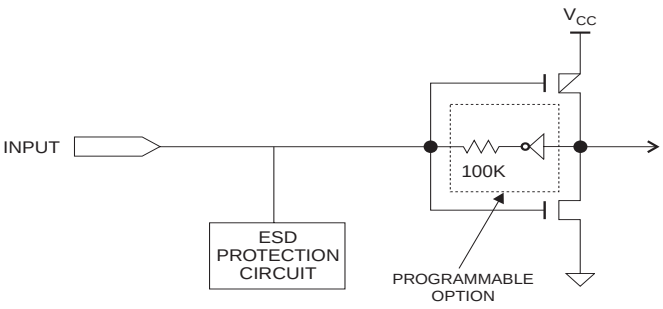
All ATF1500ABVs also have an optional pin-controlled power down mode. In this mode, current drops to below 10 µA. When the power down option is selected, the PD pin is used to power down the part. The power down option is selected in the design source file. When enabled, the device goes into power down when the PD pin is high. In the power down mode, all internal logic signals are latched and held, as are any enabled outputs. All pin transitions are ignored until the PD is brought low. When the power down feature is enabled, the PD cannot be used as a logic input or output. However, the PD pin's macrocell may still be used to generate buried foldback and cascade logic signals.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

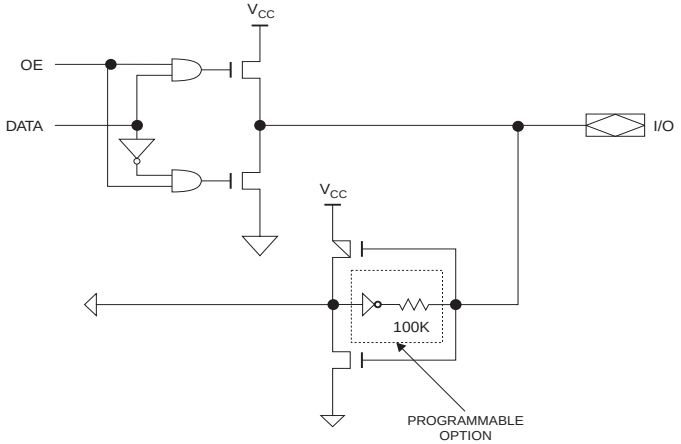
Design Software Support

ATF1500ABV designs are supported by several 3rd party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

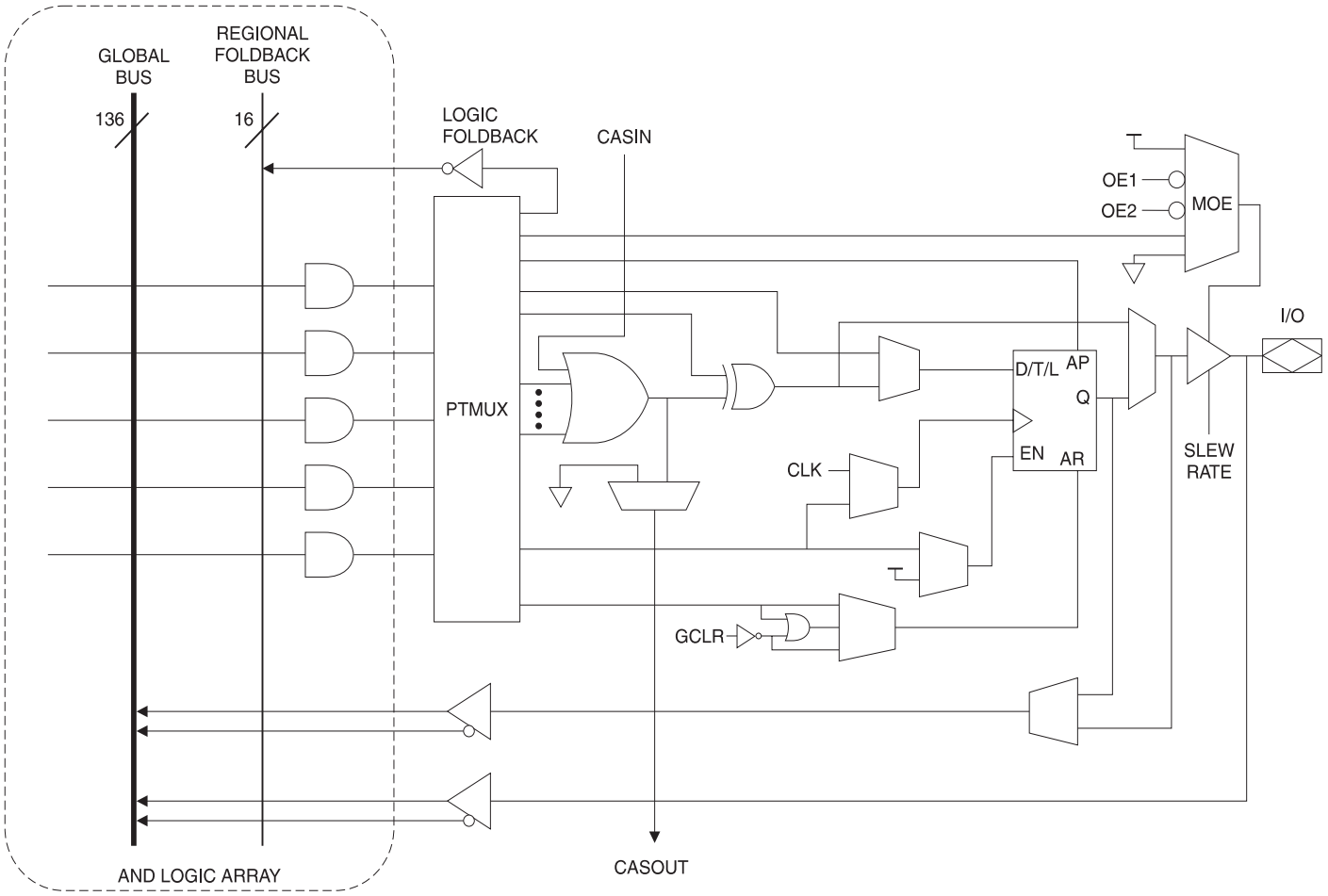
Input Diagram



I/O Diagram



ATF1500ABV Macrocell



ATF1500ABV Macrocell

The ATF1500ABV macrocell is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic; a flip flop; output select and enable; and logic array inputs.

Product Terms and Select Mux

Each ATF1500ABV macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1500ABV macrocell's OR/XOR/CASCADE logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a five input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a very small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high or low level. For combinatorial outputs, the fixed level input allows output polarity selection. For registered functions, the fixed levels allow De Morgan minimization of the product terms. The XOR gate is also used to emulate JK type flip flops.

Flip Flop

The ATF1500ABV's flip flop has very flexible data and control functions. The data input can come from either the XOR gate or from a separate product term. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell.

In addition to D, T, JK and SR operation, the flip flop can also be configured as a flow-through latch. In this mode,

data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the global CLK pin or an individual product term. The flip flop changes state on the clock's rising edge. When the CLK pin is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored.

The flip flop's asynchronous reset signal (AR) can be either the pin global clear (GCLR), a product term, or always off. AR can also be a logic OR of GCLR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Select and Enable

The ATF1500ABV macrocell output can be selected as registered or combinatorial. When the output is registered, the same registered signal is fed back internally to the global bus. When the output is combinatorial, the buried feedback can be either the same combinatorial signal or it can be the register output if the separate product term is chosen as the flip flop input.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic.

The output enable for each macrocell can also be selected as either of the two OE pins or as an individual product term.

Global/Regional Busses

The global bus contains all Input and I/O pin signals as well as the buried feedback signal from all 32 macrocells. Together with the complement of each signal, this provides a 68-bit bus as input to every product term. Having the entire global bus available to each macrocell eliminates any potential routing problems. With this architecture designs can be modified without requiring pinout changes.

Each macrocell also generates a foldback product term. This signal goes to the regional bus, and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allow generation of high fan-in sum terms (up to 21 product terms) with a small additional delay.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +5.25V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum out put pin voltage is V_{CC} + 0.75V dc, which may overshoot to 5.25V for pulses of less than 20 ns.

DC and AC Operating Conditions

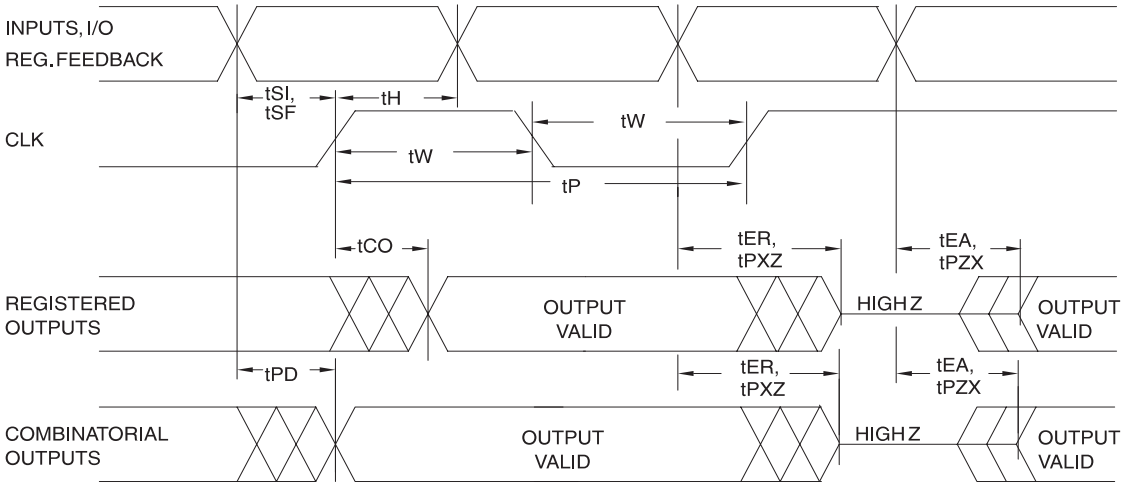
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	2.7V - 5.5V	2.7V - 5.5V

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(max)					-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH},min < $V_{IN} \le V_{CC}$					10	µA
I_{CC1}(1)	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = 0, V_{CC}	ATF1500ABV	Com.		35		mA
				Ind.		40		mA
			ATF1500ABVL	Com.			3	mA
				Ind.			5	mA
I_{CC2}	Power Supply Current, Power Down Mode	V_{CC} = MAX, V_{IN} = 0, V_{CC}				2		mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-130	mA
V_{IL}	Input Low Voltage	V_{CC}, min < V_{CC} < V_{CC}, max			-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = MIN	I_{OL} = 4 mA				0.45	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -0.1 mA		V_{CC} - .2			V

Note: 1. All I_{CC} parameters measured with outputs open, and a 16 bit loadable, up/down counter programmed into each region.

AC Waveforms



Register AC Characteristics, Input Pin Clock(1)

Symbol	Parameter	2.7-volt Adder	-12		-15		Units
			Min	Max	Min	Max	
t_{COS}(2)	Clock to Output	.5	2	7	2	8	ns
t_{CFS}	Clock to Feedback	0		3		3	ns
t_{SIS}	I, I/O Setup Time	1		10		11	ns
t_{SFS}	Feedback Setup Time	1		10		11	ns
t_{HS}	Input, I/O, Feedback Hold Time	0	0		0		ns
t_{PS}	Clock Period	1	13		14		ns
t_{WS}	Clock Width	.5	6.5		7		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$	-5		58.8		52.6	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$	-5.5		76.9		71.4	MHz
	No Feedback $1/(t_{PS})$	-5.5		76.9		71.4	MHz
t_{RPRS}	Reset Pin Recovery Time	1	3		4		ns
t_{RTRS}	Reset Term Recovery Time	1	10		12		ns

Notes: 1. AC Characteristics are for V_{CC} = 3.0 volts. For 2.7 volts, add the "2.7-volt adder."

2. For slow slew outputs, add t_{SSO} .

= Preliminary Information

Register AC Characteristics, Product Term Clock(1)

Symbol	Parameter	2.7-volt Adder	-12		-15		Units
			Min	Max	Min	Max	
t_{COA} (2)	Clock to Output	2		12		15	ns
t_{CFA}	Clock to Feedback	1		8		10	ns
t_{SIA}	I, I/O Setup Time	0	4		4		ns
t_{SFA}	Feedback Setup Time	0	4		4		ns
t_{HA}	Input, I/O, Feedback Hold Time	0	4		4		ns
t_{PA}	Clock Period	1	12		14		ns
t_{WA}	Clock Width	.5	6		7		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$	-7		62.5		52.6	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$	-6.4		83.3		71.4	MHz
	No Feedback $1/(t_{PA})$	-6.4		83.3		71.4	MHz
t_{RPRA}	Reset Pin Recovery Time	0	0		0		ns
t_{RTRA}	Reset/Preset Term Recovery Time	0	6		6		ns

Notes: 1. AC Characteristics are for V_{CC} = 3.0 volts. For 2.7 volts, add the “2.7-volt Adder.”

2. For slow slew outputs, add t_{SSO}.

AC Characteristic

Symbol	Parameter	2.7-volt Adder	-12		-15		Units
			Min	Max	Min	Max	
t_{PD} (2)	I, I/O or FB to Non-Registered Output	2	3	12	3	15	ns
t_{PD2}	I, I/O to Feedback	1		8		9	ns
t_{PD3} (2)	Feedback to Non-Registered Output	2	3	12	3	15	ns
t_{PD4}	Feedback to Feedback	1		8		9	ns
t_{EA} (2)	OE Term to Output Enable	1	3	12	3	15	ns
t_{ER}	OE Term to Output Disable	1	2	12	2	15	ns
t_{PZX} (2)	OE Pin to Output Enable	1	2	8	2	9	ns
t_{PXZ}	OE Pin to Output Disable	1	1.5	8	1.5	9	ns
t_{PF}	Preset To Feedback	1		9		12	ns
t_{PO} (2)	Preset to Registered Output	2		14		20	ns
t_{RPF}	Reset Pin to Feedback	1		3		5	ns
t_{RPO} (2)	Reset Pin to Registered Output	1		8		11	ns
t_{RTF}	Reset Term to Feedback	1		9		12	ns
t_{RTO} (2)	Reset Term to Registered Output	2		14		20	ns
t_{CAS}	Cascade Logic Delay	0		1		1	ns
t_{SSO}	Slow Slew Output Adder	0		3		4	ns
t_{FLD}	Foldback Term Delay	1		7		8	ns

Notes: 1. AC Characteristics are for V_{CC} = 3.0 volts. For 2.7 volts, add the “2.7-volt Adder.”

2. For slow slew outputs, add t_{SSO}.

= Preliminary Information

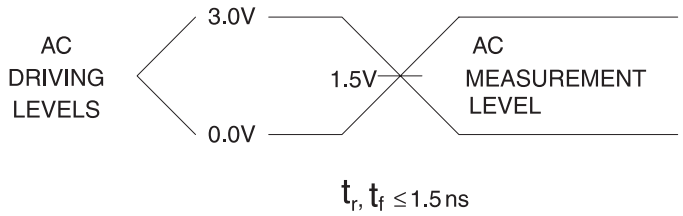
Power Down AC Characteristics(1)

Symbol	Parameter	2.7-volt Adder	-12		-15		Units
			Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O Before PD High	1	12		15		ns
t_{GVDH}	Valid OE(3) Before PD High	1	12		15		ns
t_{CVDH}	Valid Clock(3) Before PD High	1	12		15		ns
t_{DHIX}	Input Don't Care After PD High	1	22		25		ns
t_{DHGX}	$\overline{OE}$ Don't Care After PD High	1	22		25		ns
tDHCX	Clock Don't Care After PD High	1	22		25		ns
t_{DLIV}	PD Low to Valid I, I/O	0		1		1	µs
t_{DLGV}	PD Low to Valid OE(3)	0		1		1	µs
t_{DLCV}	PD Low to Valid Clock(3)	0		1		1	µs
t_{DLOV}(1)	PD Low to Valid Output	0		1		1	µs

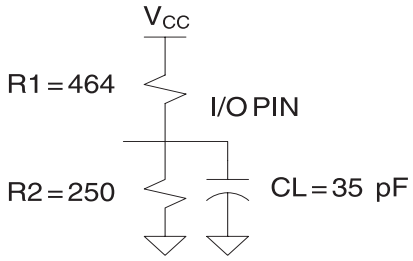
Notes: 1. AC Characteristics are for V_{CC} = 3.0 volts. For 2.7 volts, add the “2.7-volt Adder.”
2. For slow slew outputs, add t_{SSO}.
3. Pin or Product Term.

= Preliminary Information

Input Test Waveforms and Measurement Levels



Output Test Load



Pin Capacitance

(f = 1 MHz, T = 25°C)(1)

	Typ	Max	Units	Conditions
C_{IN}	4.5	5.5	pF	V_{IN} = 0V
C_{OUT}	3.5	4.5	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The ATF1500ABV's registers are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be low on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

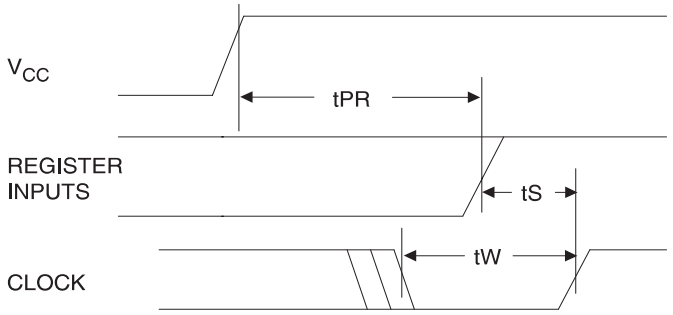
1. The V_{CC} rise must be monotonic, from below .7 volts.
2. Signals from which clocks are derived must remain stable during T_{PR}.
3. After T_{PR} occurs, all input and feedback setup times must be met before driving the clock signal high.

Power Down Mode

The ATF1500ABV includes an optional pin controlled power down feature. When this mode is enabled, the PD pin acts as the power down pin. When the PD pin is high, the device supply current is reduced to less than 10 µA. During power down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in a HI-Z state at the onset of power down will remain at HI-Z. During power down, all input signals except the power down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power down pin feature is enabled in the logic design file. Designs using the power down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Register Preload

The ATF1500ABV's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with preload vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically when vectors are run by any approved programmers. The preload mode is enabled by raising an input pin to a high voltage level. Contact Atmel PLD Applications for PRELOAD pin assignments, timing and voltage requirements.



Parameter	Description	Typ	Max	Units
T_{PR}	Power-Up Reset Time	2	10	µs
V_{RST}	Power-Up Reset Voltage	2.2	2.7	V

Output Slew Rate Control

Each ATF1500ABV macrocell contains a configuration bit for each I/O to control its output slew rate. This allows selected data paths to operate at maximum throughput while reducing system noise from outputs that are not speed-critical. Outputs default to slow edges, and may be individually set to fast in the design file. Output transition times for outputs configured as "slow" have a t_{SSO} delay adder.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1500ABV fuse patterns. Once programmed, fuse verify and preload are prohibited. However, the 160-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

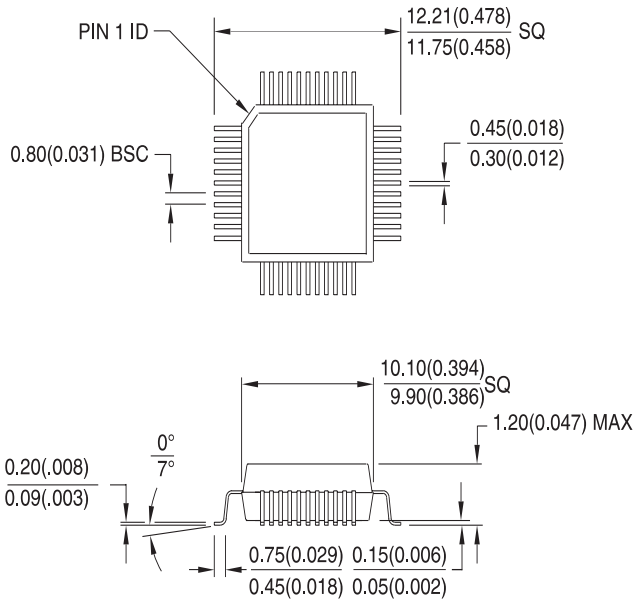
Ordering Information

t_{PD} (ns)	t_{COS} (ns)	F_{MAXS} (MHz)	Ordering Code	Package	Operation Range
12	6	62.5	ATF1500ABV-12AC ATF1500ABV-12JC	44A 44J	Commercial (0°C to 70°C)
15	8	52.6	ATF1500ABV-15AC ATF1500ABV-15JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500ABV-15AI ATF1500ABV-15JI	44A 44J	Industrial (-40°C to 85°C)
25	TBD	TBD	ATF1500ABVL-25AC ATF1500ABVL-25JC	44A 44J	Commercial (0°C to 70°C)

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)

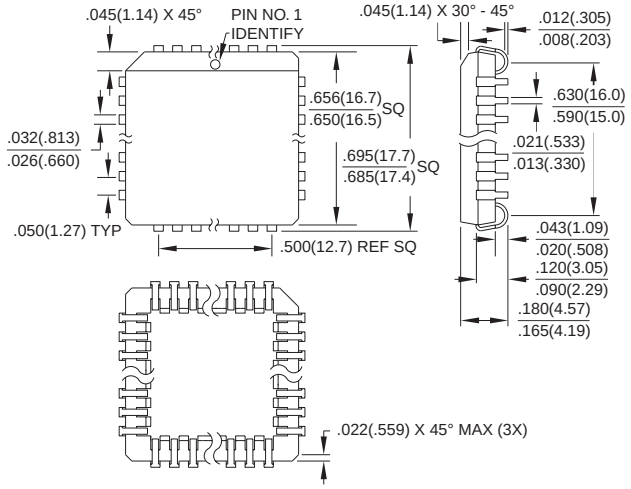
Packaging Information

44A, 44-Lead, Thin (1.0 mm)
Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

44J, 44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



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