EVALUATION KIT AVAILABLE

MAX11102/03/05/06/10/11/15/16/17

2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

General Description

The MAX11102/MAX11103/MAX11105/MAX11106/MAX11110/MAX11111/MAX11115/MAX11116/MAX11117 are 12-/10-/8-bit, compact, high-speed, low-power, successive approximation analog-to-digital converters (ADCs). These high-performance ADCs include a high-dynamic range sample-and-hold and a high-speed serial interface. These ADCs accept a full-scale input from 0V to the power supply or to the reference voltage.

The MAX11102/MAX11103/MAX11106/MAX11111 feature dual, single-ended analog inputs connected to the ADC core using a 2:1 MUX. The devices also include a separate supply input for data interface and a dedicated input for reference voltage. In contrast, the single-channel devices generate the reference voltage internally from the power supply.

These ADCs operate from a 2.2V to 3.6V supply and consume only 5.2mW at 3Msps and 3.7mW at 2Msps. The devices include full power-down mode and fast wake-up for optimal power management and a high-speed 3-wire serial interface. The 3-wire serial interface directly connects to SPI, QSPI™, and MICROWIRE® devices without external logic.

Excellent dynamic performance, low voltage, low power, ease of use, and small package size make these converters ideal for portable battery-powered data-acquisition applications, and for other applications that demand low-power consumption and minimal space.

These ADCs are available in a 10-pin TDFN package, 10-pin µMAX® package, and a 6-pin SOT23 package. These devices operate over the -40°C to +125°C temperature range.

Features

- **2Msps/3Msps Conversion Rate, No Pipeline Delay**
- **12-/10-/8-Bit Resolution**
- **1-/2-Channel, Single-Ended Analog Inputs**
- **Low-Noise 73dB SNR**
- **Variable I/O: 1.5V to 3.6V (Dual-Channel Only)**
  Allows the Serial Interface to Connect Directly to 1.5V, 1.8V, 2.5V, or 3V Digital Systems
- **2.2V to 3.6V Supply Voltage**
- **Low Power**
  3.7mW at 2Msps
  5.2mW at 3Msps
  Very Low Power Consumption at 2.5µA/ksps
- **External Reference Input (Dual-Channel Devices Only)**
- **1.3µA Power-Down Current**
- **SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- **10-Pin, 3mm x 3mm TDFN Package**
- **10-Pin, 3mm x 5mm µMAX Package**
- **6-Pin, 2.8mm x 2.9mm SOT23 Package**
- **Wide -40°C to +125°C Operation**

Applications

Data Acquisition
Portable Data Logging
Medical Instrumentation
Battery-Operated Systems
Communication Systems
Automotive Systems

Ordering Information

PART	PIN-PACKAGE	BITS	SPEED (Msps)	NO. OF CHANNELS	TOP MARK
MAX11102AUB+	10 µMAX-EP*	12	2	2	+ABBA
MAX11102ATB+	10 TDFN-EP*	12	2	2	+AWI
MAX11103AUB+	10 µMAX-EP*	12	3	2	+AAAU
MAX11103ATB+	10 TDFN-EP*	12	3	2	+AWV

Ordering Information continued at end of data sheet.

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

QSPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.
µMAX is a registered trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5245; Rev 7; 9/12

ABSOLUTE MAXIMUM RATINGS

VDD to GND .....-0.3V to +4V
REF, OVDD, AIN1, AIN2, AIN to GND .....-0.3V to the lower of (V_{DD} + 0.3V) and +4V
$\overline{CS}$, SCLK, CHSEL, DOUT TO GND.....-0.3V to the lower of (V_{OVDD} + 0.3V) and +4V
AGND to GND .....-0.3V to +0.3V
Input/Output Current (all pins) 50mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C) 696mW
10-Pin TDFN (derate 24.4mW/°C above +70°C).....1951mW
10-Pin µMAX (derate 8.8mW/°C above +70°C).....707.3mW
Operating Temperature Range ..... .-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX11102/MAX11103)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}. MAX11102: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11103: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error	OE			±0.3	±3	LSB
Gain Error	GE	Excluding offset and reference errors		±1	±3	LSB
Total Unadjusted Error	TUE			±1.5		LSB
Channel-to-Channel Offset Matching				±0.4		LSB
Channel-to-Channel Gain Matching				±0.05		LSB
DYNAMIC PERFORMANCE (MAX11103: $f_{AIN_}$ = 1MHz, MAX11102: $f_{AIN_}$ = 0.5MHz)						
Signal-to-Noise and Distortion	SINAD	MAX11103	70	72		dB
		MAX11102	70	72.5		
Signal-to-Noise Ratio	SNR	MAX11103	70.5	72		dB
		MAX11102	70.5	73		
Total Harmonic Distortion	THD	MAX11103		-85	-75	dB
		MAX11102		-85	-76	
Spurious-Free Dynamic Range	SFDR	MAX11103	76	85		dB
		MAX11102	77	85		
Intermodulation Distortion	IMD	MAX11103: f_1 = 1.0003MHz, f_2 = 0.99955MHz MAX11102: f_1 = 500.15kHz, f_2 = 499.56kHz		-84		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 68dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
Crosstalk				-90		dB

ELECTRICAL CHARACTERISTICS (MAX11102/MAX11103) (continued)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}. MAX11102: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11103: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Throughput		MAX11103	0.03		3	Msps
		MAX11102	0.02		2	
Conversion Time		MAX11103	260			ns
		MAX11102	391			
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f_{CLK}	MAX11103	0.48		48	MHz
		MAX11102	0.32		32	
ANALOG INPUT (AIN1, AIN2)						
Input Voltage Range	$V_{AIN_}$		0		V_{REF}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	$C_{AIN_}$	Track		20		pF
		Hold		4		
EXTERNAL REFERENCE INPUT (REF)						
Reference Input-Voltage Range	V_{REF}		1		V_{DD} + 0.05	V
Reference Input Leakage Current	I_{ILR}	Conversion stopped		0.005	±1	µA
Reference Input Capacitance	C_{REF}			5		pF
DIGITAL INPUTS (SCLK, $\overline{CS}$, CHSEL)						
Digital Input High Voltage	V_{IH}		0.75 x V_{OVDD}			V
Digital Input Low Voltage	V_{IL}				0.25 x V_{OVDD}	V
Digital Input Hysteresis	V_{HYST}			0.15 x V_{OVDD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.85 x V_{OVDD}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA			0.15 x V_{OVDD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF

ELECTRICAL CHARACTERISTICS (MAX11102/MAX11103) (continued)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}. MAX11102: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11103: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.6	V
Digital I/O Supply Voltage	V_{OVDD}		1.5		V_{DD}	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	MAX11103, $V_{AIN_}$ = V_{GND}			3.3	mA
		MAX11102, $V_{AIN_}$ = V_{GND}			2.6	
	I_{OVDD}	MAX11103, $V_{AIN_}$ = V_{GND}			0.33	
		MAX11102, $V_{AIN_}$ = V_{GND}			0.22	
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}	MAX11103		1.98		mA
		MAX11102		1.48		
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.6V, V_{REF} = 2.2V		0.7		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t_4	Figure 2, V_{OVDD} = 2.2V - 3.6V			15	ns
		Figure 2, V_{OVDD} = 1.5V - 2.2V			16.5	
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

ELECTRICAL CHARACTERISTICS (MAX11105)

(V_{DD} = 2.2V to 3.6V, f_{SCLK} = 32MHz, 50% duty cycle, 2Msps, C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error	OE			±0.3	±3	LSB
Gain Error	GE	Excluding offset and reference errors		±1	±3	LSB
Total Unadjusted Error	TUE			±1.5		LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise and Distortion	SINAD	f_{AIN} = 500kHz	70	72.5		dB
Signal-to-Noise Ratio	SNR	f_{AIN} = 500kHz	70.5	73		dB

ELECTRICAL CHARACTERISTICS (MAX11105) (continued)

(V_{DD} = 2.2V to 3.6V, f_{SCLK} = 32MHz, 50% duty cycle, 2Msps, C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	f_{AIN} = 500kHz		-85	-76	dB
Spurious-Free Dynamic Range	SFDR	f_{AIN} = 500kHz	77	85		dB
Intermodulation Distortion	IMD	f_1 = 500.15 kHz, f_2 = 499.56 kHz		-84		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 68dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
CONVERSION RATE						
Throughput			0.02		2	Msps
Conversion Time			391			ns
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial Clock Frequency	f_{CLK}		0.32		32	MHz
ANALOG INPUT						
Input Voltage Range	V_{AIN}		0		V_{DD}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	C_{AIN}	Track		20		pF
		Hold		4		
DIGITAL INPUTS (SCLK, $\overline{CS}$, CHSEL)						
Digital Input High Voltage	V_{IH}		0.75 x V_{VDD}			V
Digital Input Low Voltage	V_{IL}				0.25 x V_{VDD}	V
Digital Input Hysteresis	V_{HYST}			0.15 x V_{VDD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.85 x V_{VDD}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA			0.15 x V_{VDD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.6	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	V_{AIN} = V_{GND}			2.6	mA

ELECTRICAL CHARACTERISTICS (MAX11105) (continued)

(V_{DD} = 2.2V to 3.6V, f_{SCLK} = 32MHz, 50% duty cycle, 2Msps, C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}			1.48		mA
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.6V		0.7		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t_4	Figure 2, V_{DD} = +2.2V to +3.6V			15	ns
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

ELECTRICAL CHARACTERISTICS (MAX11106)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}, f_{SCLK} = 48MHz, 50% duty cycle, 3Msps; C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL				±0.4	LSB
Differential Nonlinearity	DNL	No missing codes			±0.4	LSB
Offset Error	OE			±0.5	±1	LSB
Gain Error	GE	Excluding offset and reference errors		0	±1	LSB
Total Unadjusted Error	TUE			±0.5		LSB
Channel-to-Channel Offset Matching				±0.05		LSB
Channel-to-Channel Gain Matching				±0.05		LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise and Distortion	SINAD	$f_{AIN_}$ = 1MHz	61	61.8		dB
Signal-to-Noise Ratio	SNR	$f_{AIN_}$ = 1MHz	61	61.8		dB
Total Harmonic Distortion	THD	$f_{AIN_}$ = 1MHz		-83	-74	dB
Spurious-Free Dynamic Range	SFDR	$f_{AIN_}$ = 1MHz	75			dB

ELECTRICAL CHARACTERISTICS (MAX11106) (continued)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}, f_{SCLK} = 48MHz, 50% duty cycle, 3Msps; C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Intermodulation Distortion	IMD	f_1 = 1.0003MHz, f_2 = 0.99955MHz		-82		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 60dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
Crosstalk				-90		dB
CONVERSION RATE						
Throughput			0.03		3	Msps
Conversion Time			260			ns
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f_{CLK}		0.48		48	MHz
ANALOG INPUT (AIN1, AIN2)						
Input Voltage Range	$V_{AIN_}$		0		V_{REF}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	$C_{AIN_}$	Track		20		pF
		Hold		4		
EXTERNAL REFERENCE INPUT (REF)						
Reference Input-Voltage Range	V_{REF}		1		V_{DD} + 0.05	V
Reference Input Leakage Current	I_{ILR}	Conversion stopped		0.005	±1	µA
Reference Input Capacitance	C_{REF}			5		pF
DIGITAL INPUTS (SCLK, $\overline{CS}$, CHSEL)						
Digital Input-High Voltage	V_{IH}		0.75 x V_{OVDD}			V
Digital Input-Low Voltage	V_{IL}				0.25 x V_{OVDD}	V
Digital Input Hysteresis	V_{HYST}			0.15 x V_{OVDD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output-High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.85 x V_{OVDD}			V
Output-Low Voltage	V_{OL}	I_{SINK} = 200µA			0.15 x V_{OVDD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF

ELECTRICAL CHARACTERISTICS (MAX11106) (continued)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}, f_{SCLK} = 48MHz, 50% duty cycle, 3Msps; C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.6	V
Digital I/O Supply Voltage	V_{OVDD}		1.5		V_{DD}	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	$V_{AIN_}$ = V_{GND}			3.3	mA
	I_{OVDD}	$V_{AIN_}$ = V_{GND}			0.33	
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}			1.98		mA
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.6V, V_{REF} = 2.2V		0.17		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge (Figure 2)	t_4	V_{OVDD} = 2.2V - 3.6V			15	ns
		V_{OVDD} = 1.5V - 2.2V			16.5	
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

ELECTRICAL CHARACTERISTICS (MAX11110/MAX11117)

(V_{DD} = 2.2V to 3.6V. MAX11110: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11117: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error	OE	MAX11117		±0.5	±1.65	LSB
		MAX11110		±0.3	±1.2	
Gain Error	GE	Excluding offset and reference errors, MAX11117		±0.7	±1.4	LSB
		Excluding offset and reference errors, MAX11110		±0.15	±1	
Total Unadjusted Error	TUE			±1		LSB

ELECTRICAL CHARACTERISTICS (MAX11110/MAX11117) (continued)

(V_{DD} = 2.2V to 3.6V. MAX11110: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11117: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX11117: f_{AIN} = 1MHz, MAX11110: f_{AIN} = 0.5MHz)						
Signal-to-Noise and Distortion	SINAD	MAX11117	59	61.5		dB
		MAX11110	60.5	61.5		
Signal-to-Noise Ratio	SNR	MAX11117	59	61.5		dB
		MAX11110	60.5	61.5		
Total Harmonic Distortion	THD	MAX11117		-85	-74	dB
		MAX11110		-85	-73	
Spurious-Free Dynamic Range	SFDR	MAX11117	75			dB
		MAX11110	75			
Intermodulation Distortion	IMD	MAXX11117: f_1 = 1.0003MHz, f_2 = 0.99955MHz MAX11110: f_1 = 500.15kHz, f_2 = 499.56kHz		-82		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 60dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
CONVERSION RATE						
Throughput		MAX11117	0.03		3	Msps
		MAX11110	0.02		2	
Conversion Time		MAX11117	260			ns
		MAX11110	391			
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial Clock Frequency	f_{CLK}	MAX11117	0.48		48	MHz
		MAX11110	0.32		32	
ANALOG INPUT (AIN)						
Input Voltage Range	V_{AIN}		0		V_{DD}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	C_{AIN}	Track		20		pF
		Hold		4		
DIGITAL INPUTS (SCLK, $\overline{CS}$, CHSEL)						
Digital Input-High Voltage	V_{IH}		0.75 x V_{DD}			V
Digital Input-Low Voltage	V_{IL}				0.25 x V_{DD}	V
Digital Input Hysteresis	V_{HYST}			0.15 x V_{DD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF

ELECTRICAL CHARACTERISTICS (MAX11110/MAX11117) (continued)

(V_{DD} = 2.2V to 3.6V. MAX11110: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11117: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (DOUT)						
Output-High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.85 x V_{DD}			V
Output-Low Voltage	V_{OL}	I_{SINK} = 200µA			0.15 x V_{DD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.6	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	MAX11117, V_{AIN} = V_{GND}			3.55	mA
		MAX11110, V_{AIN} = V_{GND}			2.6	
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}	MAX11117		1.98		mA
		MAX11110		1.48		
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.6V		0.17		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t_4	Figure 2, V_{DD} = +2.2V to +3.6V			15	ns
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

ELECTRICAL CHARACTERISTICS (MAX11111)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}, f_{SCLK} = 48MHz, 50% duty cycle, 3Msps, C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity	INL				±0.15	LSB
Differential Nonlinearity	DNL	No missing codes			±0.15	LSB
Offset Error	OE			0.45	±0.7	LSB
Gain Error	GE	Excluding offset and reference errors		0	±0.2	LSB
Total Unadjusted Error	TUE			0.5		LSB
Channel-to-Channel Offset Matching				0.01		LSB
Channel-to-Channel Gain Matching				0.01		LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise and Distortion	SINAD	$f_{AIN_}$ = 1MHz	49	49.8		dB
Signal-to-Noise Ratio	SNR	$f_{AIN_}$ = 1MHz	49	49.8		dB
Total Harmonic Distortion	THD	$f_{AIN_}$ = 1MHz		-75	-67	dB
Spurious-Free Dynamic Range	SFDR	$f_{AIN_}$ = 1MHz	63	67		dB
Intermodulation Distortion	IMD	f_1 = 1.0003MHz, f_2 = 0.99955MHz		-65		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 49dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
Crosstalk				-90		dB
CONVERSION RATE						
Throughput			0.03		3	Msps
Conversion Time			260			ns
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f_{CLK}		0.48		48	MHz
ANALOG INPUT (AIN1, AIN2)						
Input Voltage Range	$V_{AIN_}$		0		V_{REF}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	$C_{AIN_}$	Track		20		pF
		Hold		4		
EXTERNAL REFERENCE INPUT (REF)						
Reference Input Voltage Range	V_{REF}		1		V_{DD} + 0.05	V
Reference Input Leakage Current	I_{ILR}	Conversion stopped		0.005	±1	µA
Reference Input Capacitance	C_{REF}			5		pF

ELECTRICAL CHARACTERISTICS (MAX11111) (continued)

(V_{DD} = 2.2V to 3.6V, V_{REF} = V_{DD}, V_{OVDD} = V_{DD}, f_{SCLK} = 48MHz, 50% duty cycle, 3Msps, C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, $\overline{CS}$)						
Digital Input High Voltage	V_{IH}		0.75 x V_{OVDD}			V
Digital Input Low Voltage	V_{IL}				0.25 x V_{OVDD}	V
Digital Input Hysteresis	V_{HYST}			0.15 x V_{OVDD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA (Note 2)	0.85 x V_{OVDD}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA (Note 2)			0.15 x V_{OVDD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.6	V
Digital I/O Supply Voltage	V_{OVDD}		1.5		V_{DD}	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	$V_{AIN_}$ = V_{GND}			3.3	mA
	I_{OVDD}	$V_{AIN_}$ = V_{GND}			0.33	
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}			1.98		mA
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.6V, V_{REF} = 2.2V		0.17		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge (Figure 2)	t_4	V_{OVDD} = 2.2V - 3.6V			15	ns
		V_{OVDD} = 1.5V - 2.2V			16.5	
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

ELECTRICAL CHARACTERISTICS (MAX11115/MAX11116)

(V_{DD} = 2.2V to 3.6V. MAX11115: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11116: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity	INL				±0.25	LSB
Differential Nonlinearity	DNL	No missing codes			±0.25	LSB
Offset Error	OE			±0.45	±0.75	LSB
Gain Error	GE	Excluding offset and reference errors		±0.04	±0.5	LSB
Total Unadjusted Error	TUE			±0.75		LSB
DYNAMIC PERFORMANCE (MAX11116: f_{AIN} = 1MHz MAX11115: f_{AIN} = 500kHz)						
Signal-to-Noise and Distortion	SINAD	MAX11116	49	49.5		dB
		MAX11115	49	49.5		
Signal-to-Noise Ratio	SNR	MAX11116	49	49.5		dB
		MAX11115	49	49.5		
Total Harmonic Distortion	THD	MAX11116		-70	-66	dB
		MAX11115		-75	-67	
Spurious-Free Dynamic Range	SFDR	MAX11116	63	66		dB
		MAX11115	63	66		
Intermodulation Distortion	IMD	MAX11116: f_1 = 1.0003MHz, f_2 = 0.99955MHz MAX11115: f_1 = 500.15kHz, f_2 = 499.56kHz		-65		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 49dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
CONVERSION RATE						
Throughput		MAX11116	0.03		3	Msps
		MAX11115	0.02		2	
Conversion Time		MAX11116	260			ns
		MAX11115	391			
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f_{CLK}	MAX11116	0.48		48	MHz
		MAX11115	0.32		32	
ANALOG INPUT (AIN)						
Input Voltage Range	V_{AIN}		0		V_{DD}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	C_{AIN}	Track		20		pF
		Hold		4		
DIGITAL INPUTS (SCLK, $\overline{CS}$)						
Digital Input High Voltage	V_{IH}		0.75 x V_{DD}			V

ELECTRICAL CHARACTERISTICS (MAX11115/MAX11116) (continued)

(V_{DD} = 2.2V to 3.6V. MAX11115: f_{SCLK} = 32MHz, 50% duty cycle, 2Msps. MAX11116: f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Low Voltage	V_{IL}				0.25 x V_{DD}	V
Digital Input Hysteresis	V_{HYST}			0.15 V_{DD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.85 x V_{DD}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA			0.15 x V_{DD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.6	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	MAX11116, V_{AIN} = V_{GND}			3.55	mA
		MAX11115, V_{AIN} = V_{GND}			2.6	
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}	MAX11116		1.98		mA
		MAX11115		1.48		
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.6V		0.17		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t_4	Figure 2, V_{DD} = +2.2V to +3.6V			15	ns
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

Note 1: All timing specifications given are with a 10pF capacitor.
Note 2: Guaranteed by design in characterization; not production tested.

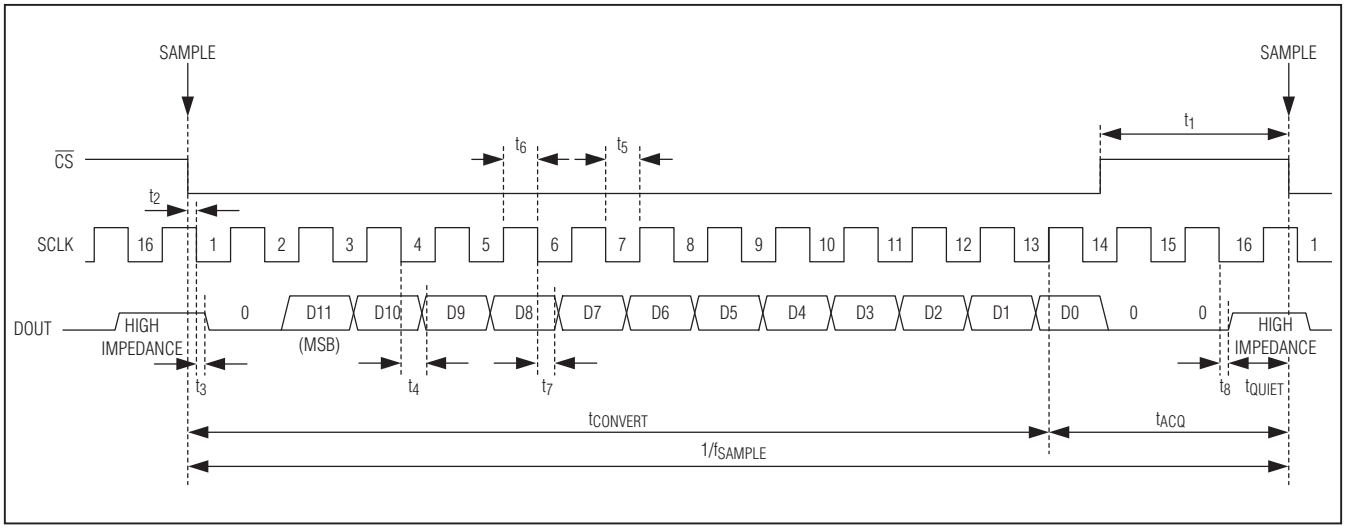


Figure 1. Interface Signals for Maximum Throughput, 12-Bit Devices

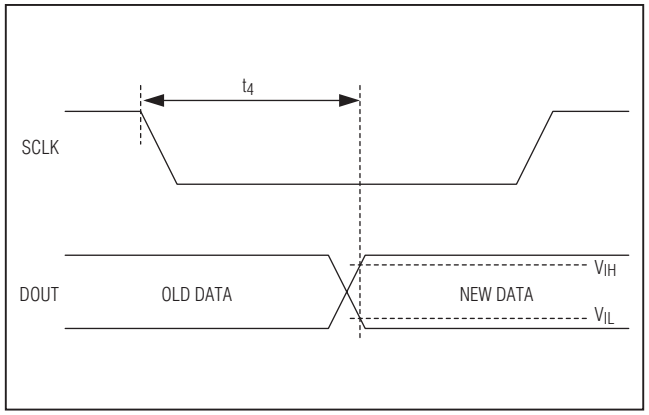


Figure 2. Setup Time After SCLK Falling Edge

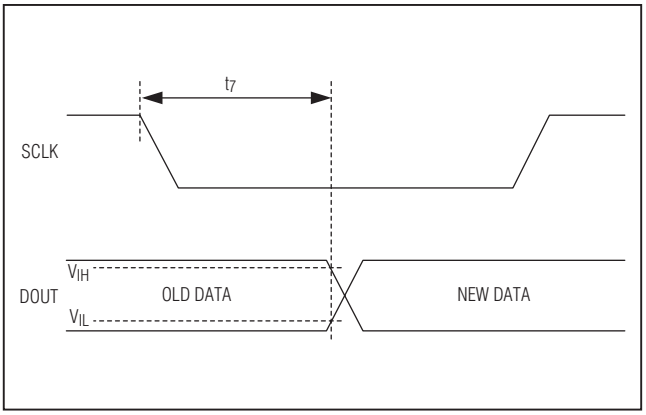


Figure 3. Hold Time After SCLK Falling Edge

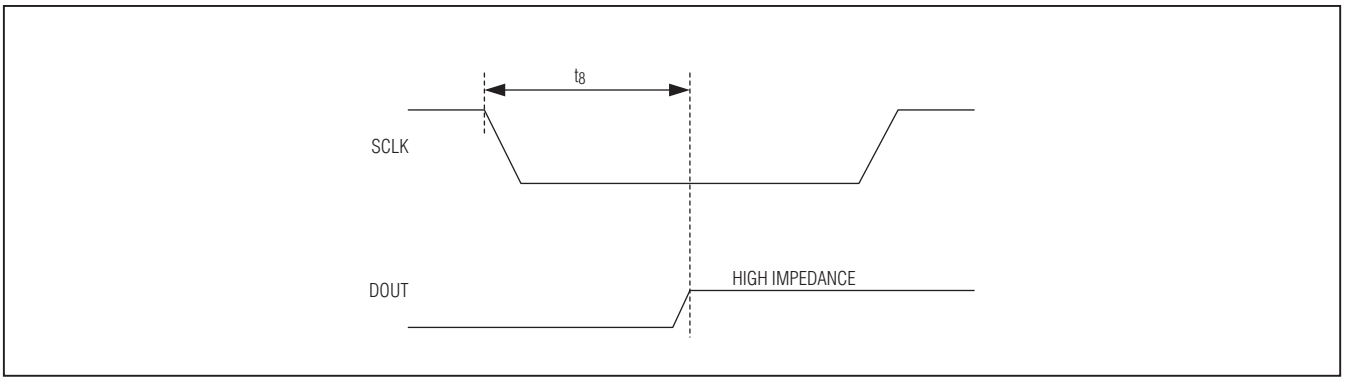
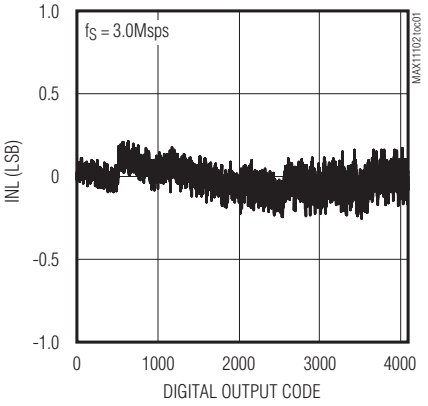


Figure 4. SCLK Falling Edge DOUT Three-State

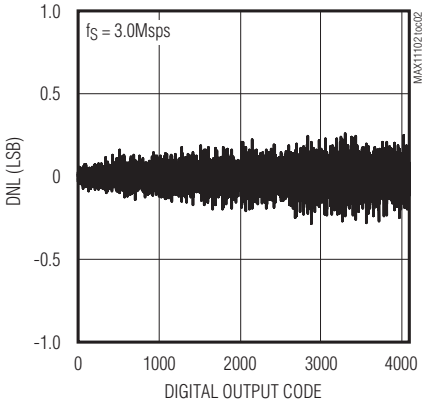
µMAX Typical Operating Characteristics

(MAX11103AUB+, T_A = +25°C, unless otherwise noted.)

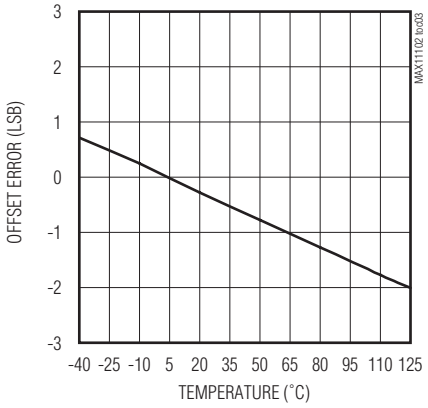
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



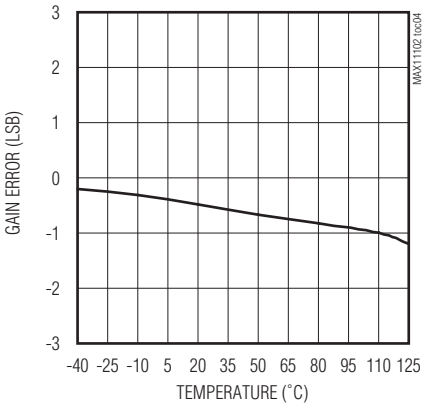
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



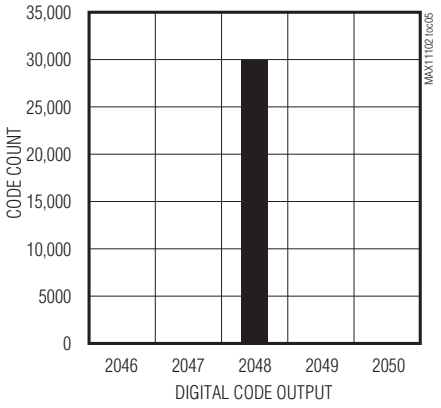
OFFSET ERROR vs. TEMPERATURE



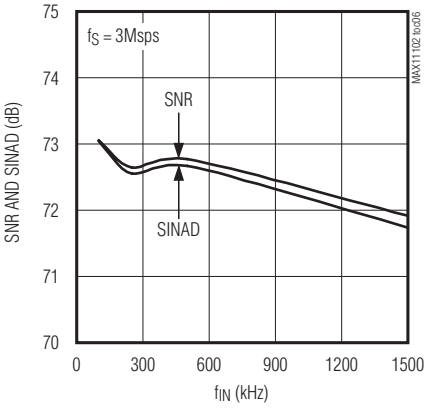
GAIN ERROR vs. TEMPERATURE



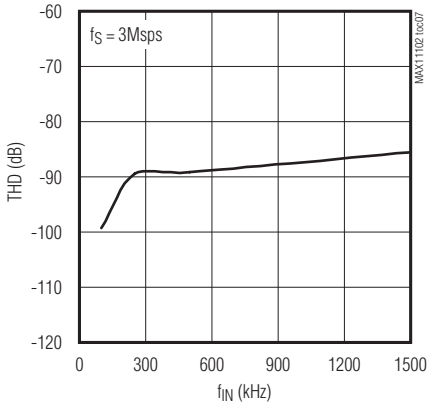
HISTOGRAM FOR 30,000 CONVERSIONS



SNR AND SINAD vs. ANALOG INPUT FREQUENCY



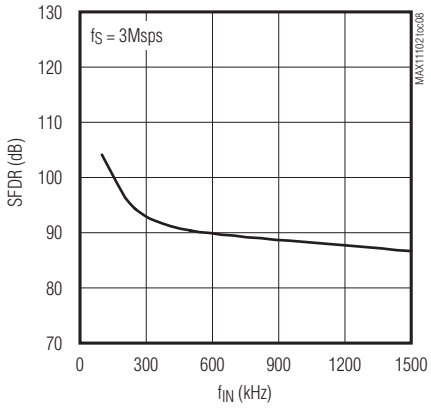
THD vs. ANALOG INPUT FREQUENCY



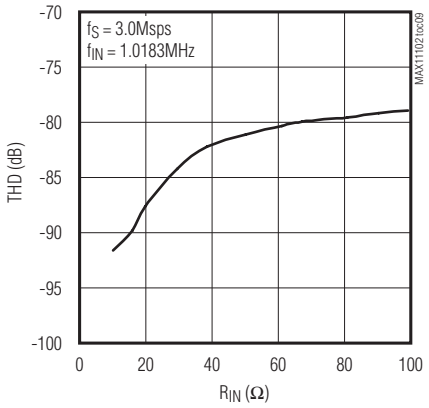
µMAX Typical Operating Characteristics (continued)

(MAX11103AUB+, T_A = +25°C, unless otherwise noted.)

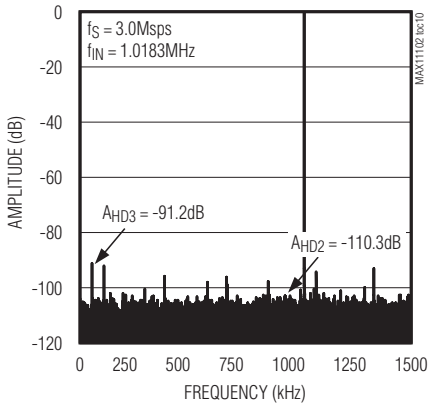
SFDR vs. ANALOG INPUT FREQUENCY



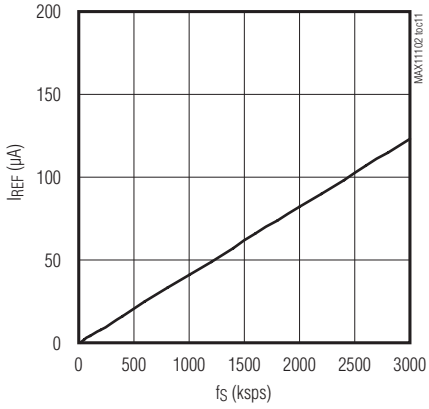
THD vs. INPUT RESISTANCE



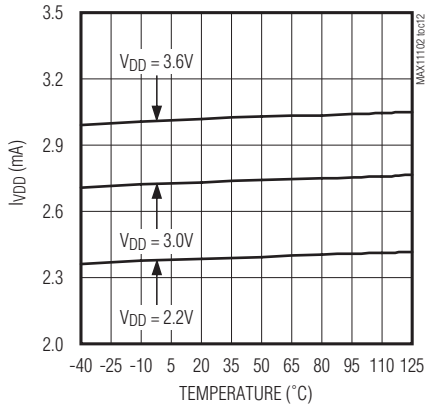
1MHz SINE-WAVE INPUT (16,834-POINT FFT PLOT)



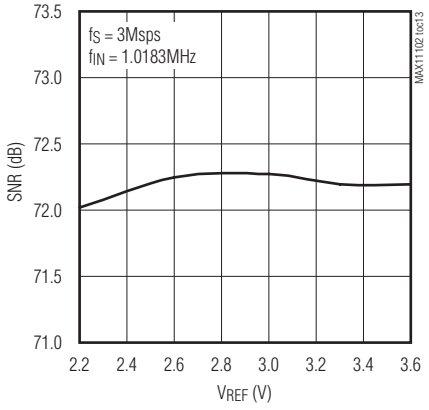
REFERENCE CURRENT vs. SAMPLING RATE



ANALOG SUPPLY CURRENT vs. TEMPERATURE



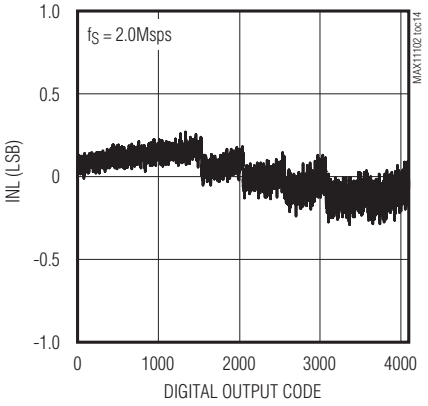
SNR vs. REFERENCE VOLTAGE



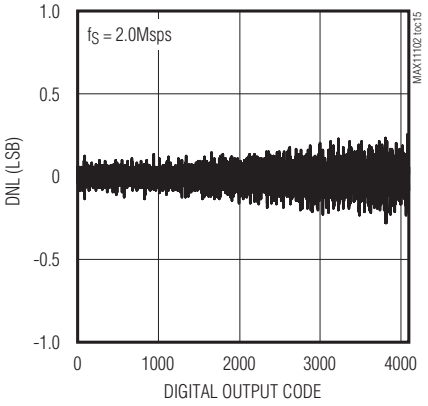
SOT Typical Operating Characteristics

(MAX11105AUB+, T_A = +25°C, unless otherwise noted.)

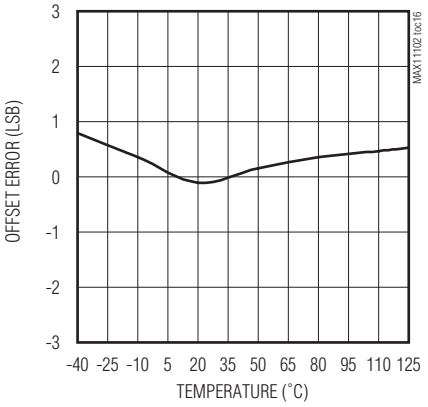
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



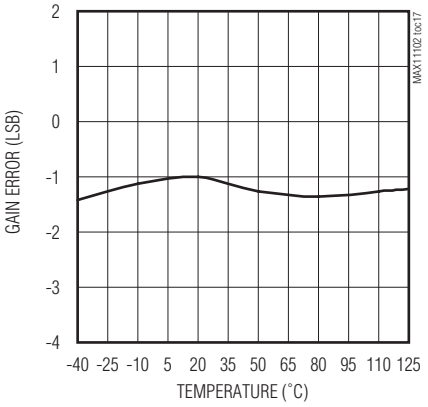
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



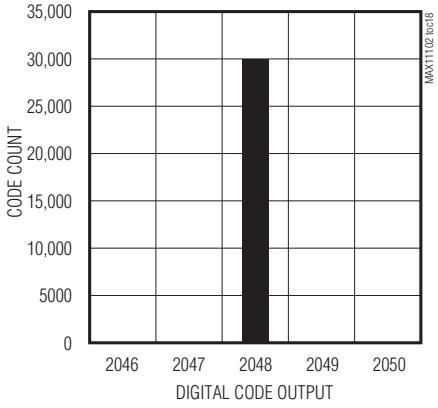
OFFSET ERROR vs. TEMPERATURE



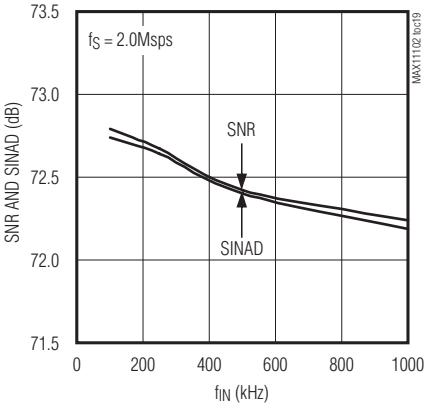
GAIN ERROR vs. TEMPERATURE



HISTOGRAM FOR 30,000 CONVERSIONS



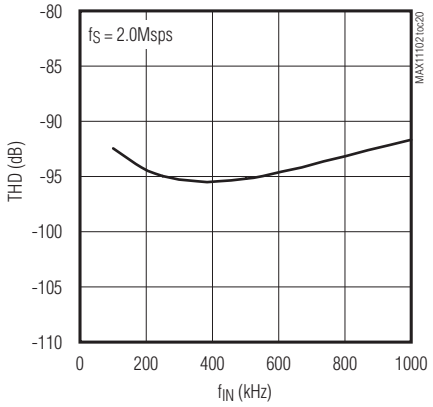
SNR AND SINAD vs. ANALOG INPUT FREQUENCY



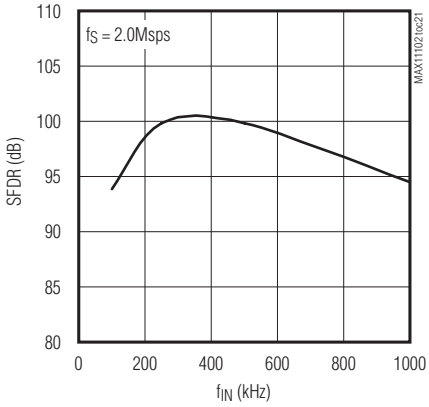
SOT Typical Operating Characteristics (continued)

(MAX11105AUB+, T_A = +25°C, unless otherwise noted.)

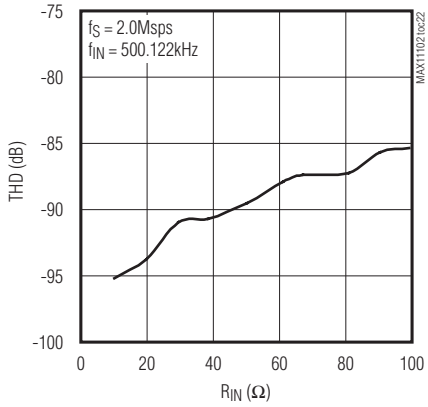
THD vs. ANALOG INPUT FREQUENCY



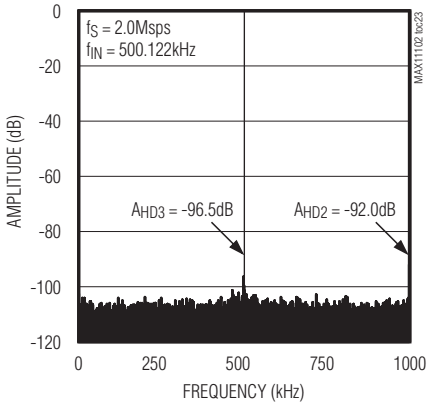
SFDR vs. ANALOG INPUT FREQUENCY



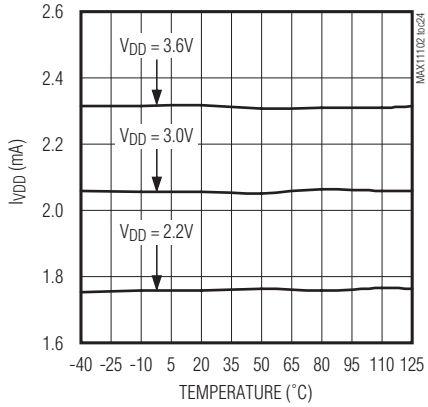
THD vs. INPUT RESISTANCE



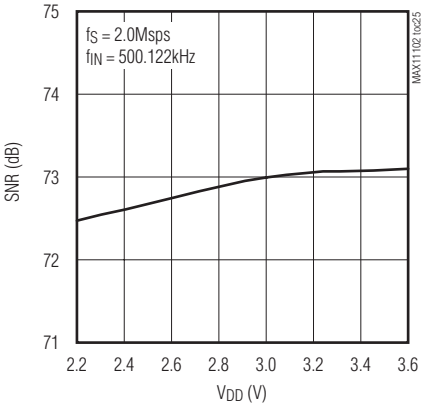
500kHz SINE-WAVE INPUT (16,834-POINT FFT PLOT)



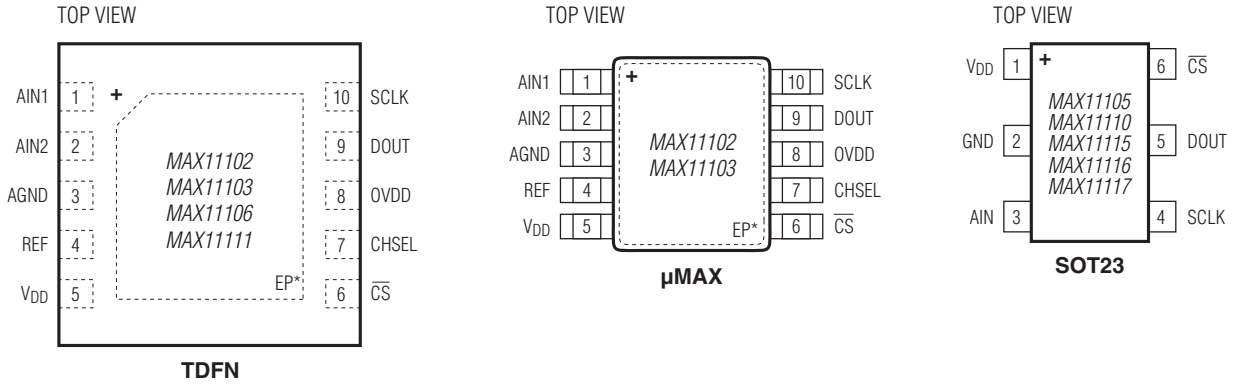
ANALOG SUPPLY CURRENT vs. TEMPERATURE



SNR vs. REFERENCE VOLTAGE (V_{DD})



Pin Configurations

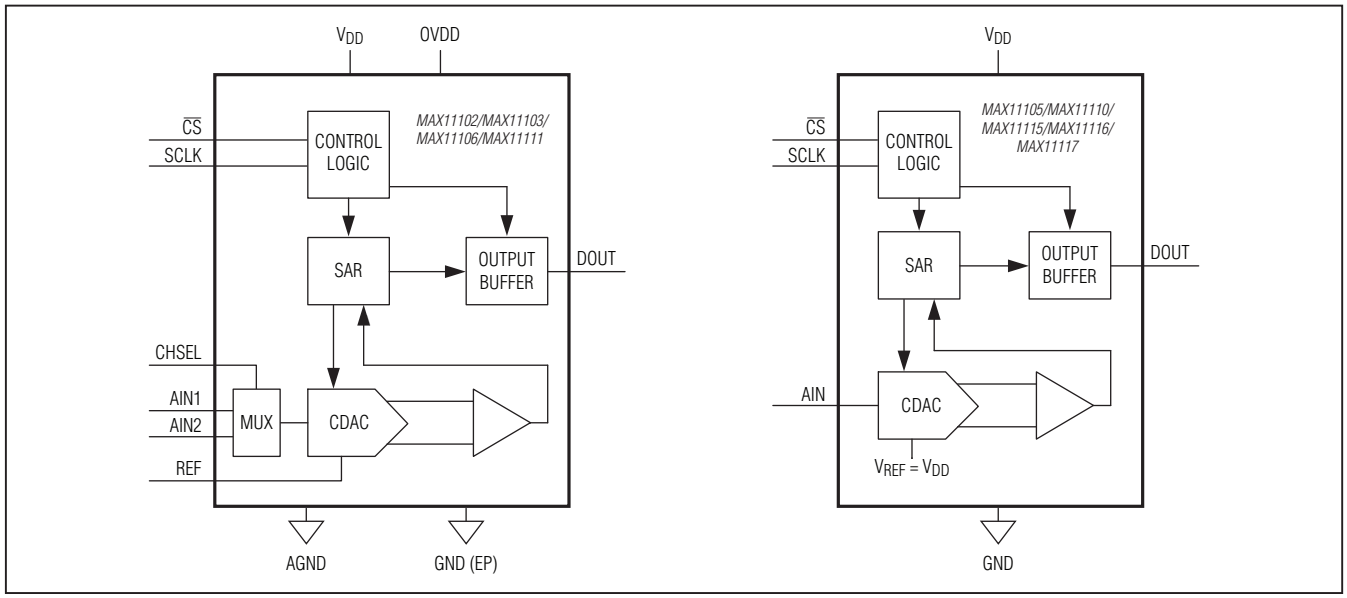


*CONNECT EXPOSED PAD TO GROUND PLANE. **DEVICES DO NOT OPERATE WHEN EP IS NOT CONNECTED TO GROUND!**

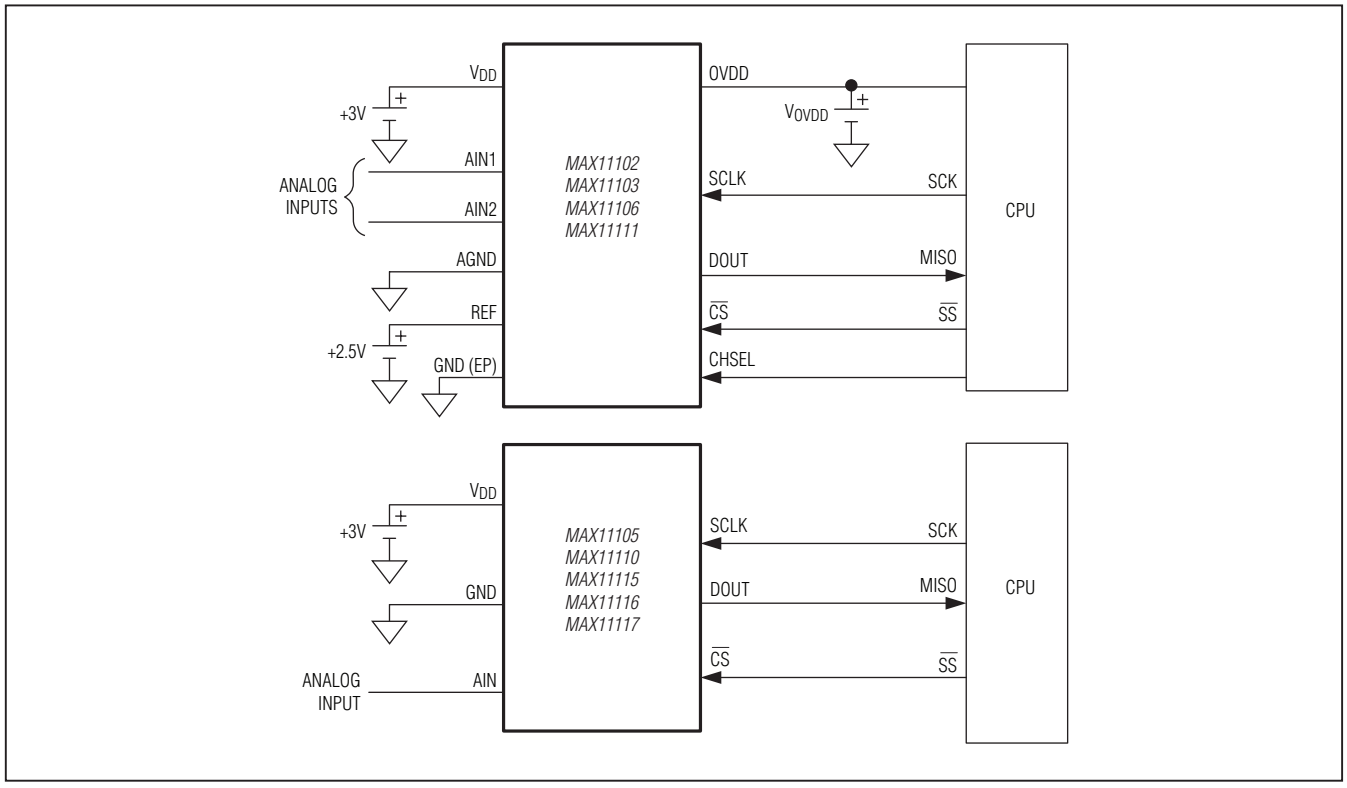
Pin Description

PIN			NAME	FUNCTION
TDFN	μMAX	SOT23		
1	1	—	AIN1	Analog Input Channel 1. Single-ended analog input with respect to AGND with range of 0V to V_{REF}.
2	2	—	AIN2	Analog Input Channel 2. Single-ended analog input with respect to AGND with range of 0V to V_{REF}.
—	—	3	AIN	Analog Input Channel. Single-ended analog input with respect to GND with range of 0V to V_{DD}.
—	—	2	GND	Ground. Connect GND to the GND ground plane.
3	3	—	AGND	Analog Ground. Connect AGND directly the GND ground plane.
4	4	—	REF	External Reference Input. REF defines the signal range of the input signal AIN1/AIN2: 0V to V_{REF}. The range of V_{REF} is 1V to V_{DD}. Bypass REF to AGND with 10μF ll 0.1μF capacitor.
5	5	1	V_{DD}	Positive Supply Voltage. Bypass V_{DD} with a 10μF ll 0.1μF capacitor to GND. V_{DD} range is 2.2V to 3.6V. For the SOT23 package, V_{DD} also defines the signal range of the input signal AIN: 0V to V_{DD}.
6	6	6	$\overline{CS}$	Active-Low Chip-Select Input. The falling edge of $\overline{CS}$ samples the analog input signal, starts a conversion, and frames the serial data transfer.
7	7	—	CHSEL	Channel Select. Set CHSEL high to select AIN2 for conversion. Set CHSEL low to select AIN1 for conversion.
8	8	—	OVDD	Digital Interface Supply for SCLK, $\overline{CS}$, DOUT, and CHSEL. The OVDD range is 1.5V to V_{DD}. Bypass OVDD with a 10μF ll 0.1μF capacitor to GND.
9	9	5	DOUT	Three-State Serial Data Output. ADC conversion results are clocked out on the falling edge of SCLK, MSB first. See Figure 1.
10	10	4	SCLK	Serial Clock Input. SCLK drives the conversion process. DOUT is updated on the falling edge of SCLK. See Figures 2 and 3.
—	—	EP	GND	Exposed Pad (TDFN and μMAX only). Connect EP directly to a solid ground plane. **Devices do not operate unless EP is connected to ground!**

Functional Diagrams



Typical Operating Circuit



Detailed Description

The MAX11102/MAX11103/MAX11105/MAX11106/MAX11110/MAX11111/MAX11115/MAX11116/MAX11117 are fast, 12-/10-/8-bit, low-power, single-supply ADCs. The devices operate from a 2.2V to 3.6V supply and consume only 8.3mW (V_{DD} = 3V)/5.2mW (V_{DD} = 2.2V) at 3Msps and 6.2mW (V_{DD} = 3V)/3.7mW (V_{DD} = 2.2V) at 2Msps. The 3Msps devices are capable of sampling at full rate when driven by a 48MHz clock and the 2Msps devices can sample at full rate when driven by a 32MHz clock. The dual-channel devices provide a separate digital supply input (OVDD) to power the digital interface enabling communication with 1.5V, 1.8V, 2.5V, or 3V digital systems.

The conversion result appears at DOUT, MSB first, with a leading zero followed by the 12-bit, 10-bit, or 8-bit result. A 12-bit result is followed by two trailing zeros, a 10-bit result is followed by four trailing zeros, and an 8-bit result is followed by six trailing zeros. See Figures 1 and 5.

The dual-channel devices feature a dedicated reference input (REF). The input signal range for AIN1/AIN2 is defined as 0V to V_{REF} with respect to AGND. The single-channel devices use V_{DD} as the reference. The input signal range of AIN is defined as 0V to V_{DD} with respect to GND.

These ADCs include a power-down feature allowing minimized power consumption at 2.5µA/ksps for lower throughput rates. The wake-up and power-down feature is controlled by using the SPI interface as described in the *Operating Modes* section.

Serial Interface

The devices feature a 3-wire serial interface that directly connects to SPI, QSPI, and MICROWIRE devices without external logic. Figures 1 and 5 show the interface signals for a single conversion frame to achieve maximum throughput.

The falling edge of $\overline{CS}$ defines the sampling instant. Once $\overline{CS}$ transitions low, the external clock signal (SCLK) controls the conversion.

The SAR core successively extracts binary-weighted bits in every clock cycle. The MSB appears on the data bus during the 2nd clock cycle with a delay outlined in the timing specifications. All extracted data bits appear successively on the data bus with the LSB appearing during the 13th/11th/9th clock cycle for 12-/10-/8-bit operation. The serial data stream of conversion bits is preceded by a leading “zero” and succeeded by trailing “zeros.” The data output (DOUT) goes into high-impedance state during the 16th clock cycle.

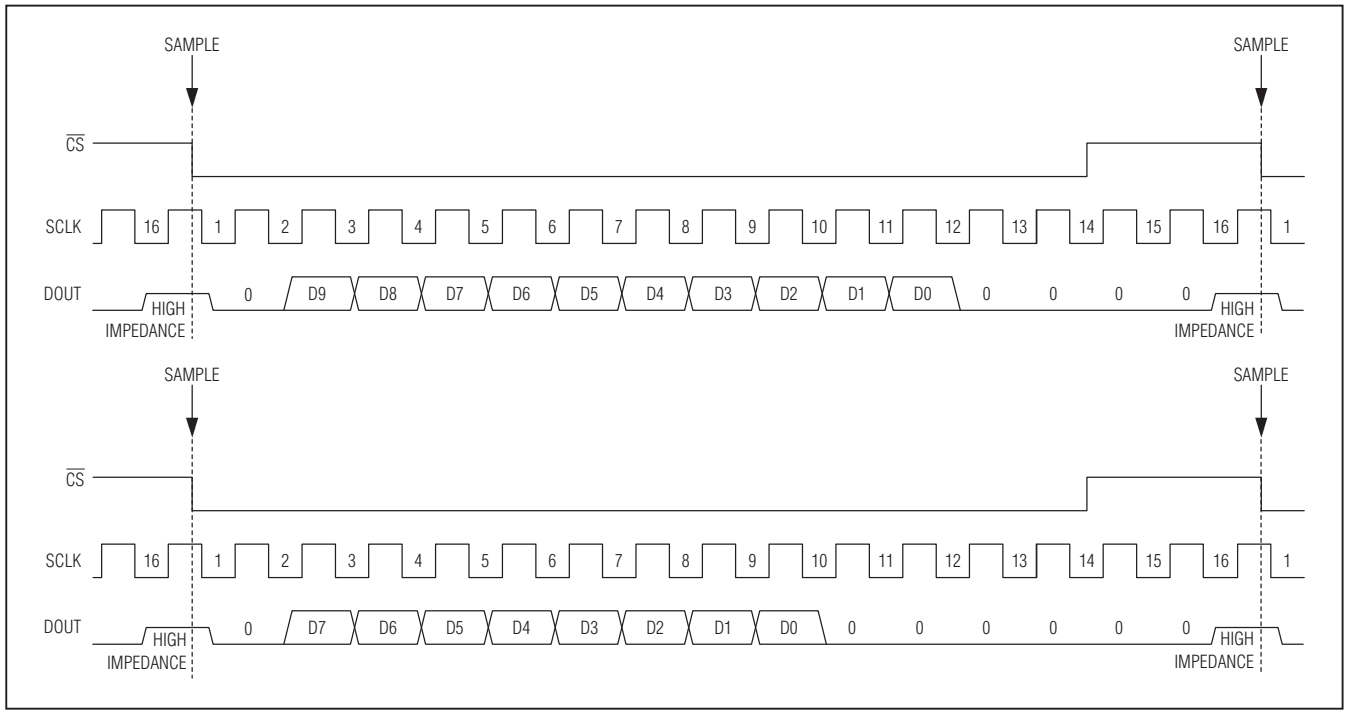


Figure 5. 10-/8-Bit Timing Diagrams

To sustain the maximum sample rate, all devices have to be resampled immediately after the 16th clock cycle. For lower sample rates, the $\overline{CS}$ falling edge can be delayed leaving DOUT in a high-impedance condition. Pull $\overline{CS}$ high after the 10th SCLK falling edge (see the *Operating Modes* section).

Analog Input

The devices produce a digital output that corresponds to the analog input voltage within the specified operating range of 0 to V_{REF} for the dual-channel devices and 0 to V_{DD} for the single-channel devices.

Figure 6 shows an equivalent circuit for the analog input AIN (for single-channel devices) and AIN1/AIN2 (for dual-channel devices). Internal protection diodes D1/D2 confine the analog input voltage within the power rails (V_{DD}, GND). The analog input voltage can swing from GND - 0.3V to V_{DD} + 0.3V without damaging the device.

The electric load presented to the external stage driving the analog input varies depending on which mode the ADC is in: track mode vs. conversion mode. In track mode, the internal sampling capacitor C_S (16pF) has to be charged through the resistor R (R = 50Ω) to the input voltage. For faithful sampling of the input, the capacitor voltage on C_S has to settle to the required accuracy during the track time.

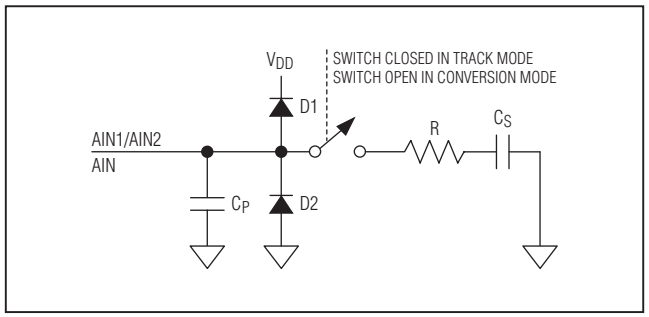


Figure 6. Analog Input Circuit

The source impedance of the external driving stage in conjunction with the sampling switch resistance affects the settling performance. The THD vs. Input Resistance graph in the *Typical Operating Characteristics* shows THD sensitivity as a function of the signal source impedance. Keep the source impedance at a minimum for high-dynamic performance applications. Use a high-performance op amp such as the MAX4430 to drive the analog input, thereby decoupling the signal source and the ADC.

While the ADC is in conversion mode, the sampling switch is open presenting a pin capacitance, C_P (C_P = 5pF), to the driving stage. See the *Applications Information* section for information on choosing an appropriate buffer for the ADC.

ADC Transfer Function

The output format is straight binary. The code transitions midway between successive integer LSB values such as 0.5 LSB, 1.5 LSB, etc. The LSB size for single-channel devices is $V_{DD}/2^n$ and for dual-channel devices is $V_{REF}/2^n$, where n is the resolution. The ideal transfer characteristic is shown in Figure 10.

Operating Modes

The ICs offer two modes of operation: normal mode and power-down mode. The logic state of the $\overline{CS}$ signal during a conversion activates these modes. The power-down mode can be used to optimize power dissipation with respect to sample rate.

Normal Mode

In normal mode, the devices are powered up at all times, thereby achieving their maximum throughput rates. Figure 7 shows the timing diagram of these devices in normal mode. The falling edge of $\overline{CS}$ samples the analog input signal, starts a conversion, and frames the serial data transfer.

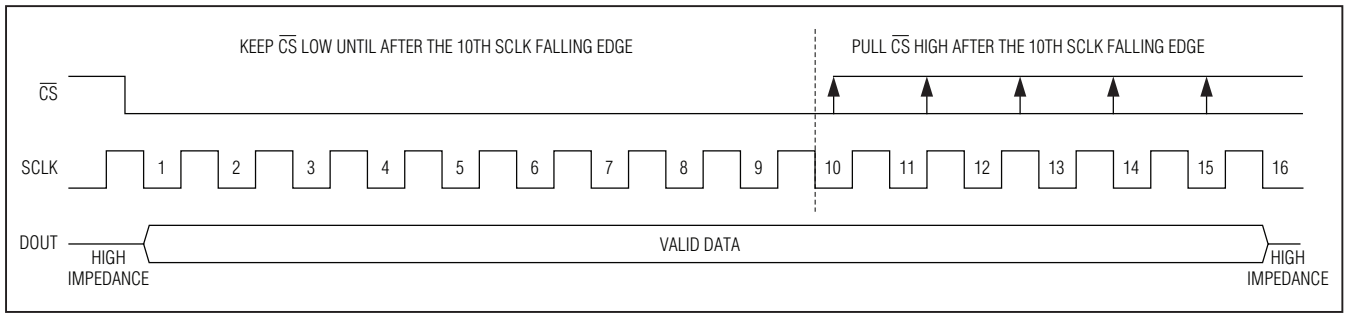


Figure 7. Normal Mode

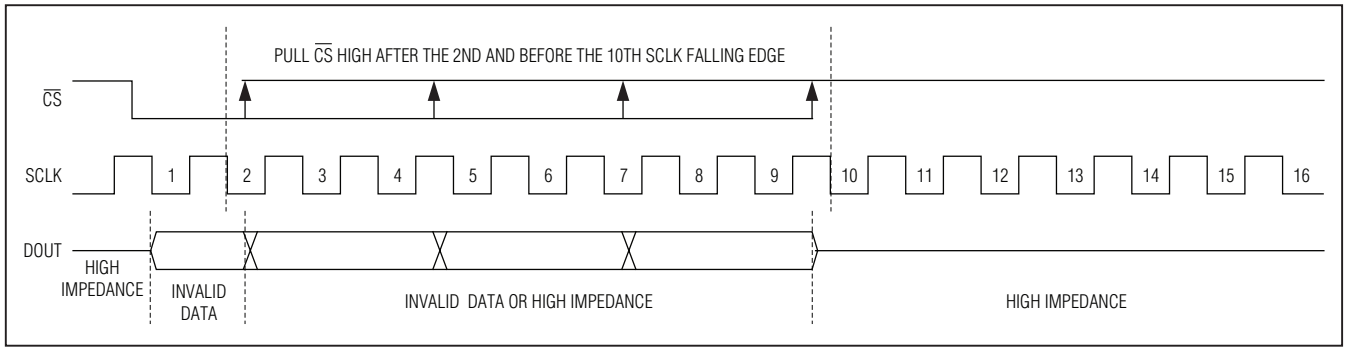


Figure 8. Entering Power-Down Mode

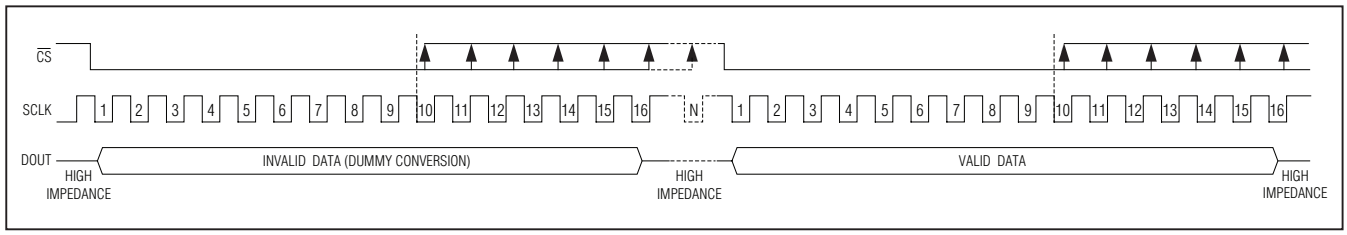


Figure 9. Exiting Power-Down Mode

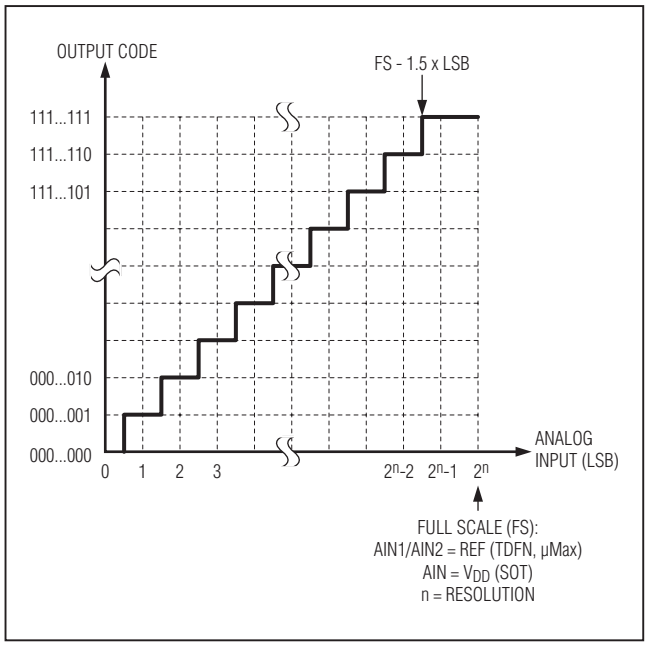


Figure 10. ADC Transfer Function

To remain in normal mode, keep $\overline{CS}$ low until the falling edge of the 10th SCLK cycle. Pulling $\overline{CS}$ high after the 10th SCLK falling edge keeps the part in normal mode. However, pulling $\overline{CS}$ high before the 10th SCLK falling edge terminates the conversion, DOUT goes into high-impedance mode, and the device enters power-down mode. See Figure 8.

Power-Down Mode

In power-down mode, all bias circuitry is shut down drawing typically only 1.3µA of leakage current. To save power, put the device in power-down mode between conversions. Using the power-down mode between conversions is ideal for saving power when sampling the analog input infrequently.

Entering Power-Down Mode

To enter power-down mode, drive $\overline{CS}$ high between the 2nd and 10th falling edges of SCLK (see Figure 8). By pulling $\overline{CS}$ high, the current conversion terminates and DOUT enters high impedance.

Exiting Power-Down Mode

To exit power-down mode, implement one dummy conversion by driving $\overline{CS}$ low for at least 10 clock cycles (see Figure 9). The data on DOUT is invalid during this dummy conversion. The first conversion following the dummy cycle contains a valid conversion result.

The power-up time equals the duration of the dummy cycle, and is dependent on the clock frequency. The power-up time for 3Msps operation (48MHz SCLK) is 333ns. The power-up time for 2Msps operation (32MHz SCLK) is 500ns.

Supply Current vs. Sampling Rate

For applications requiring lower throughput rates, the user can reduce the clock frequency (f_{SCLK}) to lower the sample rate. Figure 11 shows the typical supply current (I_{VDD}) as a function of sample rate (f_S) for the 3Msps devices. The part operates in normal mode and is never powered down. Figure 13 pertains to the 2Msps devices.

The user can also power down the ADC between conversions by using the power-down mode. Figure 12 shows for the 3Msps device that as the sample rate is reduced, the device remains in the power-down state longer and the average supply current (I_{VDD}) drops accordingly. Figure 14 pertains to the 2Msps devices.

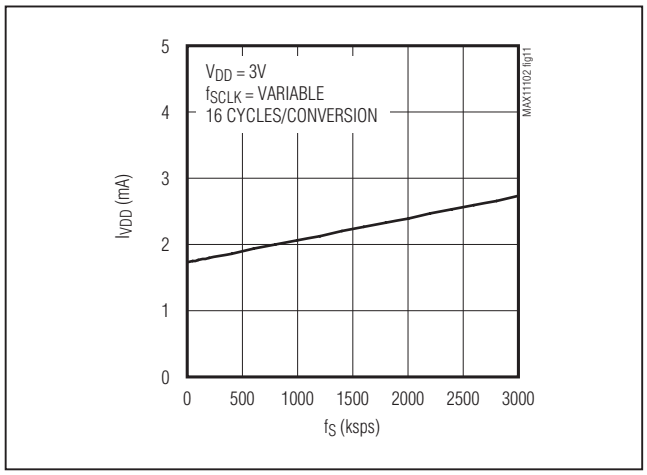


Figure 11. Supply Current vs. Sample Rate (Normal Operating Mode, 3Msps Devices)

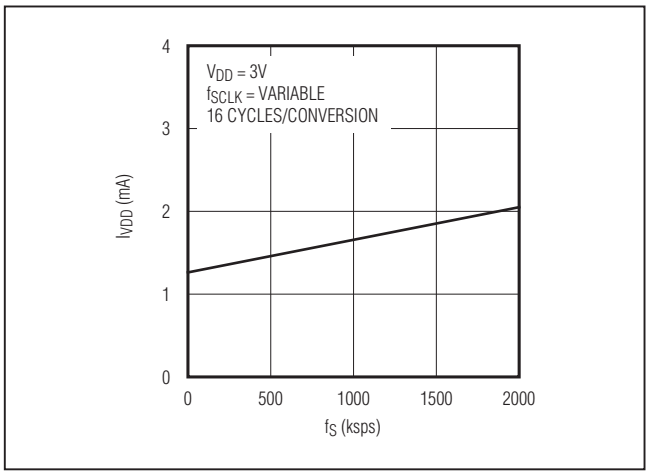


Figure 13. Supply Current vs. Sample Rate (Normal Operating Mode, 2Msps Devices)

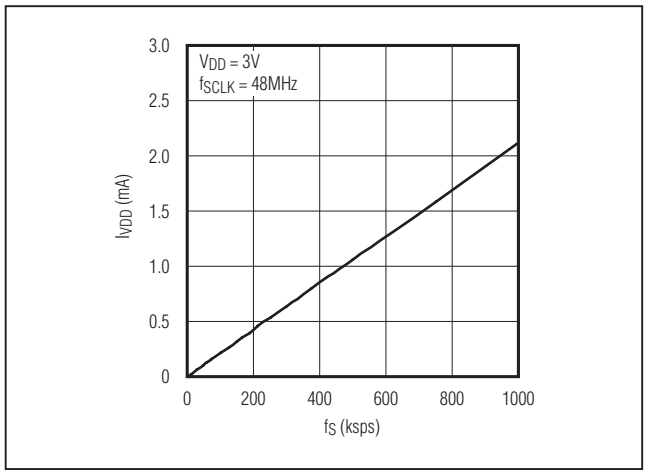


Figure 12. Supply Current vs. Sample Rate (Device Powered Down Between Conversions, 3Msps Devices)

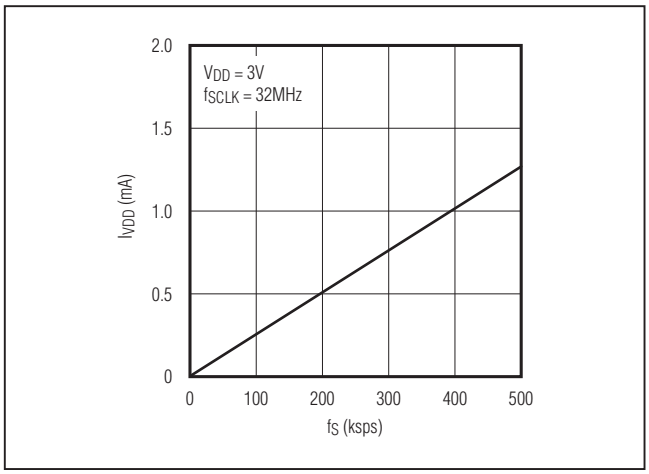


Figure 14. Supply Current vs. Sample Rate (Device Powered Down Between Conversions, 2Msps Devices)

Dual-Channel Operation

The MAX11102/MAX11103/MAX11106/MAX11111 feature dual-input channels. These devices use a channel-select (CHSEL) input to select between analog input AIN1 (CHSEL = 0) or AIN2 (CHSEL = 1). As shown in Figure 15, the CHSEL signal is required to change between the 2nd and 12th clock cycle within a regular conversion to guarantee proper switching between channels.

14-Cycle Conversion Mode

The ICs can operate with 14 cycles per conversion. Figure 16 shows the corresponding timing diagram. Observe that DOUT does not go into high-impedance mode. Also, observe that t_{ACQ} needs to be sufficiently long to guarantee proper settling of the analog input voltage. See the *Electrical Characteristics* table for t_{ACQ} requirements and the *Analog Input* section for a description of the analog inputs.

Applications Information

Layout, Grounding, and Bypassing

For best performance, use PCBs with a solid ground plane. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package. Noise in the V_{DD} power supply, OVDD, and REF affects the ADC's performance. Bypass the V_{DD}, OVDD, and REF to ground with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead and trace lengths for best supply-noise rejection.

Choosing an Input Amplifier

It is important to match the settling time of the input amplifier to the acquisition time of the ADC. The conversion results are accurate when the ADC samples the input signal for an interval longer than the input signal's worst-case settling time. By definition, settling time is the interval between the application of an input voltage step and the point at which the output signal reaches

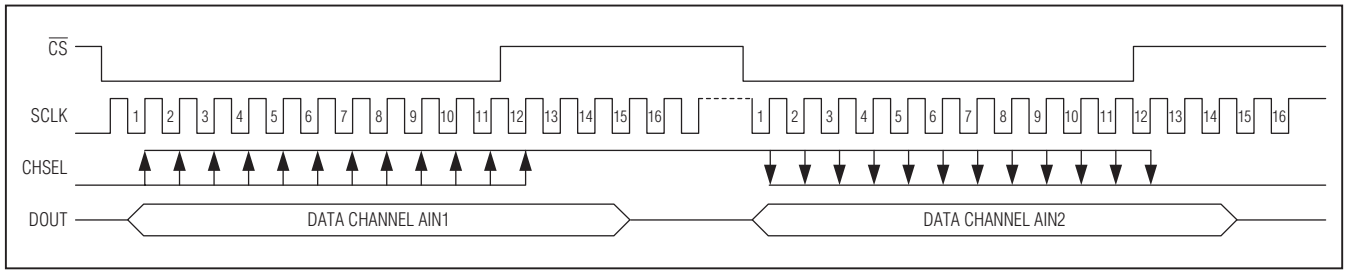


Figure 15. Channel Select Timing Diagram

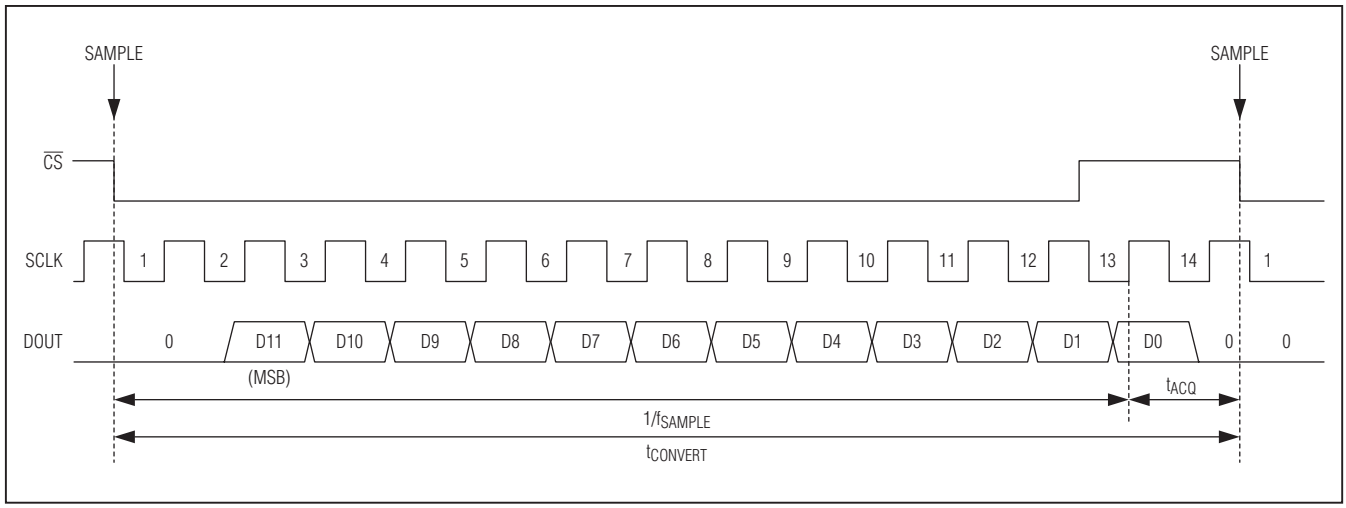


Figure 16. 14-Clock Cycle Operation

and stays within a given error band centered on the resulting steady-state amplifier output level. The ADC input sampling capacitor charges during the sampling cycle, referred to as the acquisition period. During this acquisition period, the settling time is affected by the input resistance and the input sampling capacitance. This error can be estimated by looking at the settling of an RC time constant using the input capacitance and the source impedance over the acquisition time period.

Figure 17 shows a typical application circuit. The MAX4430, offering a settling time of 37ns at 16 bits, is an excellent choice for this application. See the THD vs. Input Resistance graph in the *Typical Operating Characteristics*.

Choosing a Reference

For devices using an external reference, the choice of the reference determines the output accuracy of the ADC. An ideal voltage reference provides a perfect initial accuracy and maintains the reference voltage independent of changes in load current, temperature, and time. Considerations in selecting a reference include initial voltage accuracy, temperature drift, current source, sink capability, quiescent current, and noise. Figure 17 shows a typical application circuit using the MAX6126 to provide the reference voltage. The MAX6033 and MAX6043 are also excellent choices.

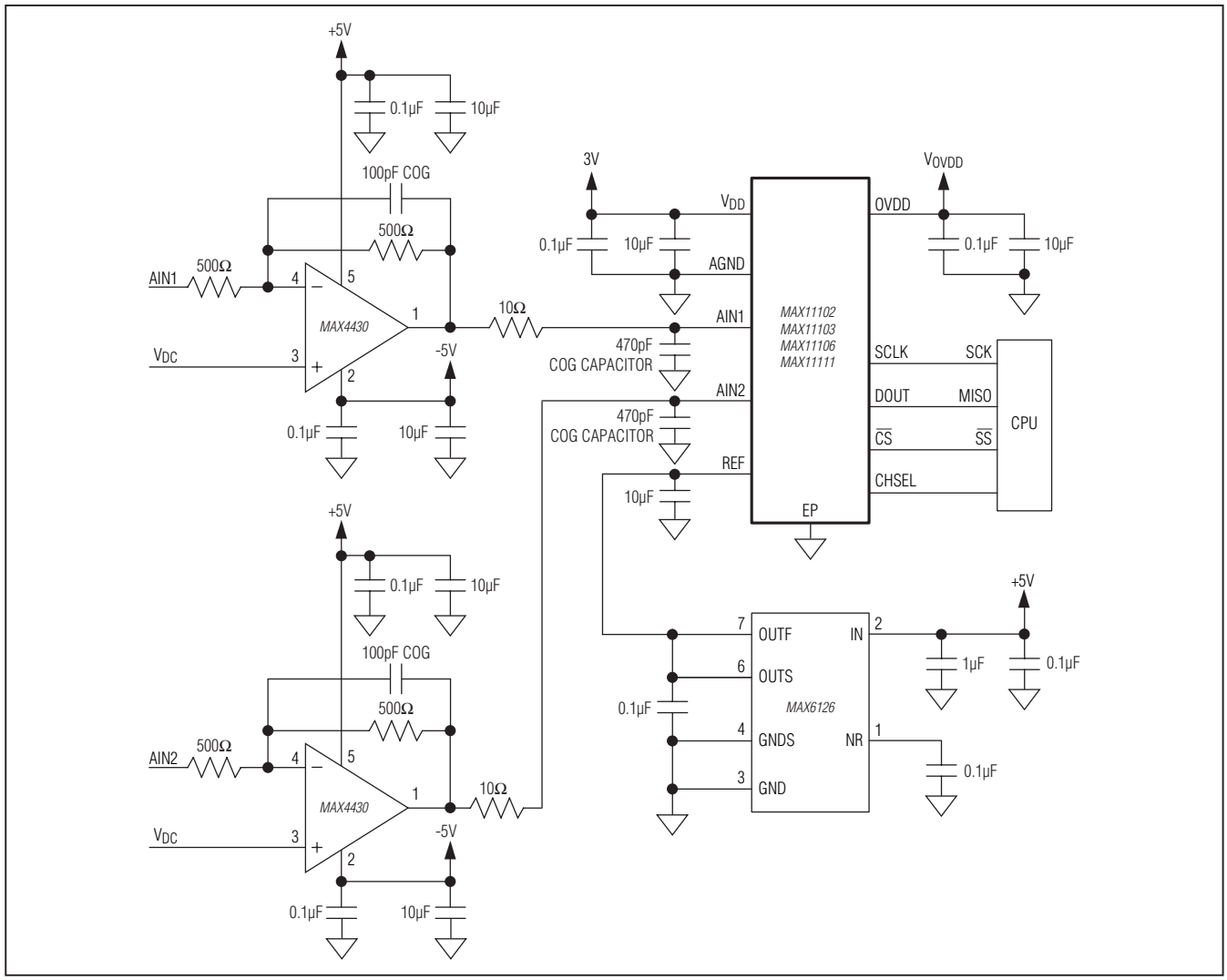


Figure 17. Typical Application Circuit

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, the straight line is a line drawn between the end points of the transfer function after offset and gain errors are nulled.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of ±1 LSB or less guarantees no missing codes and a monotonic transfer function.

Offset Error

The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

Gain Error

The deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal after adjusting for the offset error, that is, V_{REF} - 1.5 LSB.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the falling edge of sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio (SNR)

SNR is a dynamic figure of merit that indicates the converter's noise performance. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR\ (dB)\ (MAX) = (6.02 \times N + 1.76)\ (dB)$$

In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter that also degrade SNR. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Ratio and Distortion (SINAD)

SINAD is a dynamic figure of merit that indicates the converter's noise and distortion performance. SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset:

$$SINAD(dB) = 20 \times \log\left[\frac{SIGNAL_{RMS}}{(NOISE + DISTORTION)_{RMS}}\right]$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude and V_2–V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is a dynamic figure of merit that indicates the lowest usable input signal amplitude. SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR is specified in decibels with respect to the carrier (dBc).

Full-Power Bandwidth

Full-power bandwidth is the frequency at which the input signal amplitude attenuates by 3dB for a full-scale input.

Full-Linear Bandwidth

Full-linear bandwidth is the frequency at which the signal-to-noise ratio and distortion (SINAD) is equal to a specified value.

Intermodulation Distortion

Any device with nonlinearities creates distortion products when two sine waves at two different frequencies (f_1 and f_2) are applied into the device. Intermodulation distortion (IMD) is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones, f_1 and f_2. The individual input tone levels are at -6dBFS.

Ordering Information (continued)

PART	PIN-PACKAGE	BITS	SPEED (Msps)	NO. OF CHANNELS	TOP MARK
MAX11105AUT+	6 SOT23	12	2	1	+ACON
MAX11106ATB+	10 TDFN-EP*	10	3	2	+AWJ
MAX11110AUT+	6 SOT23	10	2	1	+ACOO
MAX11111ATB+	10 TDFN-EP*	8	3	2	+AWL
MAX11115AUT+	6 SOT23	8	2	1	+ACOP
MAX11116AUT+	6 SOT23	8	3	1	+ACOX
MAX11117AUT+	6 SOT23	10	3	1	+ACOY

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1033+2	**21-0137**	**90-0061**
10 µMAX-EP	U10E+3	**21-0109**	**90-0148**
6 SOT23	U6+1	**21-0058**	**90-0175**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release of the MAX11102/MAX11103/MAX11105/MAX11110/MAX11115/ MAX11116/MAX11117	—
1	7/10	Initial release of the MAX11106/MAX11111.	1–30
2	9/10	Corrected the package code of the µMAX package in the *Package Information* section.	29
3	10/10	Changed the typical power consumption to 2.2V in the *General Description*, *Features*, and *Detailed Description* sections.	1, 22
4	2/11	Update style, change voltage in Figure 17.	4, 5, 8, 9, 10, 12, 13, 14, 27
5	8/11	Updated the *Ordering Information* and *Electrical Characteristics* sections.	1, 4, 6, 8, 10, 12, 14, 29
6	10/11	Updated Figures 15 and 16.	26, 27
7	9/12	Corrected top mark information in *Ordering Information* section.	1, 29

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