



Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543T/AT/CT/DT
IDT54/74FCT2543T/AT/CT

FEATURES:

• Common features:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

• Features for FCT543T:

- Std., A, C and D speed grades
- High drive outputs (-15mA I_{OH} , 64mA I_{OL})
- Power off disable outputs permit "live insertion"

• Features for FCT2543T:

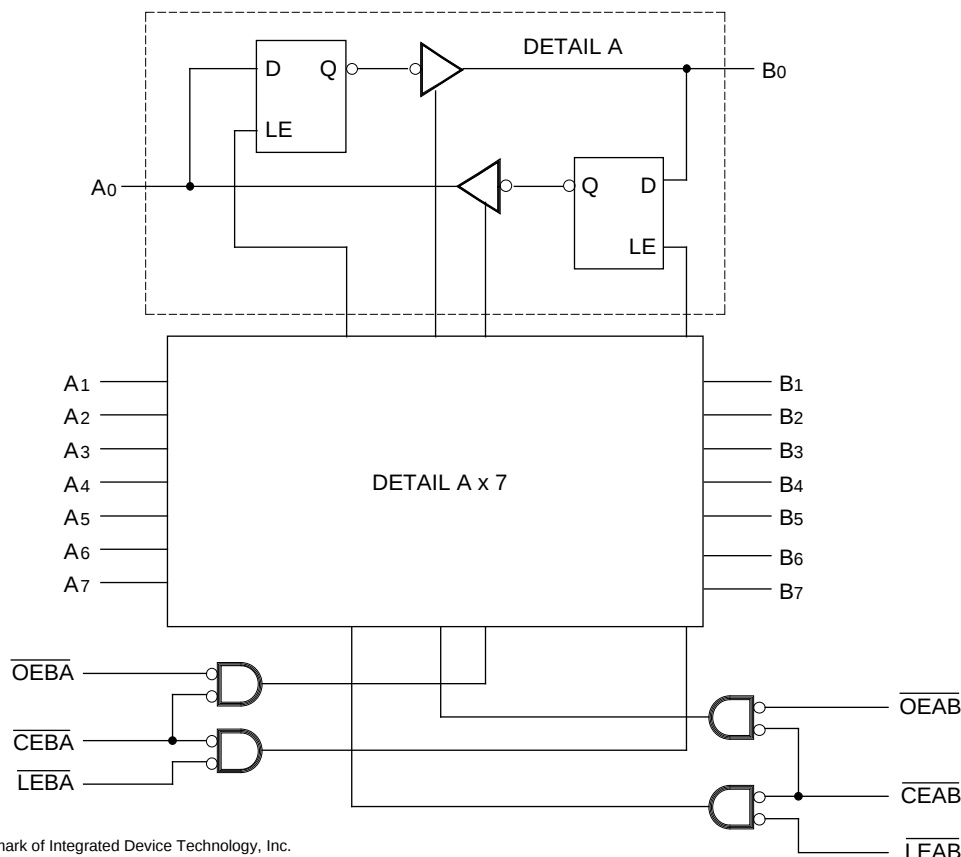
- Std., A, and C speed grades
- Resistor outputs (-15mA I_{OH} , 12mA I_{OL} Com.)
(-12mA I_{OH} , 12mA I_{OL} Mil.)
- Reduced system switching noise

DESCRIPTION:

The FCT543T/FCT2543T is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{CEAB}}$) input must be LOW in order to enter data from A_0 – A_7 or to take data from B_0 – B_7 , as indicated in the Function Table. With $\overline{\text{CEAB}}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$ and $\overline{\text{OEBA}}$ inputs.

The FCT2543T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM

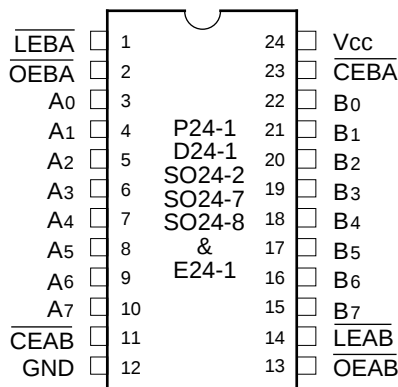


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

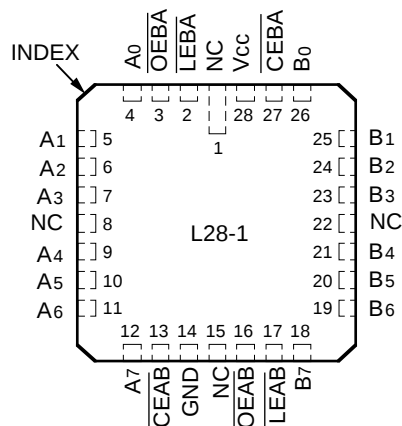
JANUARY 1995

PIN CONFIGURATIONS



2613 drw 02

DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



2613 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0–A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0–B7	B-to-A Data Inputs or A-to-B 3-State Outputs

2613 tbl 01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	–0.5 to $V_{CC} + 0.5$	–0.5 to $V_{CC} + 0.5$	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2613 lmk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

FUNCTION TABLE^(1, 2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:

2613 tbl 02

- * Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
— = Don't Care or Irrelevant
- A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

2613 lmk 04

NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	μA
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	mA

2613 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR 543T/AT/CT/DT

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.3	0.55	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$		—	—	± 1	μA

2613 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR 2543T/AT/CT/DT

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$		16	48	—	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$		-16	-48	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12\text{mA}$	—	0.3	0.50	V

NOTES:

2613 Ink 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾			Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	FCTxxxT	—	2.0	5.5	
				FCT2xxxT	—	1.1	4.2	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	3.8	7.3 ⁽⁵⁾	
				FCT2xxxT	—	1.5	4.0 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	FCTxxxT	—	6.0	16.3 ⁽⁵⁾	
				FCT2xxxT	—	3.8	13.0 ⁽⁵⁾	

NOTES:

2613 tbl 08

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT543T/ FCT2543T				FCT543AT/ FCT2543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10.0	1.5	6.5	1.5	7.5	ns
tPLH tPHL	Propagation Delay LEBA to An, LEAB to Bn		1.5	12.5	1.5	14.0	1.5	8.0	1.5	9.0	ns
tpZH tpZL	Output Enable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn		1.5	12.0	1.5	14.0	1.5	9.0	1.5	10.0	ns
tPHZ tPLZ	Output Disable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn		1.5	9.0	1.5	13.0	1.5	7.5	1.5	8.5	ns
tsu	Set-up Time, HIGH or LOW An or Bn to LEBA or LEAB		3.0	—	3.0	—	2.0	—	2.0	—	ns
th	Hold Time, HIGH or LOW An or Bn to LEBA or LEAB		2.0	—	2.0	—	2.0	—	2.0	—	ns
tw	LEBA or LEAB Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns

2513 tbl 09

Symbol	Parameter	Condition ⁽¹⁾	FCT543CT/ FCT2543CT				FCT543DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	1.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay <u>LEBA</u> to An, <u>LEAB</u> to Bn		1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
tpZH tpZL	Output Enable Time <u>OEBA</u> or <u>OEAB</u> to An or Bn <u>CEBA</u> or <u>CEAB</u> to An or Bn		1.5	8.0	1.5	9.0	1.5	5.4	—	—	ns
tPHZ tPLZ	Output Disable Time <u>OEBA</u> or <u>OEAB</u> to An or Bn <u>CEBA</u> or <u>CEAB</u> to An or Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
tsU	Set-up Time, HIGH or LOW An or Bn to <u>LEBA</u> or <u>LEAB</u>		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW An or Bn to <u>LEBA</u> or <u>LEAB</u>		2.0	—	2.0	—	1.5	—	—	—	ns
tw	<u>LEBA</u> or <u>LEAB</u> Pulse Width LOW		5.0	—	5.0	—	3.0 ⁽³⁾	—	—	—	ns

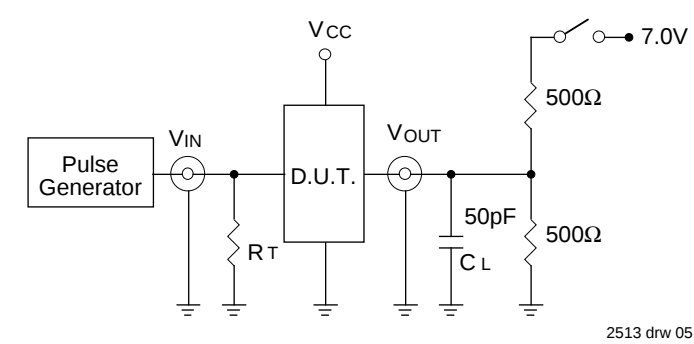
NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This limit is guaranteed but not tested.

2513 tbl 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

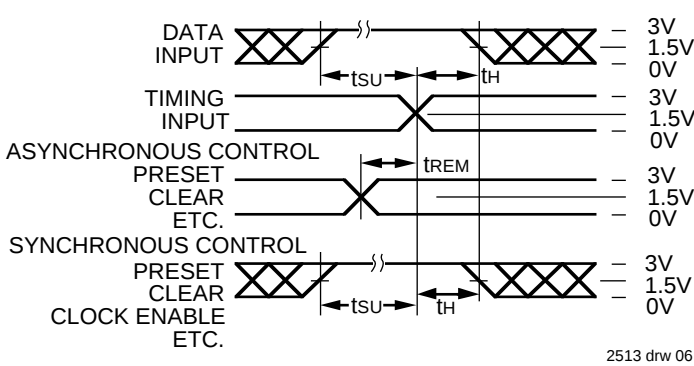


SWITCH POSITION

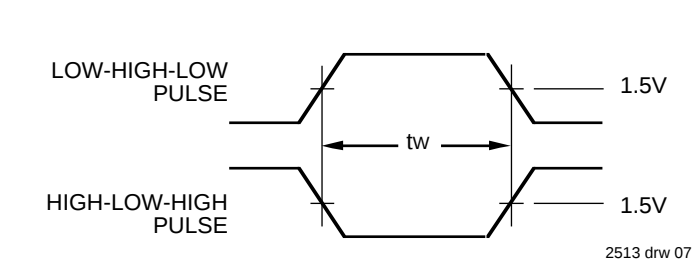
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

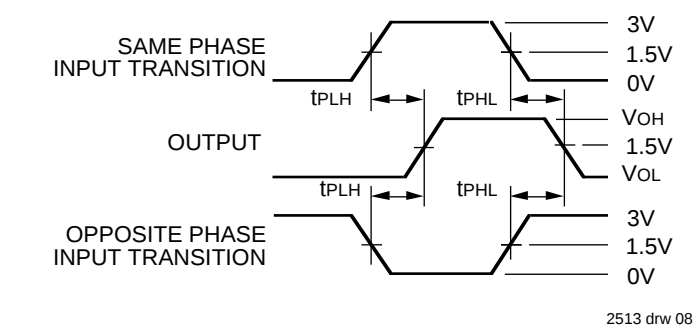
SET-UP, HOLD AND RELEASE TIMES



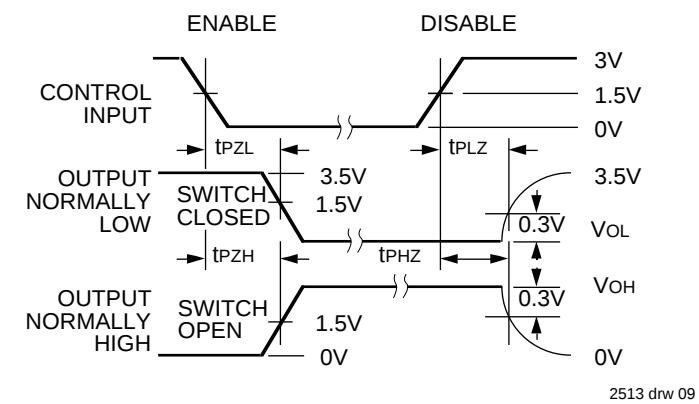
PULSE WIDTH



PROPAGATION DELAY

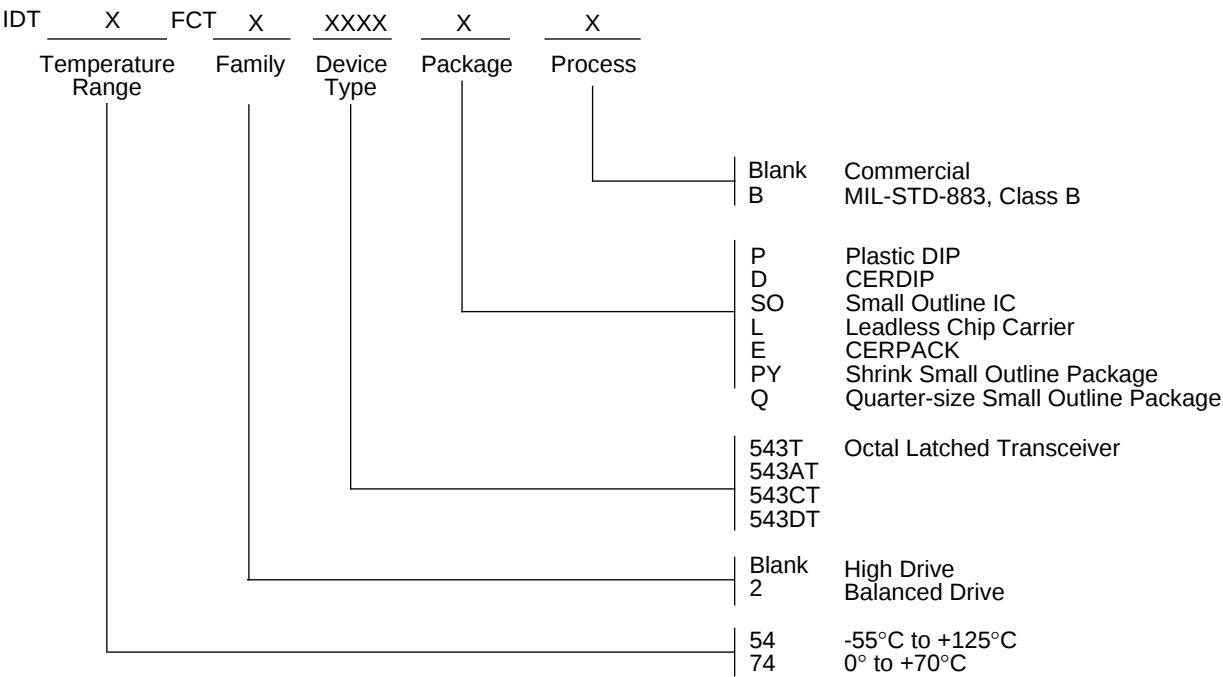


ENABLE AND DISABLE TIMES



- NOTES:
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
 - Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION



2613 drw 10