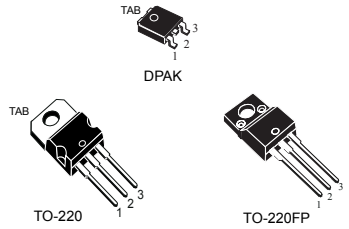
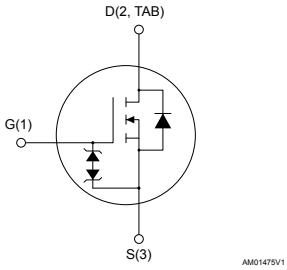
STD5NK60ZT4, STP5NK60Z, STP5NK60ZFP

Datasheet

N-channel 600 V, 1.2 Ω typ., 5 A SuperMESH™ Power MOSFET in DPAK, TO-220 and TO-220FP packages





Product status link
STD4NK60ZT4
STP5NK60Z
STP5NK60ZFP

Features

Order codes	V_{DS} @ $T_{jmax.}$	$R_{DS(on)}$ max.	Package
STD5NK60ZT4	650 V	1.6 Ω	DPAK
STP5NK60Z			TO-220
STP5NK60ZFP			TO-220FP

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK,TO-220	TO-220FP	
V_{DS}	Drain-source voltage	600		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	5	5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.16	3.16 (1)	A
I_{DM} (2)	Drain current (pulsed)	20	20 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	25	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	3		kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)		2.5	kV
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
T_j	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 5 A, di/dt ≤ 200 A/µs, V_{DSpeak} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39		5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5		°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50			°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	220	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.5 A		1.2	1.6	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	690		pF
C_{oss}	Output capacitance			90		
C_{rss}	Reverse transfer capacitance			20		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	40		pF
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 5 A, V_{GS} = 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)	-	26	34	nC
Q_{gs}	Gate-source charge			6		
Q_{gd}	Gate-drain charge			14		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	16	-	ns
t_r	Rise time			25		
$t_{d(off)}$	Turn-off delay time			36		
t_f	Fall time			25		
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 480 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 17. Test circuit for inductive load switching and diode recovery times and Figure 20. Switching time waveform)		12		
t_f	Fall time			10		
t_c	Cross-over time			24		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)				20	
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs	-	485		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 30 V (see Figure 17. Test circuit for inductive load switching and diode recovery times)		2.7		µC
I_{RRM}	Reverse recovery current			11		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-Source Zener Diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for DPAK and TO-220

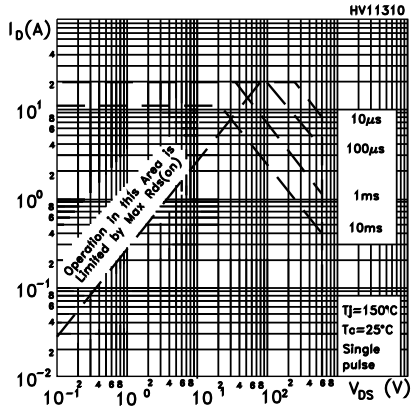


Figure 2. Thermal impedance for DPAK and TO-220

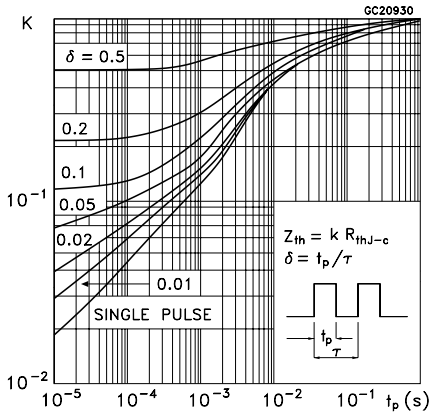


Figure 3. Safe operating area for TO-220FP

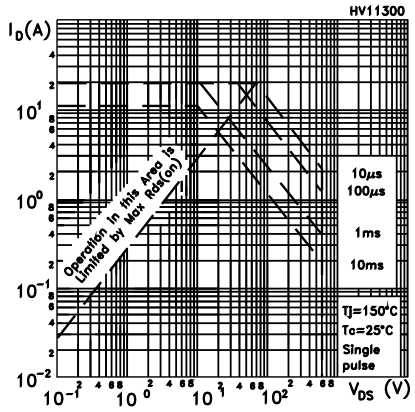


Figure 4. Thermal impedance for TO-220FP

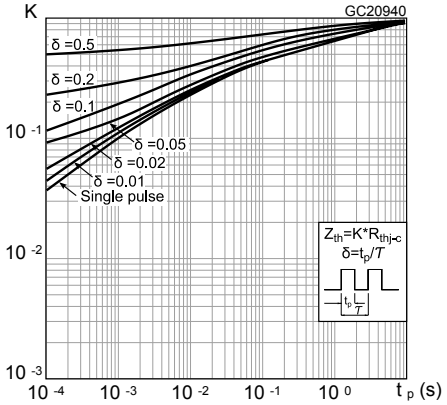


Figure 5. Output characterisics

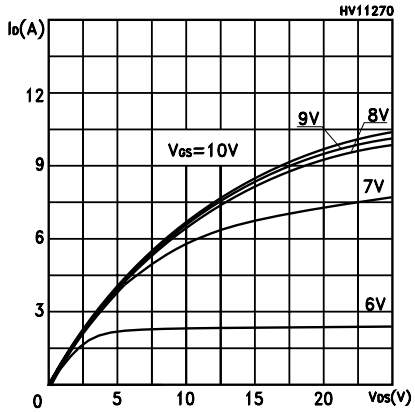


Figure 6. Transfer characteristics

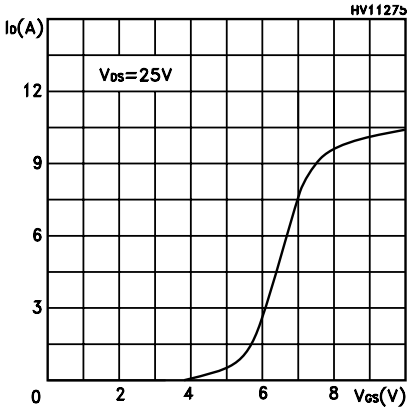


Figure 7. Static drain-source on resistance

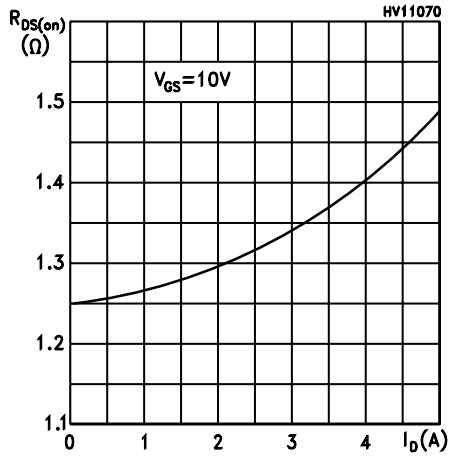


Figure 8. Gate charge vs gate-source voltage

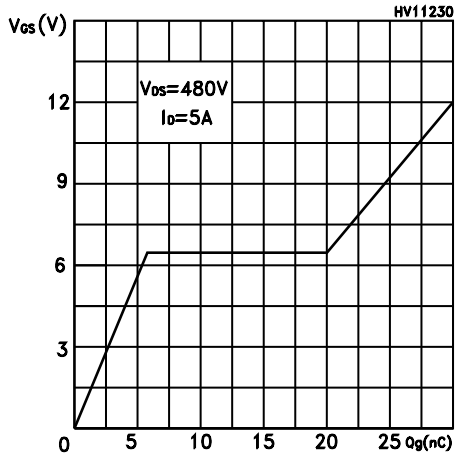


Figure 9. Capacitance variations

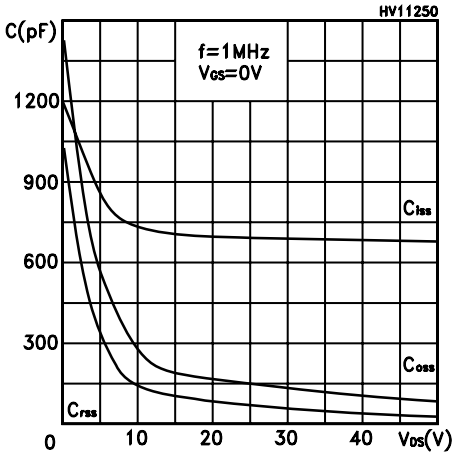


Figure 10. Normalized gate threshold voltage vs temperature

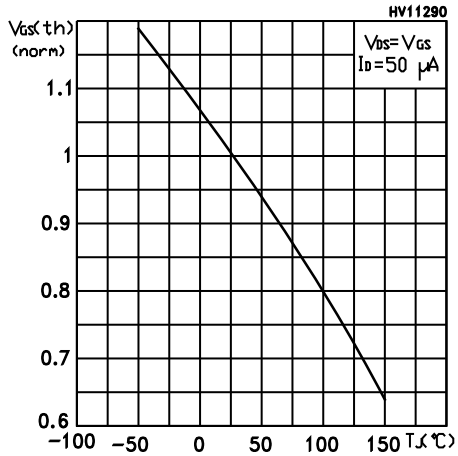


Figure 11. Normalized on resistance vs temperature

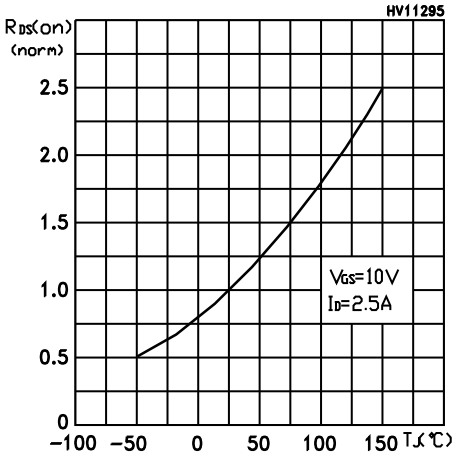


Figure 12. Source-drain diode forward characteristic

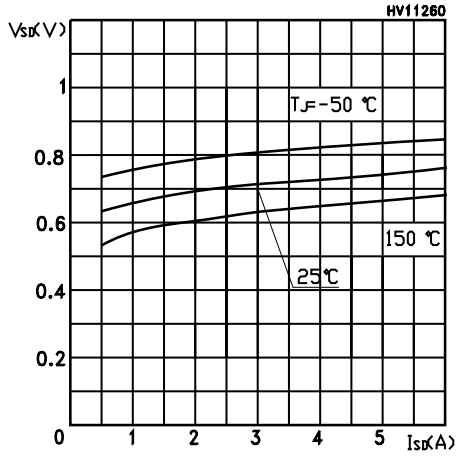


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

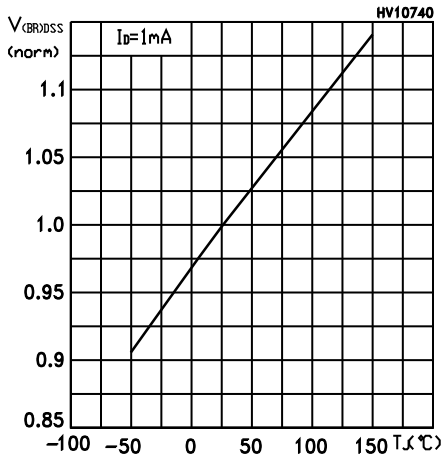
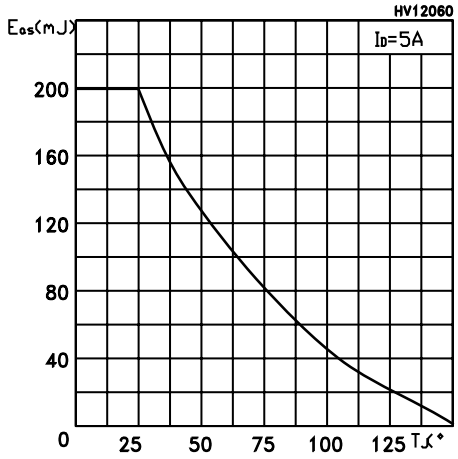


Figure 14. Maximum avalanche energy vs temperature



3 Test circuits

Figure 15. Test circuit for resistive load switching times

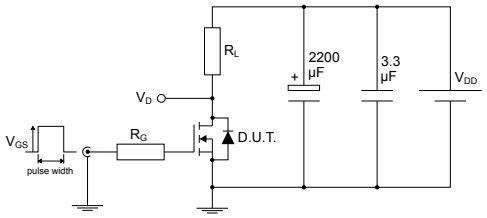


Figure 16. Test circuit for gate charge behavior

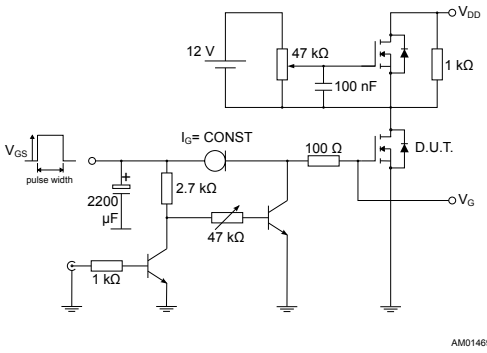


Figure 17. Test circuit for inductive load switching and diode recovery times

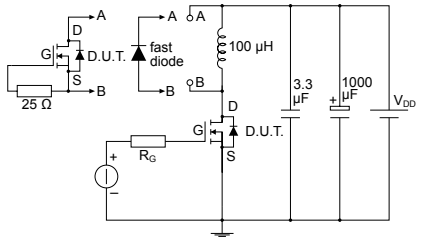


Figure 18. Unclamped inductive load test circuit

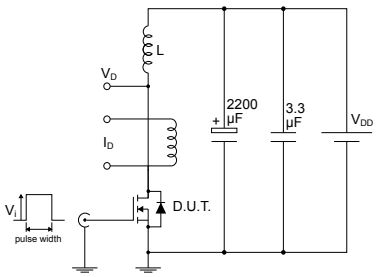


Figure 19. Unclamped inductive waveform

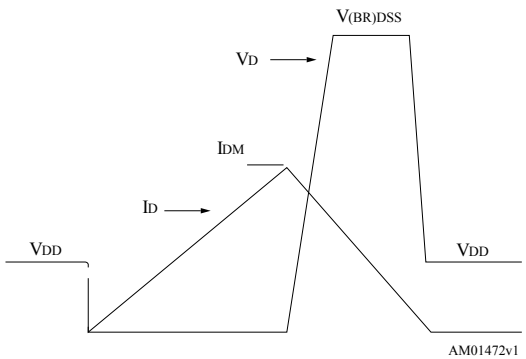
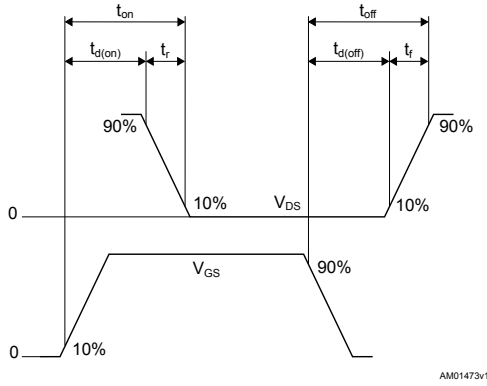


Figure 20. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 21. **DPAK (TO-252) type A2 package outline**

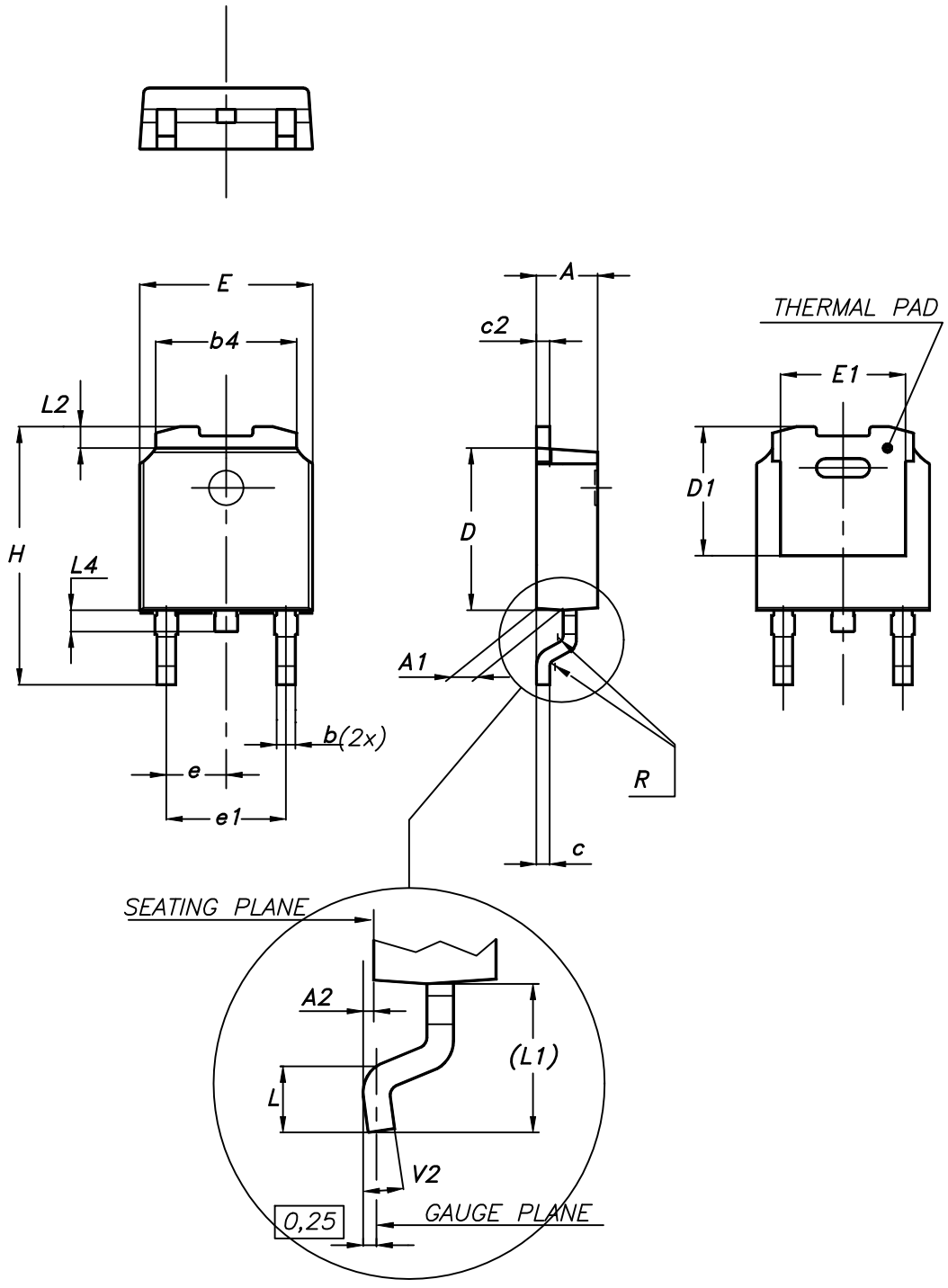


Table 9. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 22. **DPAK (TO-252) type C2 package outline**

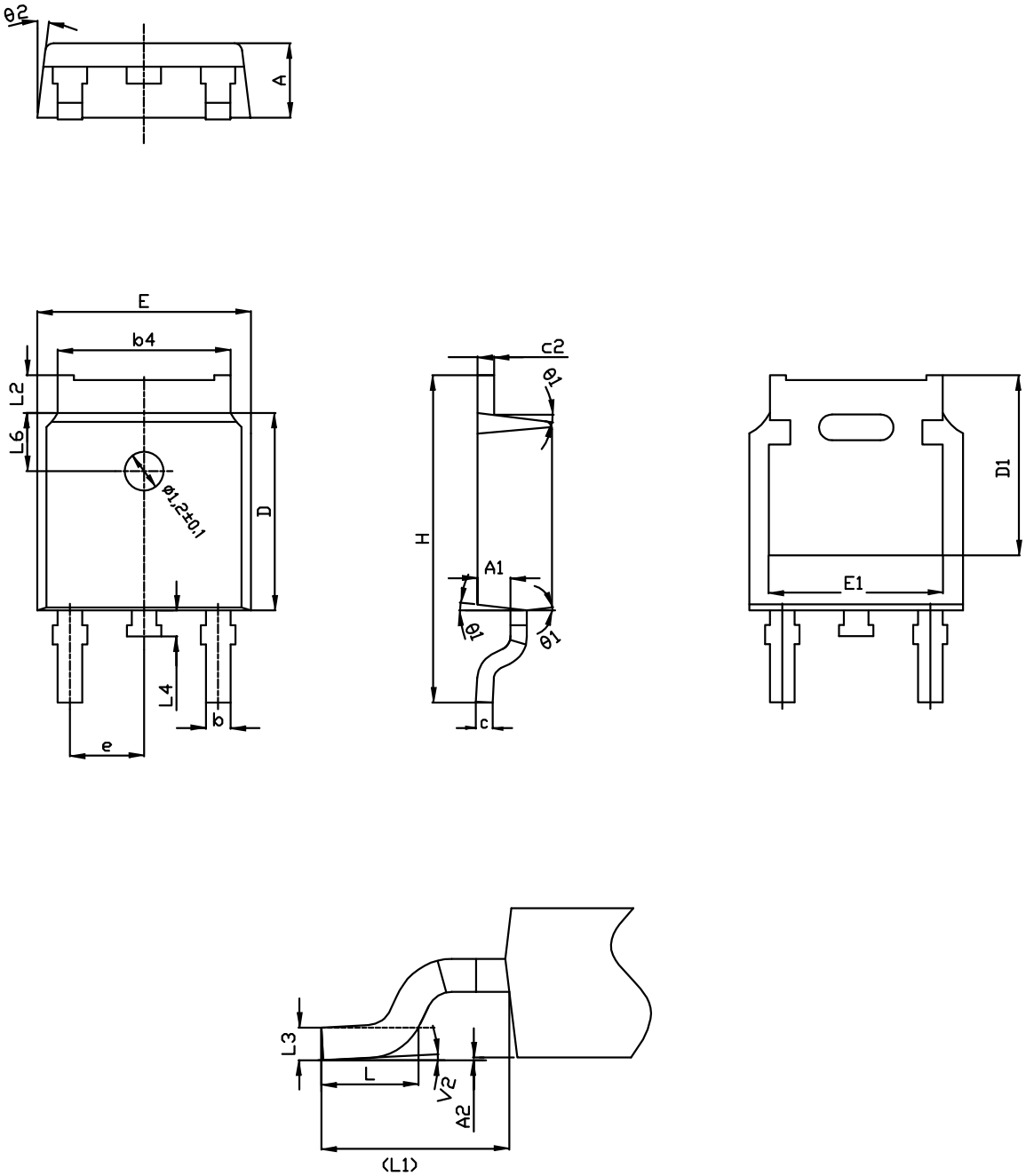


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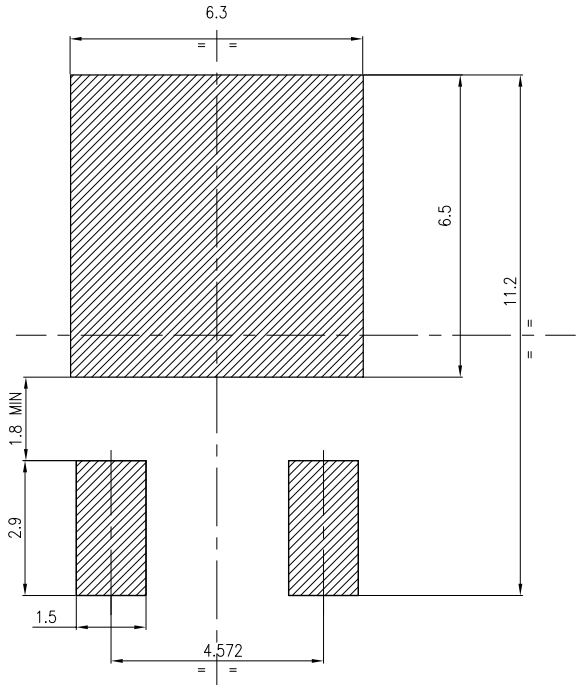
Table 10. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 23. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.3 DPAK (TO-252) packing information

Figure 24. **DPAK (TO-252) tape outline**

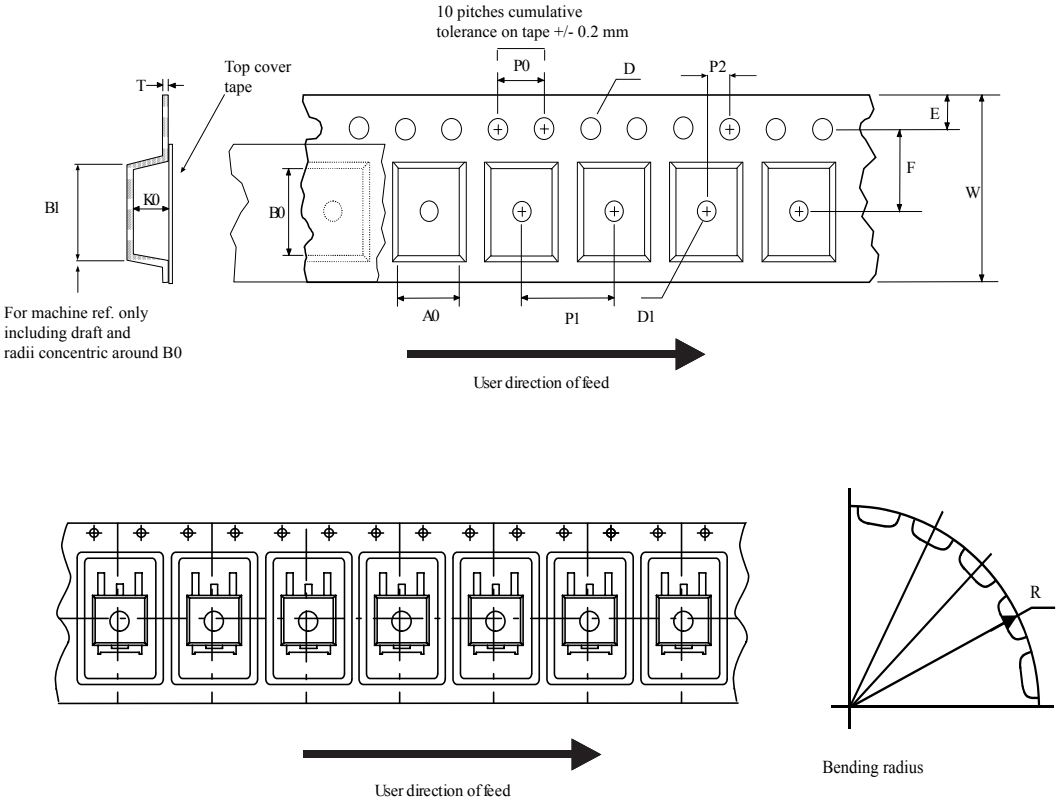


Figure 25. **DPAK (TO-252) reel outline**

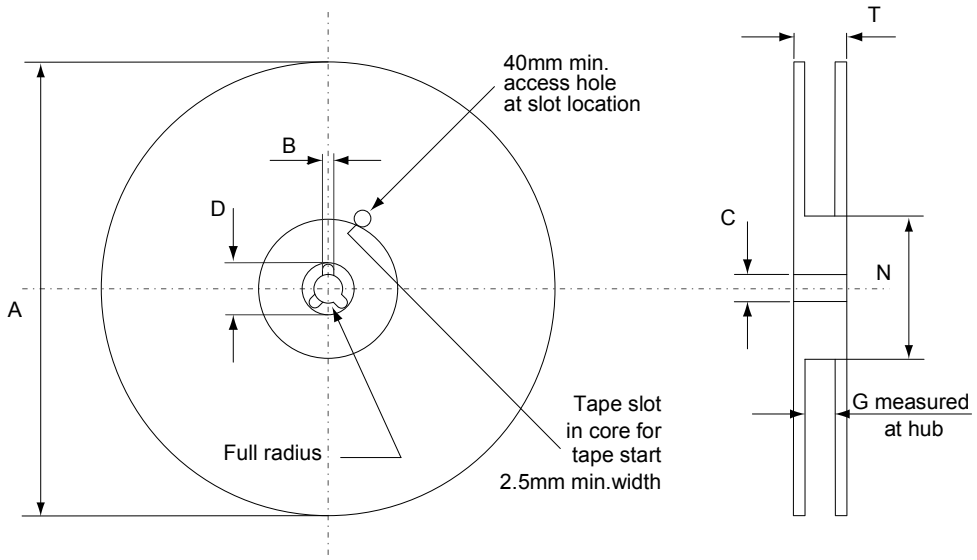


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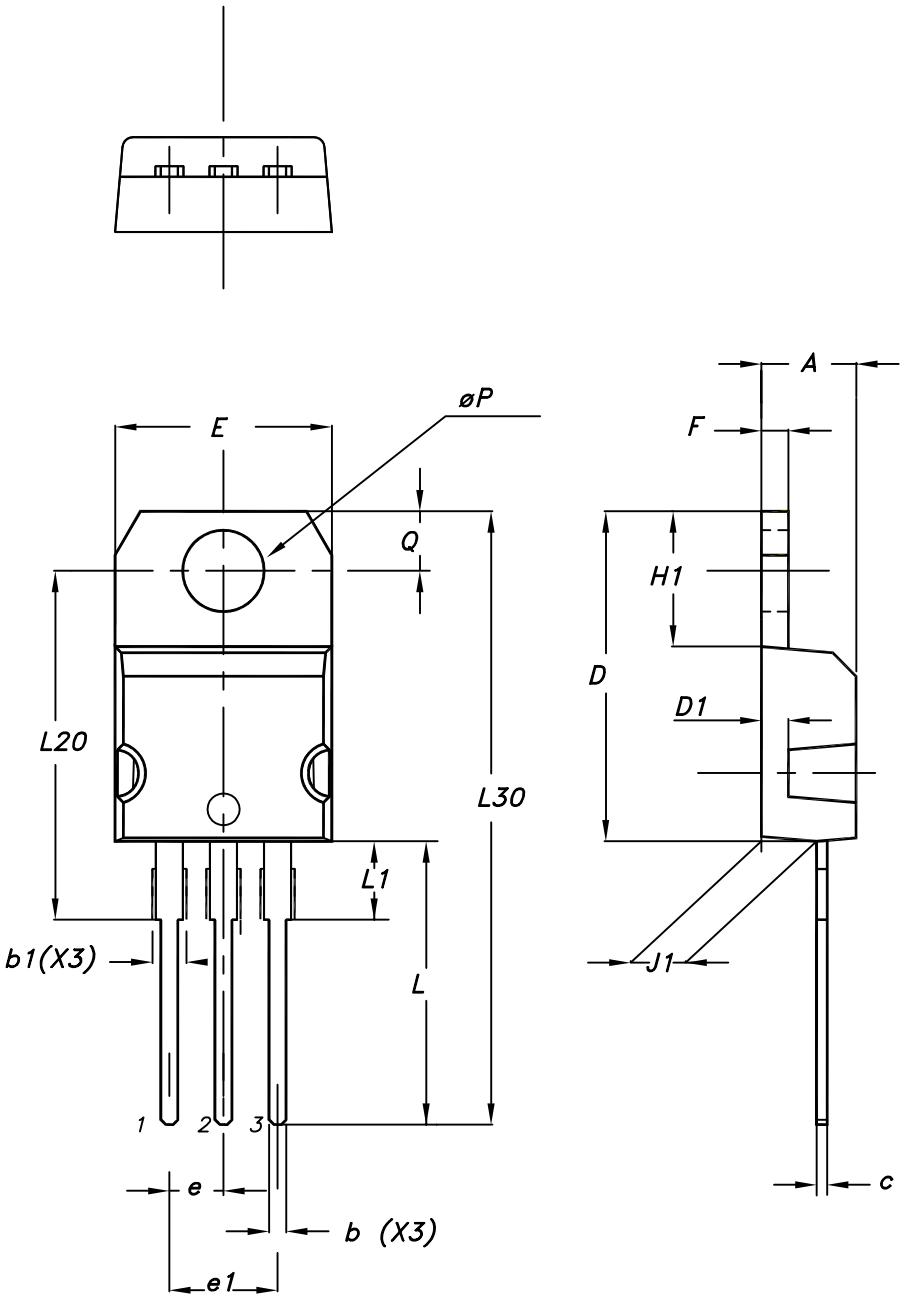
Table 11. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 26. **TO-220 type A package outline**



0015988_typeA_Rev_21

Table 12. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.5 TO-220FP package information

Figure 27. **TO-220FP package outline**

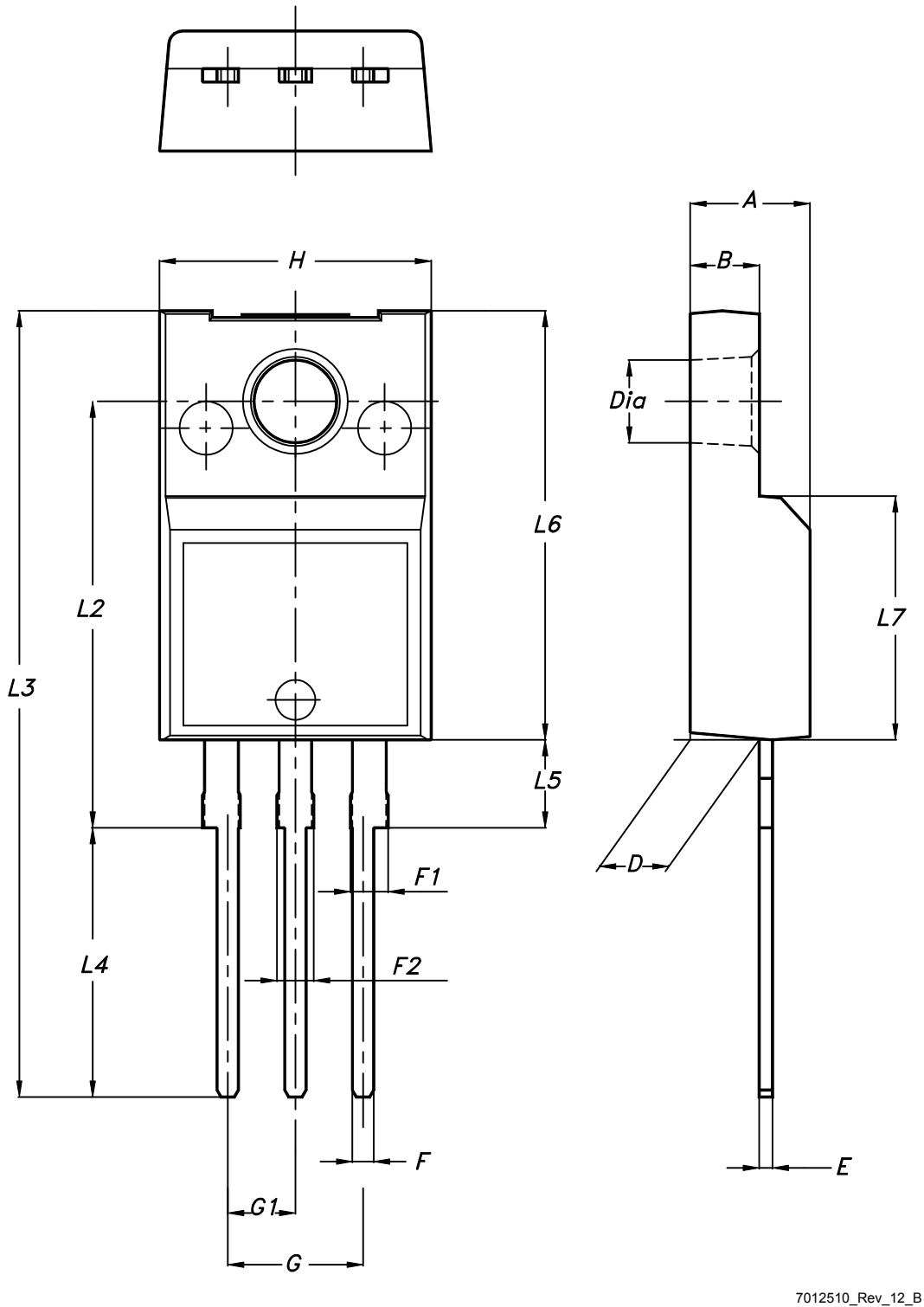


Table 13. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Ordering information

Table 14. **Order codes**

Order code	Marking	Package	Packing
STD5NK60ZT4	D5NK60Z	DPAK	Tape and reel
STP5NK60Z	P5NK60Z	TO-220	Tube
STP5NK60ZFP	P5NK60ZFP	TO-220FP	Tube

Revision history

Table 15. **Document revision history**

Date	Version	Changes
05-Apr-2005	1	First issue
29-Apr-2005	2	Modified value in Table 7.
06-Sep-2005	3	Inserted Ecopack indication
14-Oct-2005	4	Modified value on Table 1
28-Oct-2005	5	Tape & Reel info added
14-Nov-2005	6	Modified value on Table 6
15-Dec-2005	7	Various corrections
22-Aug-2018	8	Removed maturity status indication from cover page. The document status is production data. Updated Section 4 Package information. Minor text changes.

Contents