



U74LVC1G3157

CMOS IC

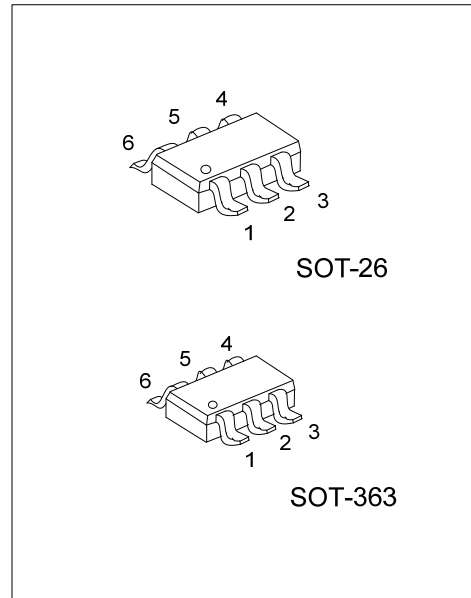
SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

DESCRIPTION

The UTC **U74LVC1G3157** is a low voltage single-pole, double-throw (SPDT) analog switch intending for use in chopping, modem, signal gating, and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

FEATURES

- * Useful in Both Analog and Digital Applications
- * Rail-to-Rail Signal Handling
- * Low ON Resistance: <math>< 10\Omega</math> on Typical @ 3.3V V_{CC}
- * Broad V_{CC} Operating Range: 1.65V to 5.5V
- * Over-Voltage Tolerance of Control Input to 6.5V

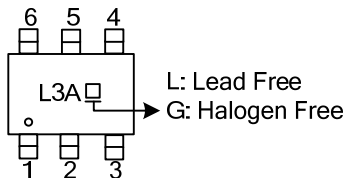


ORDERING INFORMATION

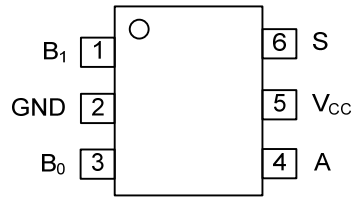
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G3157L-AG6-R	U74LVC1G3157G-AG6-R	SOT-26	Tape Reel
U74LVC1G3157L-AL6-R	U74LVC1G3157G-AL6-R	SOT-363	Tape Reel

<p>U74LVC1G3157G-AG6-R</p> <pre> (1) Packing Type (2) Package Type (3) Green Package </pre>	<p>(1) R: Tape Reel</p> <p>(2) AG6: SOT-26, AL6: SOT-363</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

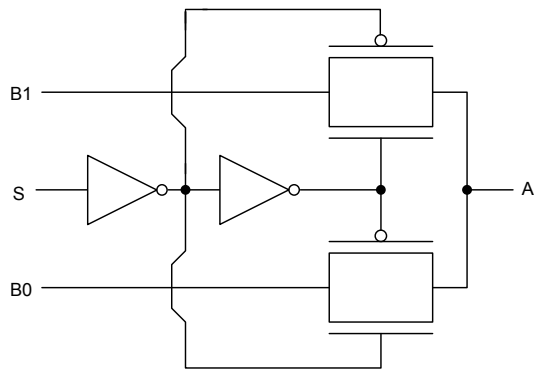


■ FUNCTION TABLE

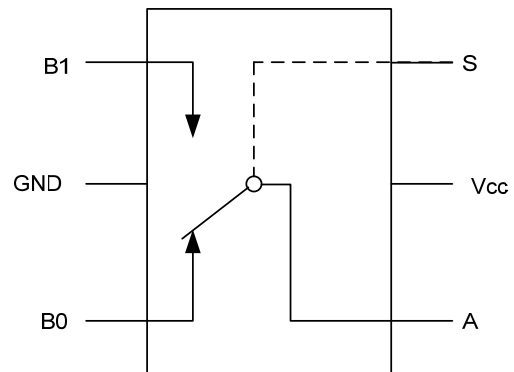
INPUT(S)	OUTPUT(Y)
L	B0 Connected to A
H	B1 Connected to A

H=High Level
L=Low Level

■ LOGIC DIAGRAM



Logic Symbol



Analog Symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +6.5	V
Switch Voltage	V_S	-0.5 ~ $V_{CC}+0.5$	V
Input Voltage	V_{IN}	-0.5 ~ +6.5	V
V_{CC} or GND Current	I_{CC}	±100	mA
Continuous Output Current	I_{OUT}	128	mA
Input Clamp Current ($V_{IN}<0V$)	I_{IK}	-50	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	°C
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-26	230	°C/W
	SOT-363	350	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		1.65		5.5	V
Control Input Voltage	V_{IN}	(Note)	0		V_{CC}	V
Switch Input Voltage	V_{IN}	(Note)	0		V_{CC}	V
Output Voltage	V_{OUT}	(Note)	0		V_{CC}	V
High-level Input Voltage	V_{IH}	$V_{CC}=1.65V$ to $1.95V$	$0.75 \times V_{CC}$			V
		$V_{CC}=2.3V$ to $5.5V$	$0.7 \times V_{CC}$			V
Low-level Input Voltage	V_{IL}	$V_{CC}=1.65V$ to $1.95V$			$0.25 \times V_{CC}$	V
		$V_{CC}=2.3V$ to $5.5V$			$0.3 \times V_{CC}$	V
Input Rise or Fall Times	$\frac{\Delta t}{\Delta V}$	Control Input $V_{CC}=2.3V \sim 3.6V$			10	ns/V
		Control Input $V_{CC}=4.5V \sim 5.5V$			5	ns/V

Note: Control input must be held HIGH or LOW; it must not float.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch On Resistance	R_{ON}	$V_{CC}=4.5V, V_{IN}=0V, I_{OUT}=30mA$		3.0	7.0	Ω
		$V_{CC}=4.5V, V_{IN}=2.4V, I_{OUT}=-30mA$		5.0	12.0	Ω
		$V_{CC}=4.5V, V_{IN}=4.5V, I_{OUT}=-30mA$		7.0	15.0	Ω
		$V_{CC}=3V, V_{IN}=0V, I_{OUT}=24mA$		4.0	9.0	Ω
		$V_{CC}=3V, V_{IN}=3V, I_{OUT}=-24mA$		10.0	20.0	Ω
		$V_{CC}=2.3V, V_{IN}=0V, I_{OUT}=8mA$		5.0	12.0	Ω
		$V_{CC}=2.3V, V_{IN}=2.3V, I_{OUT}=-8mA$		13.0	30.0	Ω
		$V_{CC}=1.65V, V_{IN}=0V, I_{OUT}=4mA$		6.5	20.0	Ω
On Resistance Match Between Channel	ΔR_{ON}	$V_{CC}=1.65V, V_{IN}=1.65V, I_{OUT}=-4mA$		17.0	50.0	Ω
		$V_{CC}=4.5V, V_{BN}=3.15V, I_A=-30mA$		0.15		Ω
		$V_{CC}=3V, V_{BN}=2.1V, I_A=-24mA$		0.2		Ω
		$V_{CC}=2.3V, V_{BN}=1.6V, I_A=-8mA$		0.5		Ω
		$V_{CC}=1.65V, V_{BN}=1.15V, I_A=-4mA$		0.5		Ω
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0$ to $5.5V, 0 \leq V_{IN} \leq 5.5V$			±0.1	μA
Off State Leakage Current	I_{OFF}	$V_{CC}=1.65$ to $5.5V, 0 \leq A, B \leq V_{CC}$			±0.1	μA
Quiescent Supply Current	I_Q	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			1	μA
Analog Signal Range		$V_{CC}=V_{CC}, V_{IN}=V_{CC}$ or GND	0		V_{CC}	V

■ SWITCHING CHARACTERISTICS (see TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Bus to Bus(Note)	t_{PLH} t_{PHL}	$C_L=50\text{ pF}$, $R_L=500\Omega$	$V_{CC}=1.65 \sim 1.95\text{V}$		3.5	ns
			$V_{CC}=2.3 \sim 2.7\text{V}$		1.2	ns
			$V_{CC}=3.0 \sim 3.6\text{V}$		0.8	ns
			$V_{CC}=4.5 \sim 5.5\text{V}$		0.3	ns
Output Enable Time Turn-On Time (A to B _N)	t_{PZL} t_{PZH}	$C_L=50\text{ pF}$, $R_L=500\Omega$	$V_{CC}=1.65 \sim 1.95\text{V}$	7.0	23.0	ns
			$V_{CC}=2.3 \sim 2.7\text{V}$	3.5	13.0	ns
			$V_{CC}=3.0 \sim 3.6\text{V}$	2.5	6.9	ns
			$V_{CC}=4.5 \sim 5.5\text{V}$	1.7	5.2	ns
Output Enable Time Turn-Off Time (A to B _N)	t_{PHZ} t_{PLZ}	$C_L=50\text{ pF}$, $R_L=500\Omega$	$V_{CC}=1.65 \sim 1.95\text{V}$	3.0	12.5	ns
			$V_{CC}=2.3 \sim 2.7\text{V}$	2.0	7.0	ns
			$V_{CC}=3.0 \sim 3.6\text{V}$	1.2	5.0	ns
			$V_{CC}=4.5 \sim 5.5\text{V}$	0.8	3.5	ns

Note: Guaranteed by design.

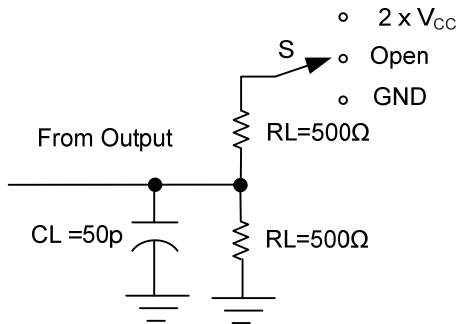
■ DYNAMIC CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bandwidth	BW	$R_L=50\Omega$, Switch ON	$V_{CC}=1.8\text{V}$		220	MHz
			$V_{CC}=2.3\text{V}$		220	MHz
			$V_{CC}=3.0\text{V}$,		220	MHz
			$V_{CC}=4.5\text{V}$		220	MHz
OFF Isolation	O_{ISO}	$R_L=50\Omega$, $f=10\text{MHz}$, Switch OFF	$V_{CC}=1.8\text{V}$,		-60	dB
			$V_{CC}=2.3\text{V}$		-65	dB
			$V_{CC}=3.0\text{V}$		-65	dB
			$V_{CC}=4.5\text{V}$		-65	dB
Crosstalk	X_{TALK}	$R_L=50\Omega$, $f=10\text{MHz}$, Switch ON	$V_{CC}=1.8\text{V}$		-66	dB
			$V_{CC}=2.3\text{V}$		-66	dB
			$V_{CC}=3.0\text{V}$		-66	dB
			$V_{CC}=4.5\text{V}$		-66	dB
Total Harmonic Distortion	THD	$R_L=600\Omega$, $C_L=50\text{pF}$, $f=600\text{Hz} \sim 20\text{KHz}$	$V_{CC}=1.8\text{V}$		0.015	%
			$V_{CC}=2.3\text{V}$		0.025	%
			$V_{CC}=3.0\text{V}$		0.015	%
			$V_{CC}=4.5\text{V}$		0.01	%

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$)

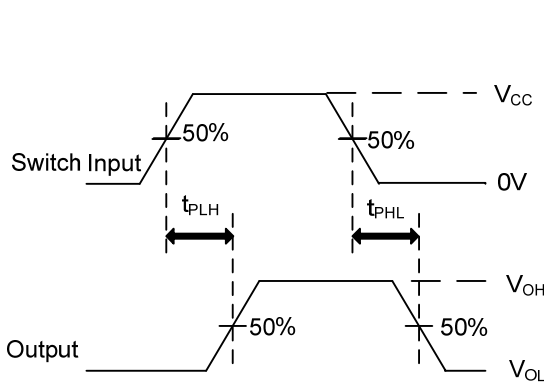
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Control Pin Input Capacitance	C_{IN}	$V_{CC}=0\text{V}$		2.3		pF
B Port Off Capacitance	C_{IO-B}	$V_{CC}=5.0\text{V}$		6.5		pF
A Port Capacitance When Switch Is Enabled	C_{IOA-ON}	$V_{CC}=5.0\text{V}$		18.5		pF

■ TEST CIRCUIT AND WAVEFORMS

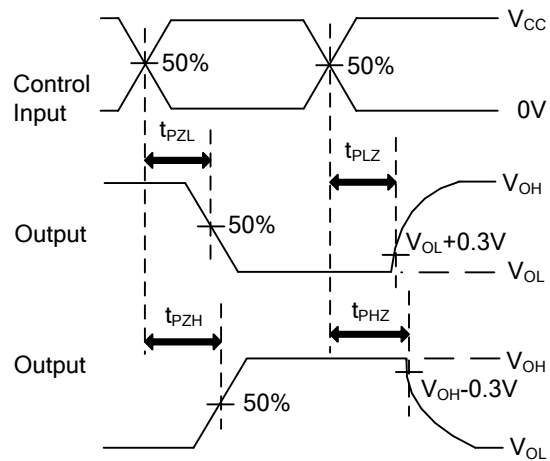


TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

Note: C_L includes probe and jig capacitance.
 $PRR \leq 1\text{MHz}$, $Z_0 = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ns}$.

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