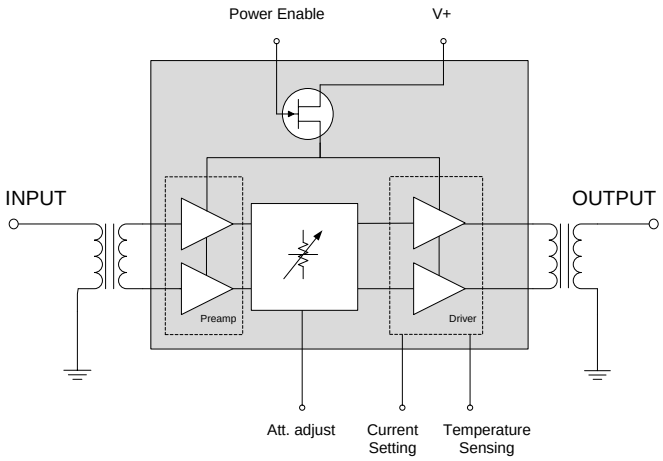
RFAM3620

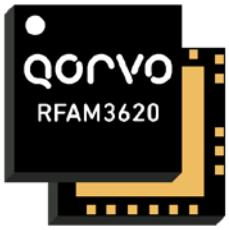
CATV Edge QAM MCM 1218MHz 36dB

Product Description

The RFAM3620 is an Integrated Edge QAM Amplifier Module. The part employs GaAs pHEMT die, GaAs MESFET die, a 20 dB range variable attenuator and a power enable feature, has high output capability, and is operated from 45 MHz to 1218 MHz. It provides excellent linearity and superior return loss performance with low noise and optimal reliability.

Functional Block Diagram





21 pin, 11.0 mm x 11.0 mm x 1.375 mm package

Product Features

- Excellent Linearity
- Extremely High Output Capability
- Voltage Controlled Attenuator
- Power Enable Feature
- Extremely Low Distortion
- Optimal Reliability
- Low Noise
- Unconditionally Stable Under all Terminations
- 36 dB Min Gain at 1218 MHz
- 510 mA Typical at 12 VDC
- Temperature sensing feature

Applications

- Head End Equipment
- 45 – 1218 MHz Downstream Edge QAM RF Modulators

Ordering Information

Part No.	Description
RFAM3620SB	Sample bag 5 pcs
RFAM3620SQ	Sample bag 25 pcs
RFAM3620SR	7” Reel with 100 pcs
RFAM3620TR7	7” Reel with 250 pcs
RFAM3620TR13	13” Reel with 750 pcs
RFAM3620PCBA-410	Fully assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
DC Supply over-voltage (5 minutes)	+14 V
Storage Temperature	−40 to 100 °C
Operating Mounting Base Temperature	−30 to 100 °C
Moisture Sensitivity Level IPC/JEDEC J-STD-20	MSL 3 @ 260 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Electrical Specifications – part 1

Parameter	Conditions (V+=12V, TMB=30°C, ZS=ZL=75Ω, ATT=0dB)	Min	Typ	Max	Units
Operational Frequency Range	–	45	–	1218	MHz
Current (I_{DD})	–		510	550	mA
Gain	f_o = 45 MHz		35.5		dB
Gain	f_o = 1218 MHz	36.0	37.0	38.0	
Gain Slope	45 to 1218 MHz [1]	0.5	1.0	2.5	
Gain Flatness	45 to 1218 MHz		0.5	1.0	
Input Return Loss	f_o= 45 to 160 MHz	18		–	dB
	f_o= 160 to 1003 MHz	15		–	
	f_o= 1003 to 1218 MHz	15		–	
Output Return Loss	f_o= 45 to 160 MHz	18		–	dB
	f_o= 160 to 1003 MHz	15		–	
	f_o= 1003 to 1218 MHz	15		–	
Noise Figure	f_o= 50 to 1218 MHz	–	3.0	5.0	dB
Attenuator Range	Attenuator Voltage 0V to 12V	0 - 20			dB
Power Enable/Disable	Logic high (3.3V) applied to power enable pin [2]		Amp enabled		
Power Enable/Disable	Logic low (0V) applied to power enable pin [3]		Amp disabled		
Thermal Resistance	Junction to Mounting Base		6.5		K/W

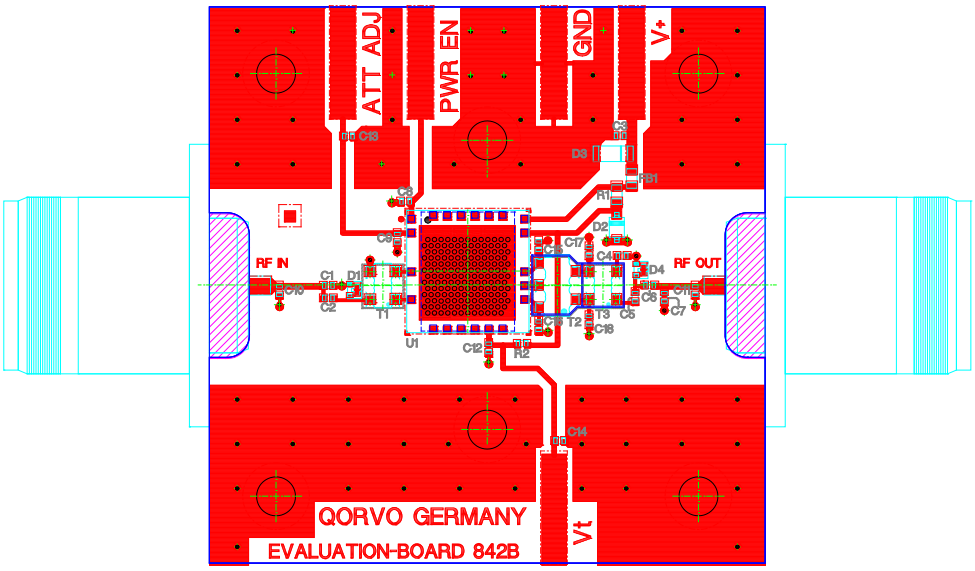
Electrical Specifications – part 2

Parameter	Conditions (V+=12V, TMB=30°C, ZS=ZL=75Ω, ATT=0dB)	Min	Typ	Max	Units
Adjacent Channel Power Ratio (ACPR); N=4 contiguous 256QAM channels	Channel Power = 58 dBmV; Adjacent channel up to 750 kHz from channel block edge, f= 50 to 1000 MHz			-58	dBc
	Channel Power = 58 dBmV; Adjacent channel (750 kHz from channel block edge to 6 MHz from channel block edge), f= 50 to 1000 MHz			-60	dBc
	Channel Power = 58 dBmV; Next-adjacent channel (6 MHz from channel block edge to 12 MHz from channel block edge), f= 50 to 1000 MHz			-63	dBc
	Channel Power = 58 dBmV; Third-adjacent channel (12 MHz from channel block edge to 18 MHz from channel block edge), f= 50 to 1000 MHz			-65	dBc
2nd Order Harmonic (HD2); N=1 256QAM channel	Channel Power = 66 dBmV; In each of 2N contiguous 6 MHz channels coinciding with 2nd harmonic components (up to 1000MHz)			-63	dBc
3rd Order Harmonic (HD3); N=1 256QAM channel	Channel Power = 66 dBmV; In each of 3N contiguous 6 MHz channels coinciding with 3rd harmonic components (up to 1000MHz)			-63	dBc
CTB	Vo=48 dBmV, flat, 79 analog channels plus 75 digital channels (-6dB offset) [4]		-73		dBc
XMOD			-70		dBc
CSO			-75		dBc
CIN			64		dB

1. The slope is defined as the difference between the gain at the start frequency and the gain at the stop frequency.
2. Logic high is defined as power enable voltage >2V
3. Logic low is defined as power enable voltage <0.4V
4. 79 analog channels, NTSC frequency raster: 55.25MHz to 547.25MHz, +48dBmV flat output level, plus 75 digital channels, -6dB offset relative to the equivalent analog carrier.

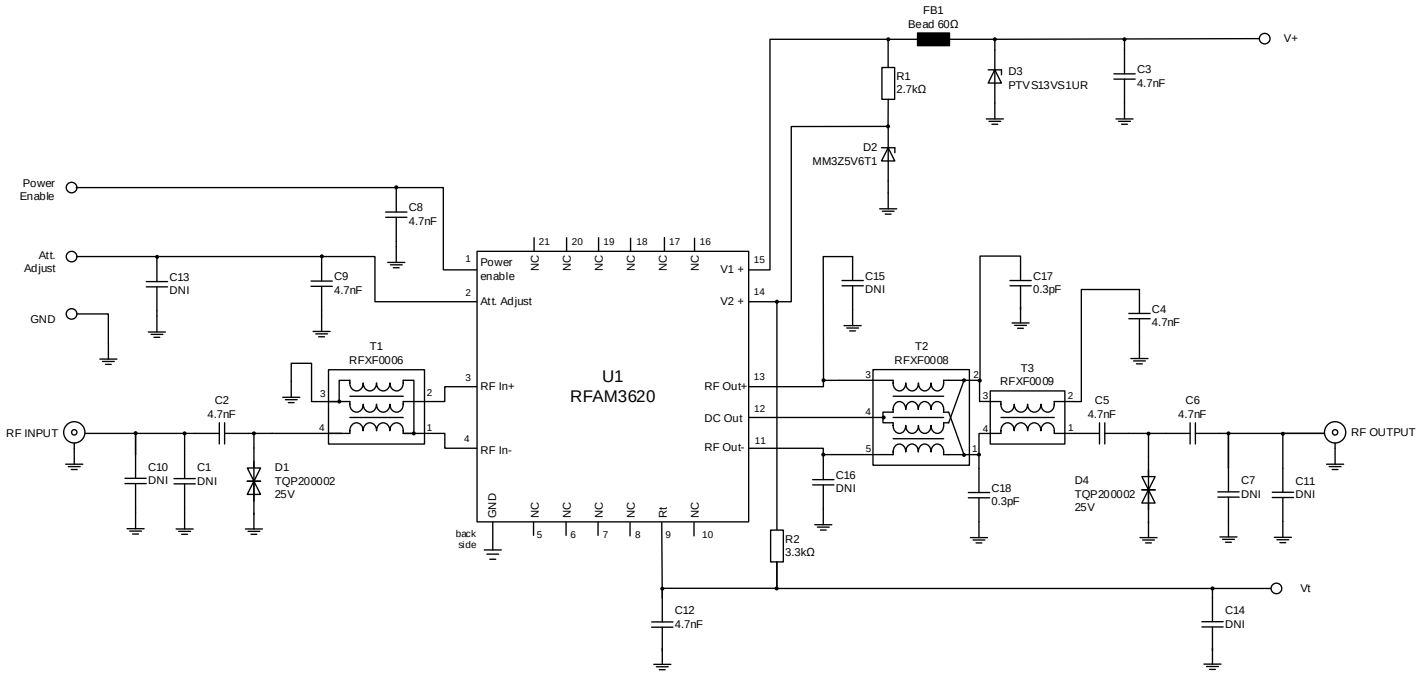
Composite Second Order (CSO) - The CSO parameter (both sum and difference products) is defined by ANSI/SCTE 6. Composite Triple Beat (CTB) The CTB parameter is defined by ANSI/SCTE 6. Cross Modulation (XMOD) - Cross modulation (XMOD) is measured at baseband (selective voltmeter method), referenced to 100% modulation of the carrier being tested. Carrier to Intermodulation Noise (CIN) - The CIN parameter is defined by ANSI/SCTE 17 (Test procedure for carrier to noise).

Evaluation Board Assembly Drawing



Note:
The ground plane of the RFAM3620 module should be soldered onto a board equipped with as many thermal vias as possible. Underneath this thermal via array a heat sink with thermal grease needs to be placed which is able to dissipate the complete module DC power. In any case the module backside temperature should not exceed 100°C

Evaluation Board Schematic

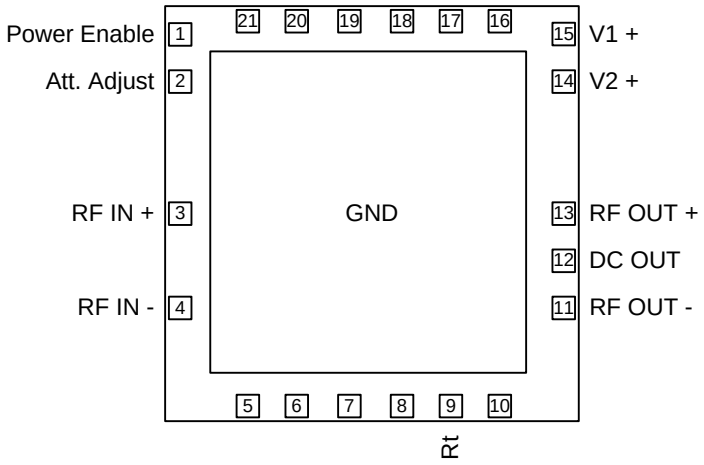


Evaluation Board Bill of Materials (BOM)

Reference Des.	Value	Description	Manuf.	Part Number
PCB	Rev B	PCB RFAM3620 – EVB 842B	Qorvo	
C1, C7, C10, C11, C15, C16	DNI	optional to improve matching in application		
C2, C3, C4, C5, C6, C8, C9, C12	4.7 nF	CAP, 0402, 10%, 50V, X7R		
C13, C14	DNI	optional blocking CAP		
C17, C18	0.3 pF	CAP, 0402, ±0.1pF, 50V, C0G		
R1	2.7 kΩ	RES, 0402, 1%, TK100		
R2	3.3 kΩ	RES, 0402, 1%, TK100		
FB1	60 Ω	Impedance Bead, 0603, 60Ω @ 100MHz, LM, DCR 0.10 Ω, 800mA	TaiyoYuden	BK 1608 HS 600
D1, D4	25 V	ESD Protection Diode TQP200002, TSLP3	Qorvo/ Unisem	TQP200002
D2	5.6 V	Zener Diode MM3Z5V6T1G, SOD-323	ON Semi	MM3Z5V6T1G
D3	13 V	Diode, TVS, PTVS13VS1UR, SOD123W	NXP	PTVS13VS1UR
T1		RFXF0006	Qorvo	
T2		RFXF0008	Qorvo	
T3		RFXF0009	Qorvo	
U1	DUT	RFAM3620	Qorvo	

Notes:

Pin Configuration



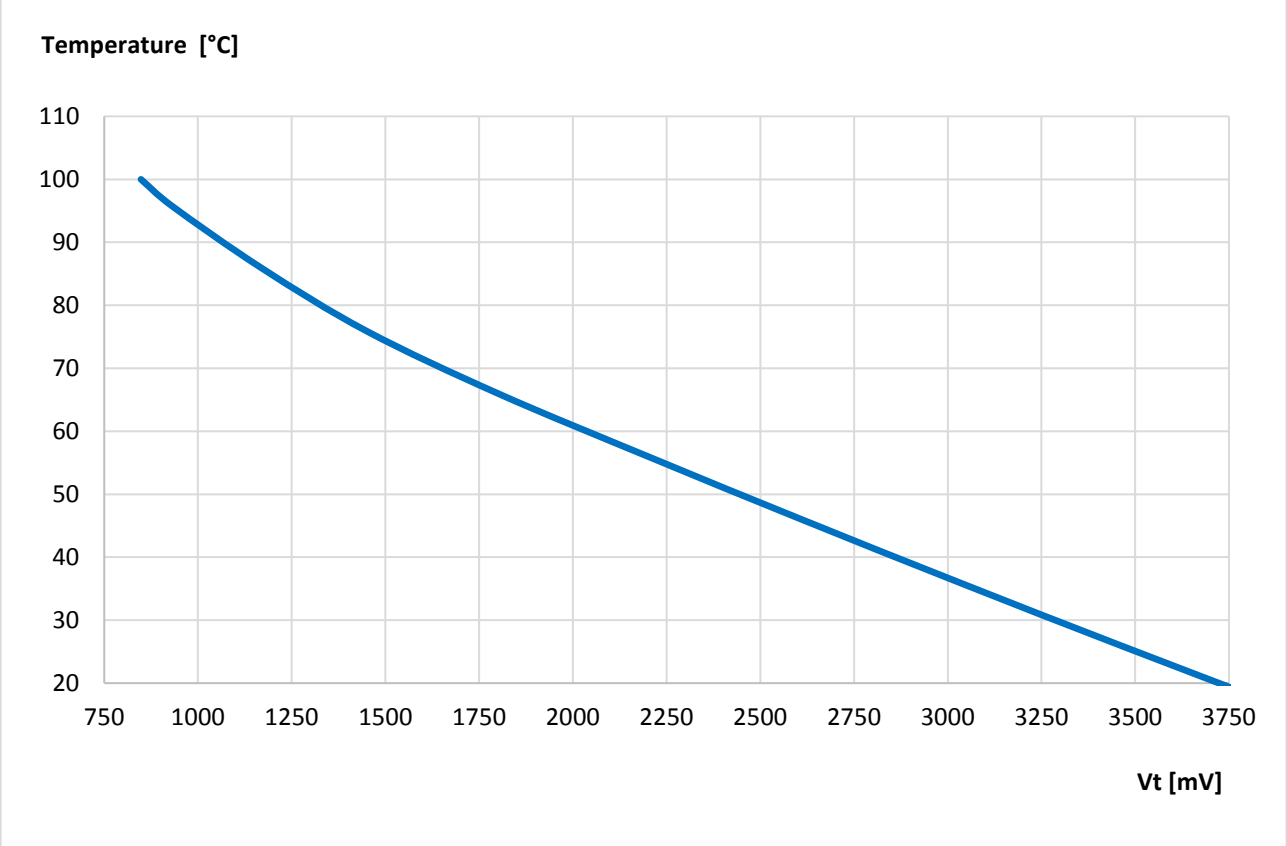
Pin Description

Pin No.	Label	Description
1	Power Enable	Logic Level (3.3V) Power Enable Control
2	Att. Adjust	Voltage Adjustable Attenuator
3	RF IN (+)	RF AMP Positive Input
4	RF IN (-)	RF AMP Negative Input
5 - 8	N.C.	
9	Rt	NTC Output for Temperature Sensing
10	N.C.	
11	RF OUT (-)	RF AMP Negative Output
12	DC Out	12V Output
13	RF OUT (+)	RF AMP Positive Output
14	V2 +	Supply Voltage 5.6V
15	V1 +	Supply Voltage 12V
16 - 21	N.C.	

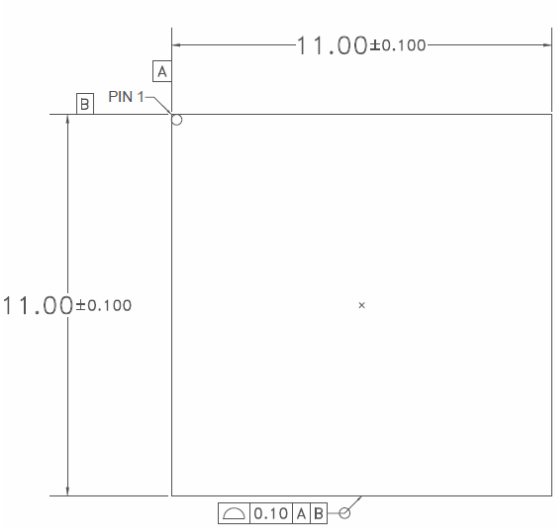
RFAM3620 Temperature Sensing Feature

The RFAM3620 provides an internal NTC resistor for temperature sensing. This resistor is located right next to the output transistor stage. Within the application circuit the NTC is part of a voltage divider. The output voltage of the voltage divider (Vt) can be correlated to the module backside temperature.

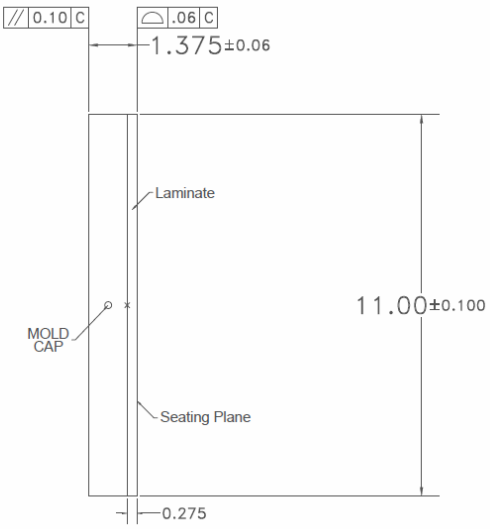
Module Backside Temperature versus Vt (typical values)



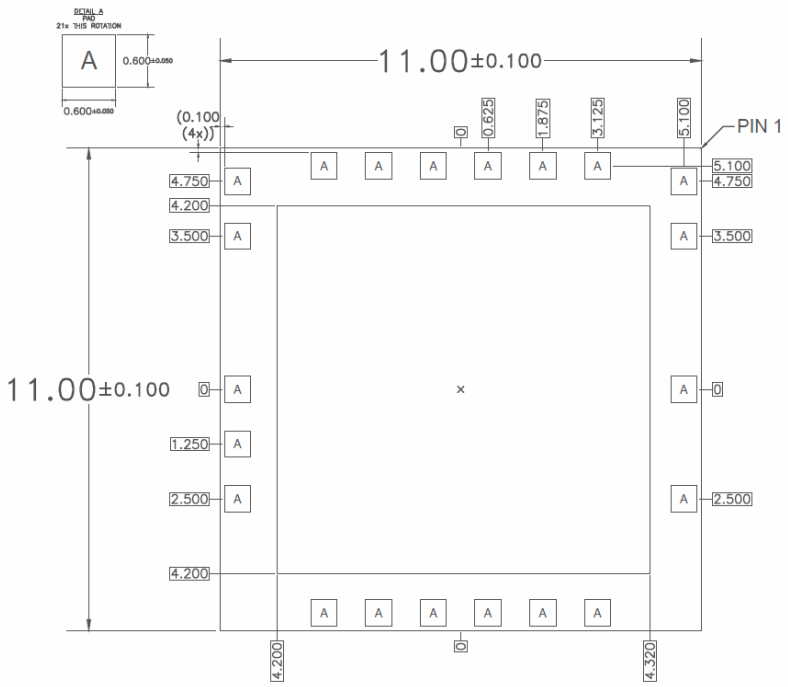
Package Outline Drawing (Dimensions in millimeters)



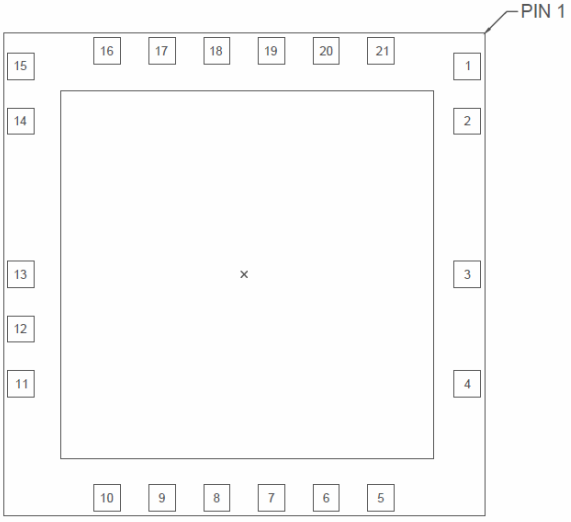
TOP VIEW



SIDE VIEW



BOTTOM VIEW

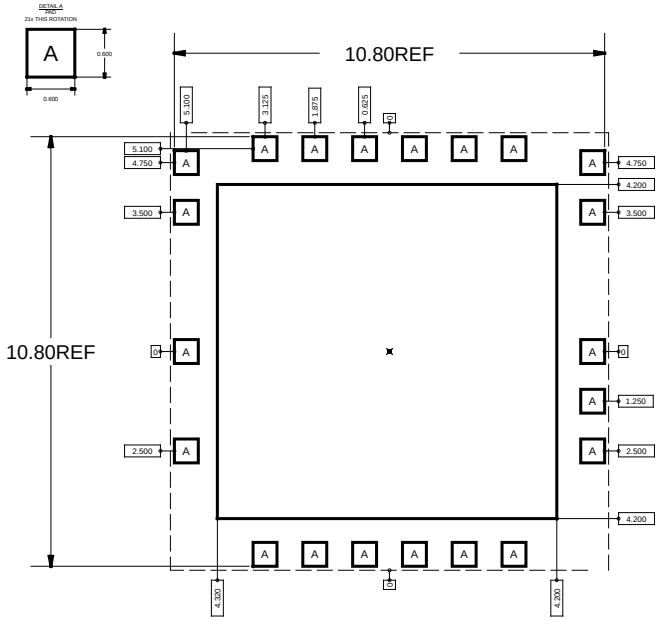


BOTTOM PINS VIEW

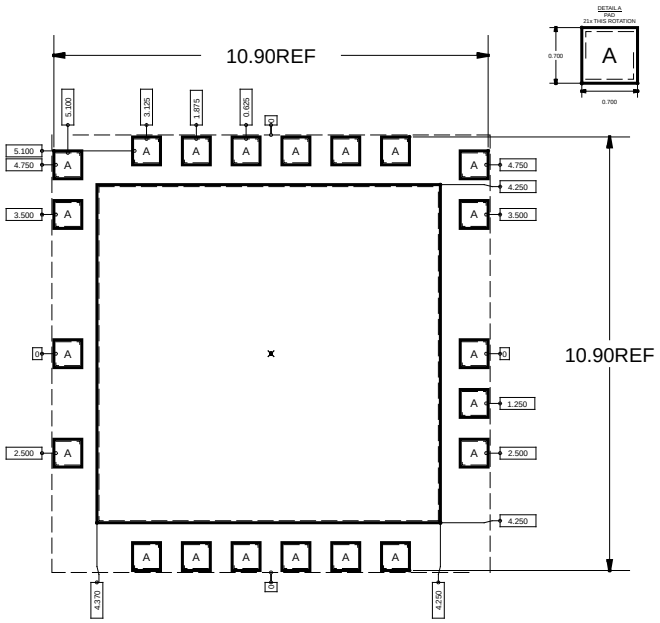
Notes:

1. Dimension and tolerance formats conform to ASME Y14.5M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Metal Land Pattern (Dimensions in millimeters)



RECOMMENDED LAND PATTERN



RECOMMENDED LAND PATTERN MASK

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 2 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
5. Place mounting screws near the part to fasten a back side heat sink.
6. Do not apply solder mask to the back side of the PC board in the heat sink contact region.
7. Ensure that the backside via region makes good physical contact with the heat sink.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	ANSI/ESD/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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