CY7B951

Local Area Network ATM Transceiver

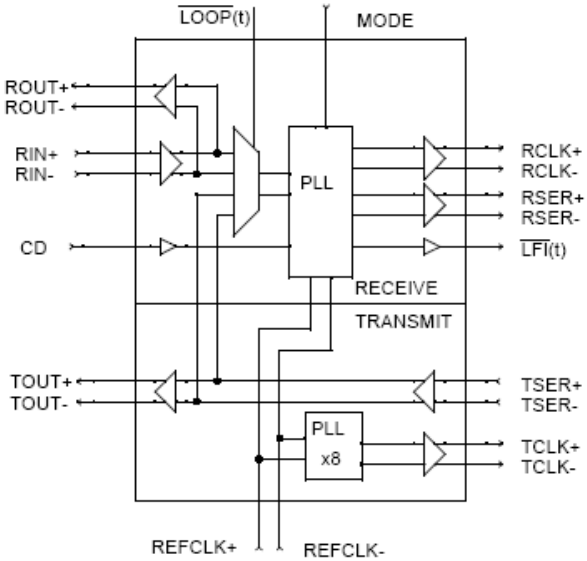
Features

- SONET/SDH and ATM Compatible
- Compatible with PMC-Sierra PM5345 SUNI™
- Clock and data recovery from 51.84- or 155.52-MHz datastream
- 155.52-MHz clock multiplication from 19.44-MHz source
- 51.84-MHz clock multiplication from 6.48-MHz source
- ±1% frequency agility
- Line Receiver Inputs: No external buffering required
- Differential output buffering
- • 100K ECL compatible I/O
- No output clock “drift” without data transitions
- Link Status Indication
- Loopback testing
- Single +5V supply
- 24-pin SOIC
- Compatible with fiber optic modules, coaxial cable, and twisted pair media
- No external PLL components
- Power down options to minimize power or crosstalk
- Low operating current: <65 mA
- 0.8 µ BiCMOS
- Pb-Free Packages Available

Functional Description

The Local Area Network ATM Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ or NRZI serial data stream and to provide differential data buffering for the Transmit side of the system.

Logic Block Diagram



Pin Configuration

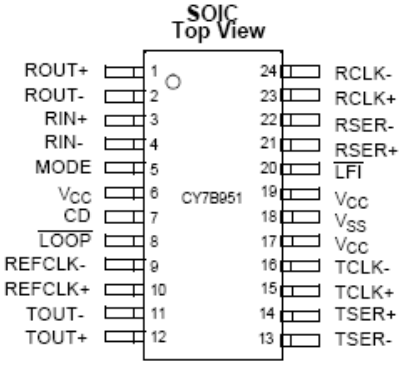
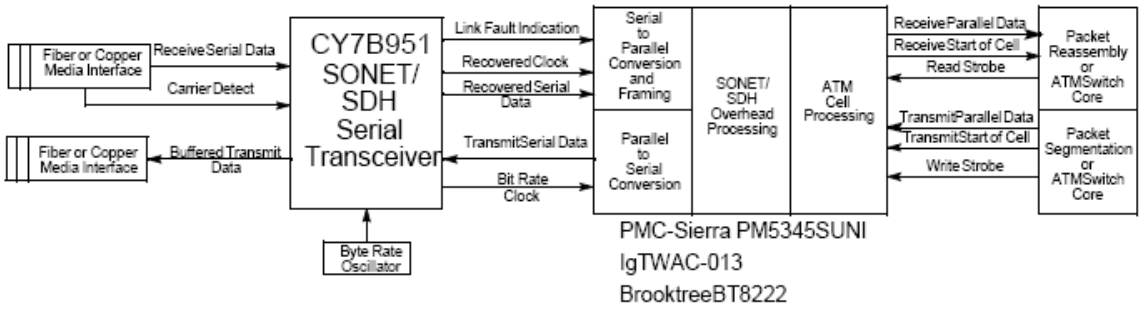


Figure 1. SONET/SDH and ATM Interface



Pin Descriptions

Name	I/O	Description
RIN±	Differential In	Receive Input. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embedded clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signaling levels. If the RIN± inputs are not being used, connect RIN+ to V_{CC} and RIN– to V_{SS}.
ROUT±	ECL Out	Receive Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the input data stream (RIN±). This output pair can be used for Receiver input data equalization in copper based systems, reducing the system impact of data-dependent jitter. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
RSER±	ECL Out	Recovered Serial Data. These ECL 100K outputs (+5V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.
RCLK±	ECL Out	Recovered Clock. These ECL 100K outputs (+5V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V_{CC} or left unconnected, the entire Receive PLL will be powered down.
CD	TTL/ECL In	Carrier Detect. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK·8 frequency. Also, the Link Fault Indicator (LFI) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data stream inputs (RIN). When the CD input is at a TTL LOW, the internal transitions detection circuitry is disabled.
LFI	TTL Out	Link Fault Indicator. This output indicates the status of the input data stream (RIN±). It is controlled by three functions: the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the LFI output will be HIGH. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the LFI output will be LOW. If CD is at a TTL LOW then the LFI output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.
TSER±	Differential In	Transmit Serial Data. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the LOOP pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the TSER± inputs are not being used, connect TSER+ to V_{CC} and TSER– to V_{SS}.
TOUT±	ECL Out	Transmit Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low-impedance copper media.
REFCLK±	Diff/TTL In	Reference Clock. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK– is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.
TCLK±	ECL Out	Transmit Clock. These ECL 100K outputs (+5V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.

Pin Descriptions (continued)

Name	I/O	Description
LOOP	TTL In	Loop Back Select. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the LOOP input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When LOOP is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.
MODE	3-Level In	Frequency Mode Select. This three-level input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH the two PLLs operate at the SONET (SDH) STS-3 (STM-1) line rate of 155.52 MHz. When this input is held LOW the two PLLs operate at the SONET STS-1 line rate of 51.84 MHz. The REFCLK± frequency in both operating modes is 1/8 the PLL operating frequency. When the MODE input is left floating or held at $V_{CC}/2$ the TSER± inputs substitute for the internal PLL VCO for use in factory testing.
V_{CC}		Power.
V_{SS}		Ground.

Description

The CY7B951 Local Area Network ATM Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52 MHz or 51.84 MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit clock, from a byte-rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system (see Figure 1).

Operating Frequency

The CY7B951 operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. The MODE input has three different functional selections. When MODE is connected to V_{CC}, the highest operating range of the device is selected. A 19.44 MHz ±1% source must drive the REFCLK input and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48 MHz ±1% source must drive the REFCLK inputs and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84 MHz ±1%. When the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test mode.

Transmit Functions

The transmit section of the CY7B951 contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK·8) to produce a PECL (Pseudo ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE pin as explained above. The CY7B951 Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter, as shown in Figure 1.

The REFCLK± input can be configured three ways. When both REFCLK+ and REFCLK– are connected to a differential 100K-compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK– or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the CY7B951 yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the receiver is to recover clock (RCLK±) and data (RSER±) from the incoming differential PECL data stream (RIN±) without the need for external buffering. These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2.5V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK·8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin as explained earlier. To ensure accurate data and clock recovery, REFCLK·8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK·8 frequency accuracy be within 20–100 ppm.

The differential input serial data (RIN±) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT±. This output pair can be used as part of the transmission line interface circuit for base line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

Carrier Detect (CD) and Link Fault Indicator ($\overline{LFI}$) Functions

The Link Fault Indicator ($\overline{LFI}$) output is a TTL-level output that indicates the status of the receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{LFI}$ is controlled by the Carrier Detect input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW ($\leq$2.5V Max.), the $\overline{LFI}$ output will transition LOW and the Receiver PLL will align itself with the REFCLK·8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data stream inputs (RIN).

In addition, the CY7B951 has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transition can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive media coupling. The CY7B951 will detect a quiet link by counting the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, $\overline{LFI}$ will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will ensure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. $\overline{LFI}$ will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 512 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW ($\leq$0.8V). When CD is pulled to a TTL LOW the $\overline{LFI}$ will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLKX8 frequency. $\overline{LFI}$ LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

Loopback Testing

The TTL level $\overline{LOOP}$ pin is used to perform loopback testing. When $\overline{LOOP}$ is asserted (held LOW) the Transmitter serial input (TSER±) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{LOOP}$ input is deasserted (held HIGH the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{LOOP}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{LOOP}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power Down Modes

There are several power down features on the CY7B951. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC}, the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the Link Fault Indicator ($\overline{LFI}$) will still reflect the state of the Carrier Detect (CD) input. This feature can be used for aggressive power management.

Applications

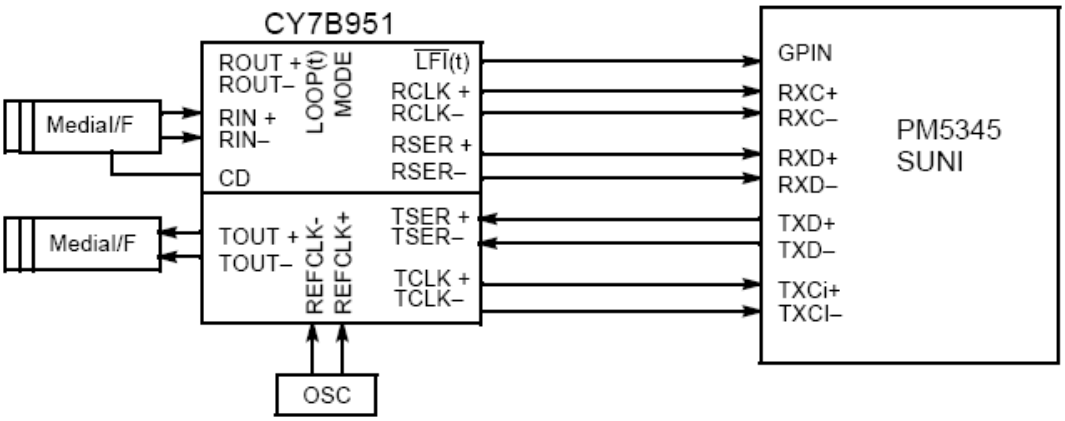
The CY7B951 can be used in Local Area Network ATM applications. The operating frequency of the CY7B951 is centered around the SONET/SDH STS-1 rate of 51.84 MHz and the SONET/SDH STS-3/STM-1 rate of 155.52 MHz. This device can also be used in data mover and Local Area Network (LAN) applications that operate at these frequencies.

The CY7B951 can provide clock and data recovery as well as output buffering for physical layer protocol engines such as the SONET/SDH and ATM processing application shown in Figure 1 and Figure 2.

Figure 1 shows the CY7B951 in an ATM system that uses the PMC-Sierra PM5345 SUNI, or the IgT WAC-013, or the Brooktree BT8222 device. Assuming that PM5345 SUNI is used, the CY7B951 will recover clock and data from the input serial data stream and pass it to the PM5345 SUNI. The SUNI device will perform serial to parallel conversion, SONET/SDH overhead processing and ATM cell processing and then pass ATM cells to an ATM packet reassembly engine. On the Transmit side, a segmentation engine will divide long packets of data such as Ethernet packets into 53 byte cells and pass them to the SUNI. The SUNI device will then perform ATM cell processing, such as header generation, SONET/SDH overhead processing and parallel to serial conversion. This serial data will then be passed to the CY7B951 which will buffer this data stream and pass it along to the transmission media.

The CY7B951 provides the necessary clock and data recovery function to the PM5345. These differential PECL clock and data signals interface directly with the RXD± and RXC± inputs of the SUNI device as shown in Figure 2. In addition, the CY7B951 provides transmit data output buffering for direct drive of cable transmission media. Lastly, the CY7B951 provides a bit rate reference clock to the SUNI transmitter by multiplying a local clock by eight allowing an inexpensive crystal oscillator to be used for the local reference.

Figure 2. CY7B951 to PMC-Sierra PM5345 SUNI Connection Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

Output Current into TTL Outputs (LOW).....30 mA

Output Current into ECL Outputs (HIGH).....–50 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .....>200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to 70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Condition	Min.	Max.	Unit
TTL Compatible Input Pins (LOOP, REFCLK+, REFCLK–)						
V_{IHT}	Input HIGH Voltage			2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage			–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK	$V_{IN} = V_{CC}$	+0.5	+200	µA
		LOOP	$V_{IN} = V_{CC}$	–10	+10	µA
I_{ILT}	Input LOW Current	REFCLK	$V_{IN} = 0.0V$	–50	+50	µA
		LOOP	$V_{IN} = 0.0V$	–500		µA
TTL Compatible Output Pins (LFI)						
V_{OHT}	Output HIGH Voltage		$I_{OH} = –2$ mA	2.4		v
V_{OLT}	Output LOW Voltage		$I_{OL} = 4$ mA		0.45	V
I_{OST}	Output Short Circuit Current		$V_{OUT} = 0V$[2]	–15	–90	mA
ECL Compatible Input Pins (REFCLK ± CD, TSER±, RIN±)						
I_{IHE}	ECL Input HIGH Current	REFCLK/CD	$V_{IN} = V_{IHE(MAX)}$		+250	µA
		TSER/RIN	$V_{IN} = V_{IHE(MAX)}$		+750	µA
I_{ILE}[3]	ECL Input LOW Current	REFCLK/CD	$V_{IN} = V_{ILE(MAX)}$	+0.5		µA
		TSER/RIN	$V_{IN} = V_{ILE(MAX)}$	–200		µA

Notes
1. T_A is the "instant on" case temperature.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Input currents are always positive at all voltages above $V_{CC}/2$.

Electrical Characteristics Over the Operating Range (continued)

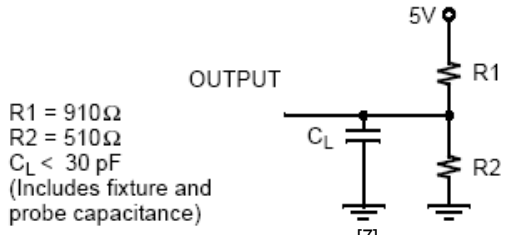
Parameter	Description		Test Condition	Min.	Max.	Unit
V_{IDIFF}	Input Differential Voltage	TSER/RIN		50	1200	mV
		REFCLK		100	1200	mV
V_{IHE}	Input High Voltage	TSER/RIN			V_{CC}	V
		REFCLK		3.0	V_{CC}	V
		CD		V_{CC} – 1.165	V_{CC}	V
V_{ILE}	Input LOW Voltage	TSER/RIN		2.0		V
		REFCLK		2.5		V
		CD (ECL)		2.5	V_{CC} – 1.475	V
		CD (Disable)		–0.5	0.8	V
ECL Compatible Output Pins (ROUT±, RCLK±, RSER±, TOUT±, TCLK±)						
V_{OHE}	ECL Output HIGH Voltage		Commercial	V_{CC} – 1.03	V_{CC} – 0.83	V
			Industrial[4]	V_{CC} – 1.08	V_{CC} – 0.83	V
V_{OLE}	ECL Output LOW Voltage		T > 0°C	V_{CC} – 1.86	V_{CC} – 1.62	V
V_{ODIFF}	Output Differential Voltage			0.6		V
Three-Level Input Pins (MODE)						
V_{IHH}	Three-Level Input HIGH			V_{CC} – 0.75	V_{CC}	V
V_{IMM}	Three-Level Input MID			$V_{CC}/2$ – 0.5	$V_{CC}/2$ + 0.5	V
V_{ILL}	Three-Level Input LOW			0.0	0.75	V
Operating Current[5]						
I_{CCS}	Static Operating Current				30	mA
I_{CCR}	Receiver Operating Current				50	mA
I_{CCT}	Transmitter Operating Current				13	mA
I_{CCE}	ECL Pair Operating Current				7.0	mA
I_{CC5}	Additional Current 51.84 MHz				7.0	mA
I_{CCO}	Additional Current $\overline{LFI}$ = LOW				3	mA

Capacitance[6]

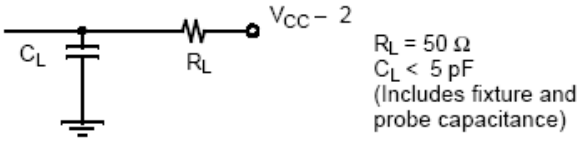
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 5.0V	10	pF

Notes
4. Specified only for temperatures below 0°C.
5. Total Receiver operating current (assuming that the Transmitter is not activated) can be found by adding $I_{CCS} + I_{CCR} + x * I_{CCE}$; where x is 2 if the ROUT± outputs are not activated and 3 if they are activated.
   Total Transmitter operating current (assuming that the Receiver is not activated) can be found by adding $I_{CCS} + I_{CCT} + x * I_{CCE}$; where x is 1 if the TOUT± outputs are not activated and 2 if they are activated.
   Total device power (assuming that the Transmitter and the Receiver are activated) can be found by adding $I_{CCS} + I_{CCR} + I_{CCT} + x * I_{CCE}$; where x represents the number of ECL output pairs activated.
6. Tested initially and after any design or process changes that may affect these parameters.

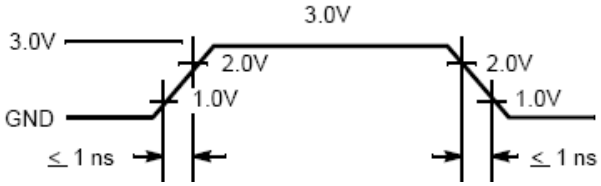
AC Test Loads and Waveforms



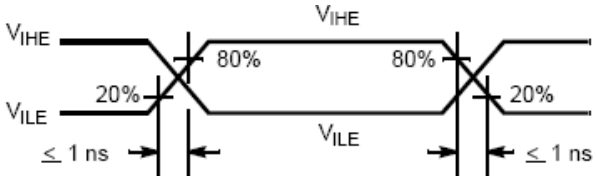
(a) TTL AC Test Load[7]



(b) ECL AC Test Load[7]



(c) TTL Input Test Waveform



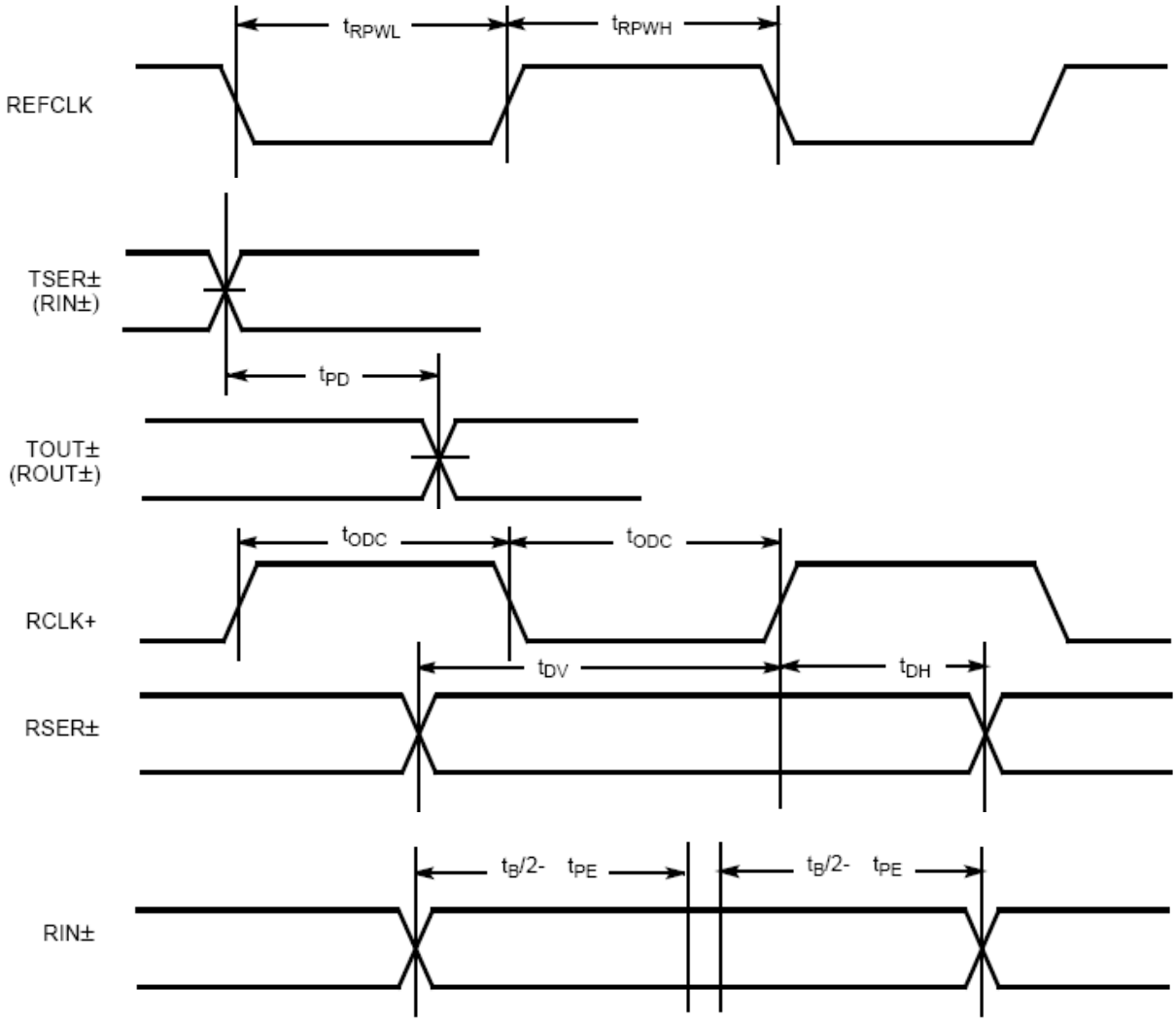
(d) ECL Input Test Waveform

Switching Characteristics Over the Operating Range

Parameter	Description		Min.	Max.	Unit
f_{REF}	Reference Frequency	MODE = LOW	6.41	6.55	MHz
		MODE = HIGH	19.24	19.64	MHz
f_B	Bit Time[8]	MODE = LOW	19.5	19.1	ns
		MODE = HIGH	6.50	6.40	ns
t_{PE}	Receiver Static Phase Error[6]	MODE = LOW		100	ps
		MODE = HIGH		200	ps
t_{ODC}	Output Duty Cycle (TCLK±, RCLK±)[6]		48	52	%
t_{RF}	Output Rise/Fall Time[6]		0.4	1.2	ns
t_{LOCK}	PLL Lock Time (RIN transition density 25%)[9]			100	µs
t_{RPWH}	REFCLK Pulse Width HIGH		10		ns
t_{RPWL}	REFCLK Pulse Width HIGH		10		ns
t_{DV}	Data Valid		3		ns
t_{DH}	Data Hold		1		ns
t_{PD}	Propagation Delay (RIN to ROUT, TSER to TOUT)[10]			10	ns

Notes
7. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
8. f_B is calculated as $1/(f_{REF}X8)$.
9. t_{LOCK} is the time needed for transitioning from lock to REFCLK X8 to lock to data.
10. The ECL switching threshold is the differential zero crossing (i.e., the place where + and – signals cross).

Switching Waveforms for the CY7B951 SONET/SDH Serial Transceiver

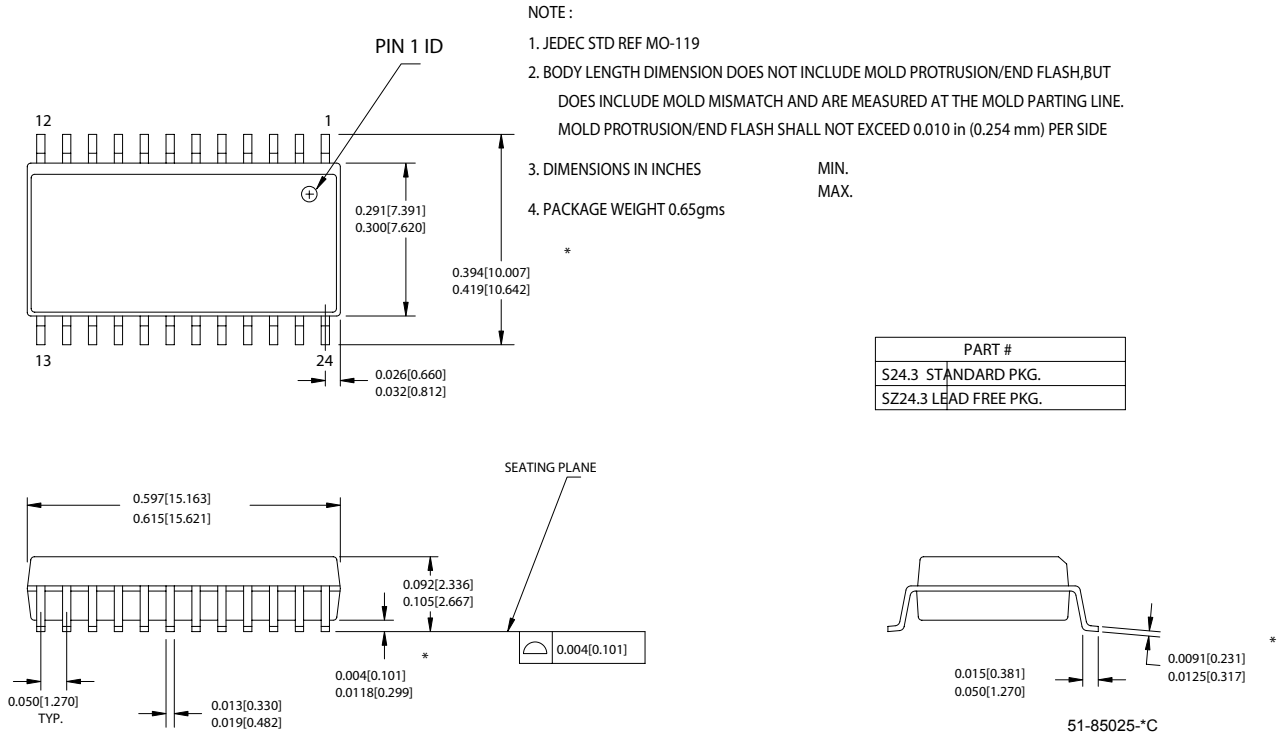


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7B951-SC	S24.3	24-Lead (300-Mil) Molded SOIC	Commercial
25	CY7B951-SXC	SZ24.3	24-Lead (300-Mil) Pb-Free Molded SOIC	Commercial
25	CY7B951-SI	S24.3	24-Lead (300-Mil) Molded SOIC	Industrial
25	CY7B951-SXI	SZ24.3	24-Lead (300-Mil) Pb-Free Molded SOIC	Industrial

Package Diagram

Figure 3. 24-Lead (300-Mil) SOIC S24.3/SZ24.3



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Document History Page

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