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Status	Product Specification
ACL Products	

AC11013: Product Specification
ACT11013: Objective Specification
Dual 4-input NAND Schmitt-trigger

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11013 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11013 provides two separate 4-input NAND gate functions which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	C_L = 50pF	4.3	8.0	ns
C_{PD}	Power dissipation capacitance,per gate[1]	f = 1MHz; C_L = 50pF	29	32	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

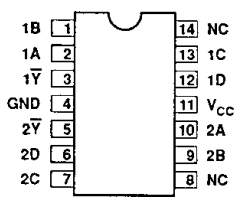
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

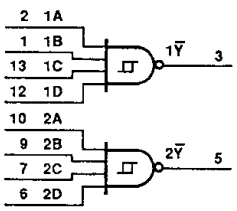
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11013N 74ACT11013N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11013D 74ACT11013D

PIN CONFIGURATION

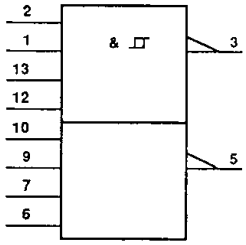
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 4-input NAND Schmitt-trigger 74AC/ACT11013

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	$1\overline{Y}$ - $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	$n\overline{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11013			74ACT11013			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 4-input NAND Schmitt-trigger

74AC/ACT11013

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11013				74ACT11013				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		3.6		0.44					
			I_{OL} = 24mA	4.5		3.6		0.44		3.6		0.44	
				5.5		3.6		0.44		3.6		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±0.1		±0.1		±0.1	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		4.0		4.0		4.0		4.0	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 4-input NAND Schmitt-trigger 74AC/ACT11013

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11013					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	2.5 2.3	6.4 6.5	8.7 8.7	2.5 2.3	9.7 9.9	ns

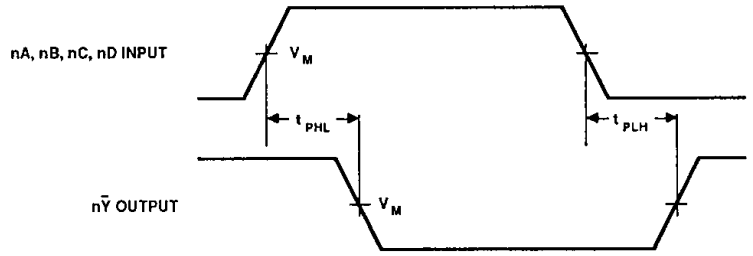
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11013					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	2.0 2.0	4.2 4.4	6.4 6.9	2.0 2.0	7.1 7.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11013					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (n$\overline{Y}$) Propagation Delays

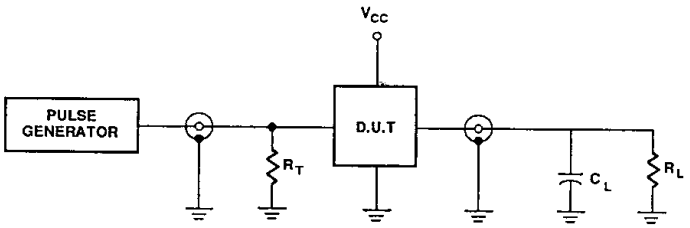
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Dual 4-input NAND Schmitt-trigger

74AC/ACT11013

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns