

20Amps, 650Volts N-Channel Super Junction MOS-FET

Product Summary

$V_{DS} @ T_{j,max}$	650V
$R_{DS(on),max}$	0.15Ω
I_{DM}	60A
$Q_{g,typ}$	39nC

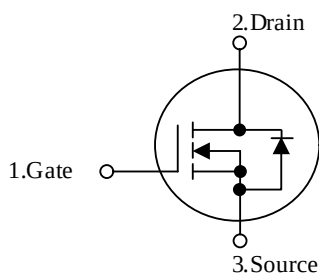
DESCRIPTION

FTK20NS65 Power MOS FET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

FEATURES

- ☐ Ultra fast body diode
- ☐ Ultra low $R_{DS(on)}$
- ☐ Ultra low gate charge (typ. $Q_g = 39nC$)
- ☐ 100% UIS tested
- ☐ RoHS compliant

SYMBOL



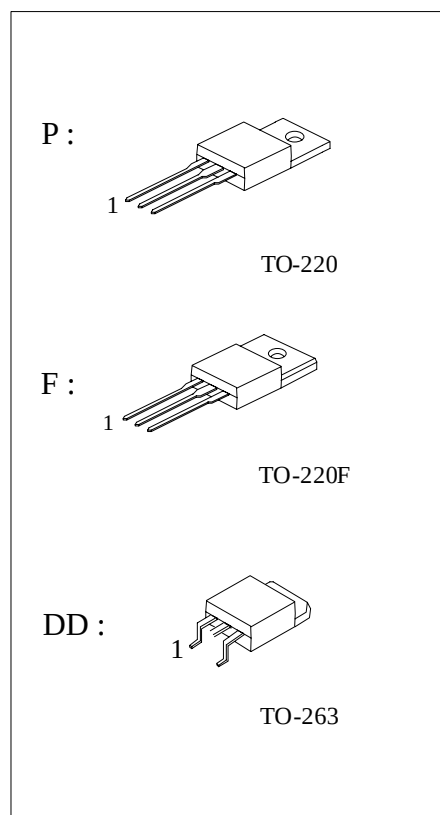
Applications

- ☐ Power factor correction (PFC).
- ☐ Switched mode power supplies (SMPS).
- ☐ Uninterruptible power supply (UPS).

ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK20NS65P	TO-220	G	D	S	Tube
FTK20NS65F	TO-220F	G	D	S	Tube
FTK20NS65DD	TO-263	G	D	S	Reel & Taping

Note: Pin Assignment: G: Gate D: Drain S: Source





Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DSS}	650	V
Continuous drain current ($T_c = 25^{\circ}\text{C}$) ($T_c = 100^{\circ}\text{C}$)	I_D	20	A
		13	A
Pulsed drain current ¹⁾	I_{DM}	60	A
Gate - Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse ²⁾	E_{AS}	600	mJ
Avalanche energy, repetitive ³⁾	E_{AR}	0.4	mJ
Avalanche current, repetitive ³⁾	I_{AR}	20	A
Power Dissipation ($T_c = 25^{\circ}\text{C}$) - Derate above 25°C	P_D	205	W
		1.64	W/ $^{\circ}\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^{\circ}\text{C}$
Continuous diode forward current	I_S	20	A
Diode pulse current	$I_{S,pulse}$	60	A

Thermal Characteristics TO-220/TO-263

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.61	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	$^{\circ}\text{C/W}$

Thermal Characteristics TO-220F

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.7	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	$^{\circ}\text{C/W}$



FTK20NS65P/F/DD

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =0.25 mA	650	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =0.25mA	2.5	3.5	4.5	V
Drain cut-off current	I _{DSS}	V _{DS} =650 V, V _{GS} =0 V, T _j = 25°C T _j = 125°C	- -	- 10	1 -	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =30 V, V _{DS} =0 V	-	-	50	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-30 V, V _{DS} =0 V	-	-	-50	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =10 A T _j = 25°C T _j = 150°C	- - -	 0.15 0.4	 0.18 -	 Ω
Gate resistance	R _G	f=1 MHz, open drain	-	4.5	-	Ω
Dynamic characteristics						
Input capacitance	C _{iSS}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	2637	-	pF
Output capacitance	C _{oSS}		-	1250	-	
Reverse transfer capacitance	C _{rSS}		-	17	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 380V, I _D = 10A R _G = 4.7Ω, V _{GS} =10V	-	23	-	ns
Rise time	t _r		-	33	-	
Turn-off delay time	t _{d(off)}		-	113	-	
Fall time	t _f		-	11	-	
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DD} =480 V, I _D =10A, V _{GS} =0 to 10 V	-	10.3	-	nC
Gate to drain charge	Q _{gd}		-	13.7	-	
Gate charge total	Q _g		-	39	-	
Gate plateau voltage	V _{plateau}		-	5.5	-	V
Reverse diode characteristics						
Diode forward voltage	V _{SD}	V _{GS} =0 V, I _F =10A	-	1.0	-	V
Reverse recovery time	t _{rr}	V _R =50 V, I _F =20A, dI _F /dt=100 A/μs	-	513	-	ns
Reverse recovery charge	Q _{rr}		-	7.5	-	μC
Peak reverse recovery current	I _{rrm}		-	29	-	A

Notes:

- Limited by maximum junction temperature, maximum duty cycle is 0.75.
- I_{AS} = 5A, V_{DD} =60V, Starting T_j= 25°C.
- Repetitive Rating: Pulse width limited by maximum junction temperature.

Typical Characteristics

Electrical Characteristics Diagrams

Figure 1. On-Region Characteristics

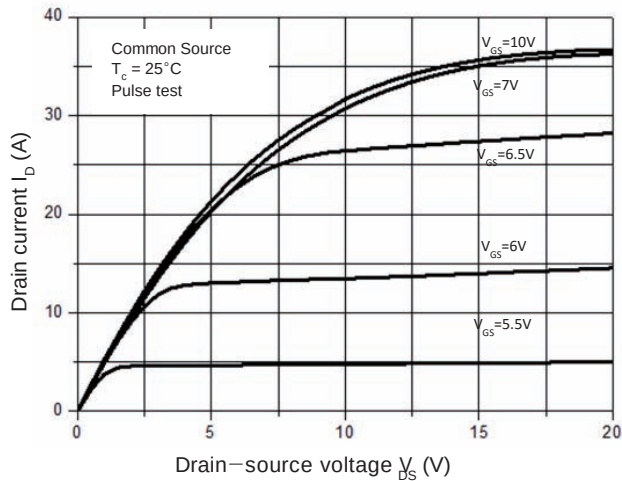


Figure 2. Transfer Characteristics

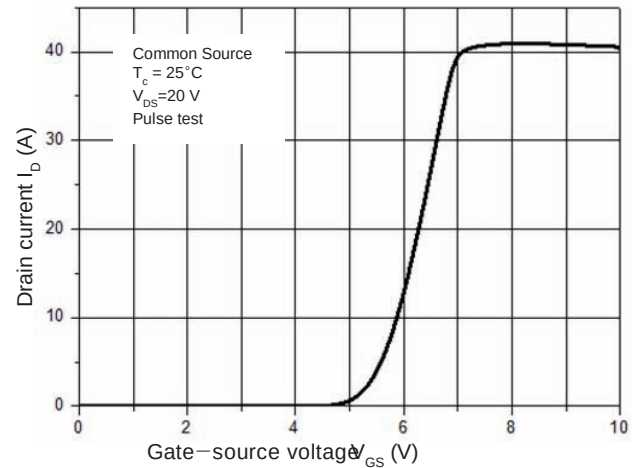


Figure 3. On-Resistance Variation vs. Drain Current

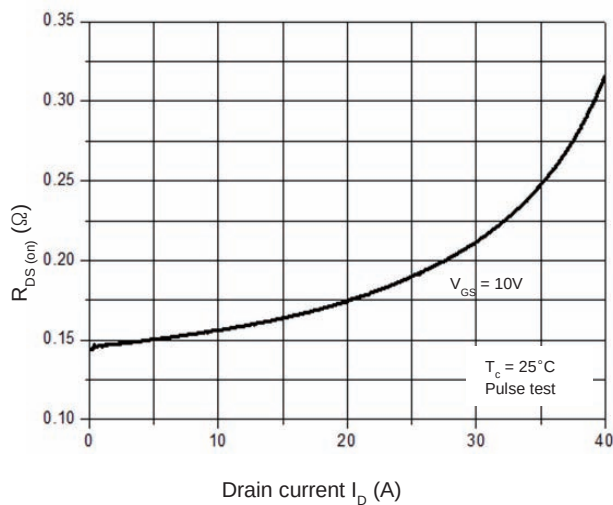


Figure 4. Threshold Voltage vs. Temperature

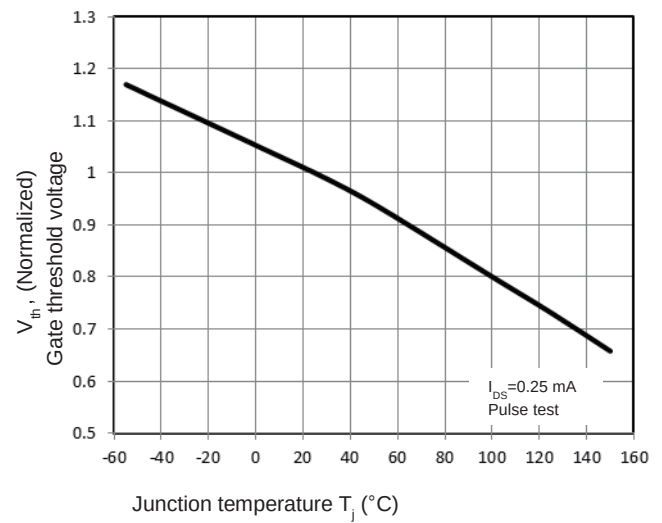


Figure 5. Breakdown Voltage vs. Temperature

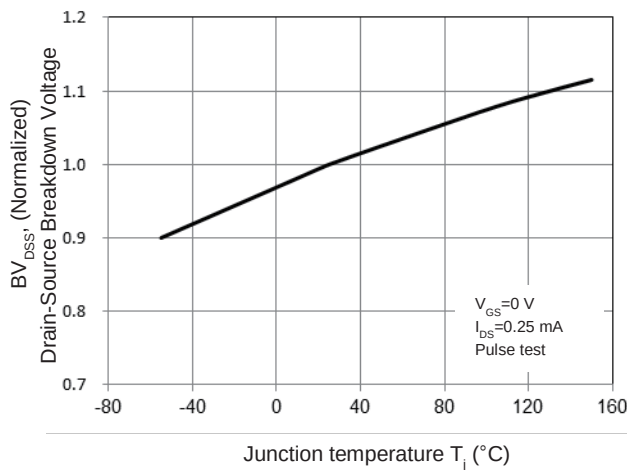


Figure 6. On-Resistance vs. Temperature

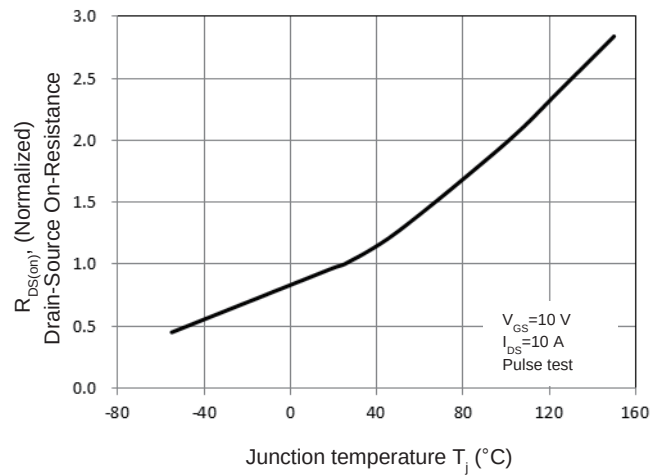


Figure 7. Capacitance Characteristics

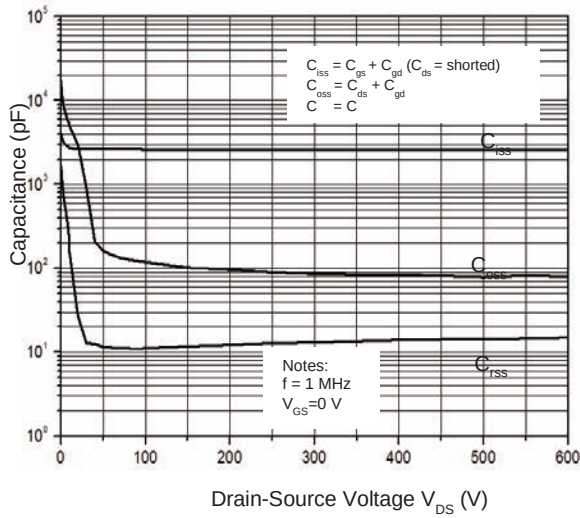


Figure 8. Gate Charge Characterist

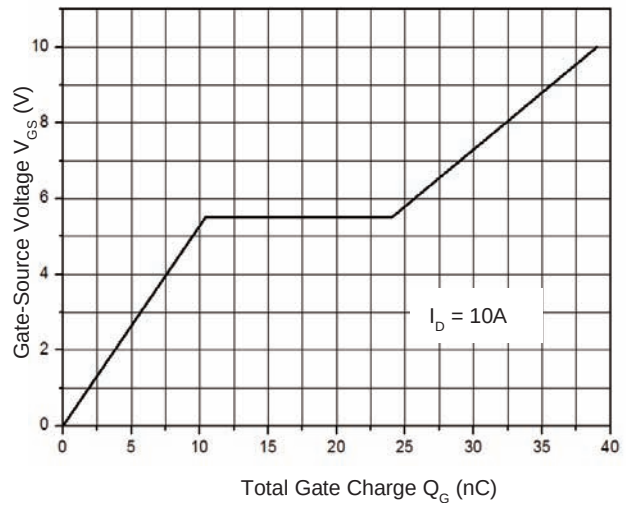


Figure 9.1 Maximum Safe Operating Area

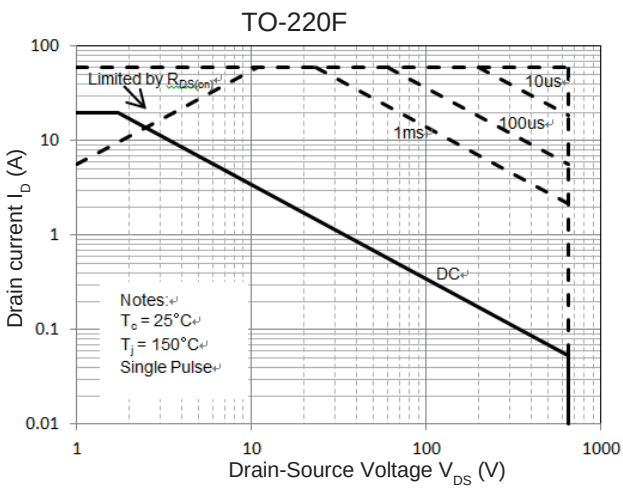


Figure 9.2 Maximum Safe Operating Area

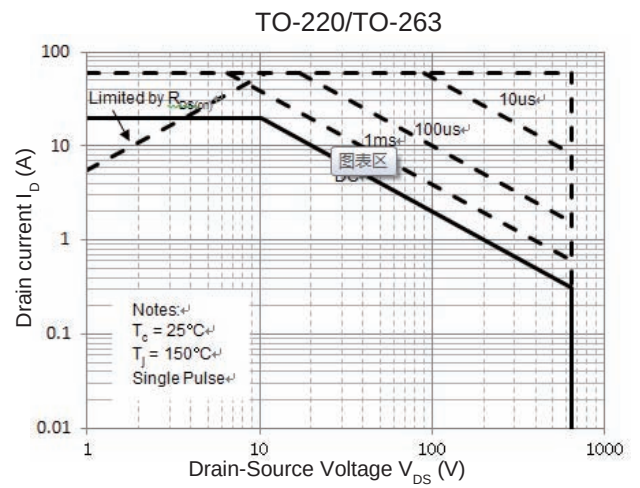


Figure 10.1 Power Dissipation vs. Temperature

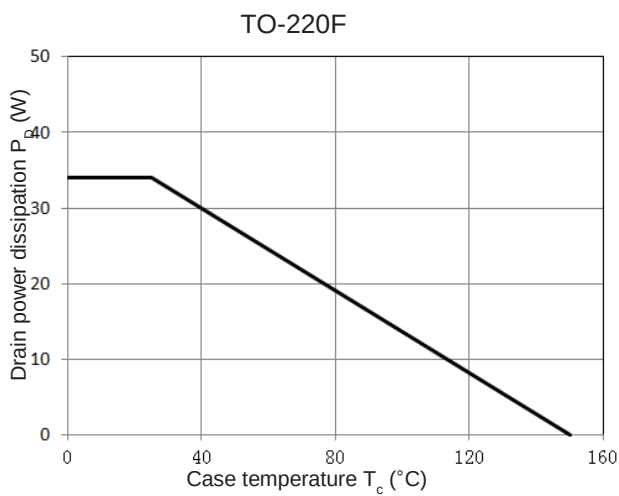
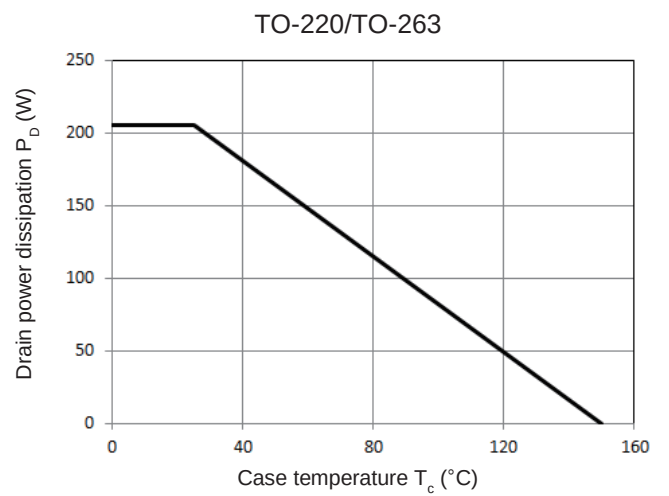


Figure 10.2 Power Dissipation vs. Temperature





■ TEST CIRCUITS AND WAVEFORMS (Cont.)

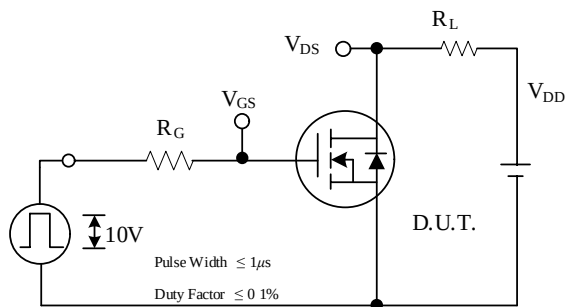


Fig. 2A Switching Test Circuit

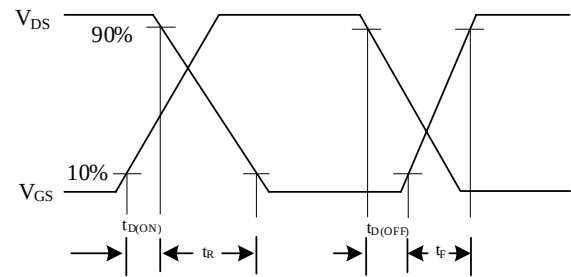


Fig. 2B Switching Waveforms

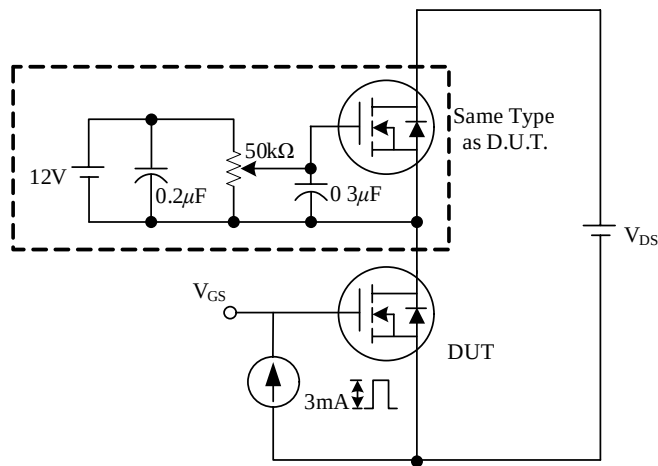


Fig. 3A Gate Charge Test Circuit

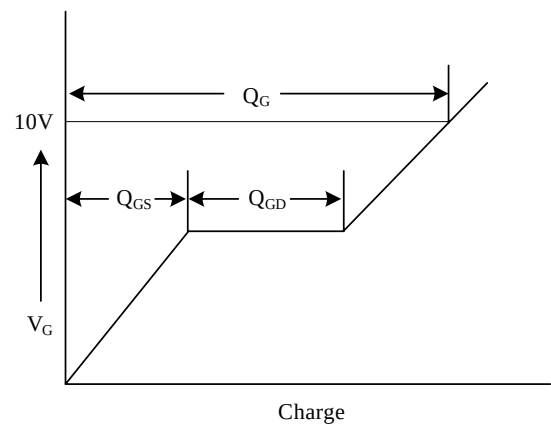


Fig. 3B Gate Charge Waveform

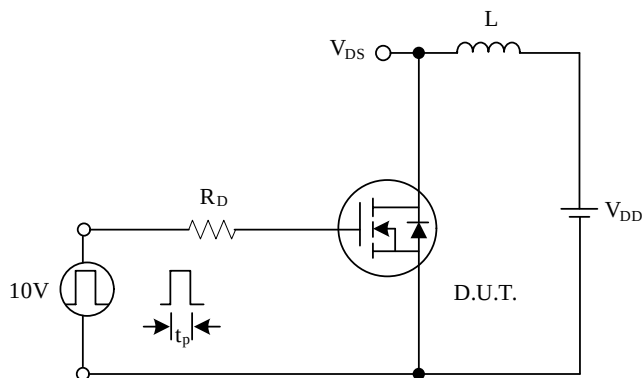


Fig. 4A Unclamped Inductive Switching Test Circuit

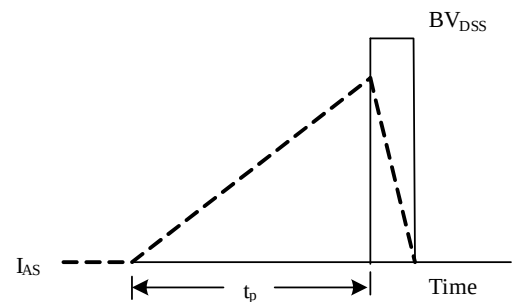


Fig. 4B Unclamped Inductive Switching Waveforms