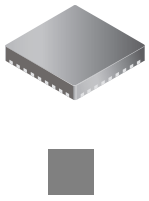
Bipolar Stepper and High Current DC Motor Driver

Features and Benefits

- 36 V output rating
- 2.4 A dc motor driver
- 1.2 A bipolar stepper driver
- Synchronous rectification
- Internal undervoltage lockout (UVLO)
- Thermal shutdown circuitry
- Crossover-current protection
- Very thin profile QFN package

Package: 36 pin QFN with exposed thermal pad
0.90 mm nominal height (suffix EV)



Approximate scale 1:1

Description

The A3989 is designed operate at voltages up to 36 V while driving one bipolar stepper motor, at currents up to 1.2A, and one dc motor, at currents up to 2.4 A. The A3989 includes a fixed off-time pulse width modulation (PWM) regulator for current control. The stepper motor driver features dual 2-bit nonlinear DACs (digital-to-analog converters) that enable control in full, half, and quarter steps. The dc motor is controlled using standard PHASE and ENABLE signals. Fast or slow current decay is selected via the MODE pin. The PWM current regulator uses the Allegro® patented mixed decay mode for reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Protection features include thermal shutdown with hysteresis, undervoltage lockout (UVLO) and crossover current protection. Special power up sequencing is not required.

The A3989 is supplied in a leadless 6 mm × 6 mm × 0.9 mm, 36 pin QFN package with exposed power tab for enhanced thermal performance. The package is lead (Pb) free, with 100% matte tin leadframe plating.

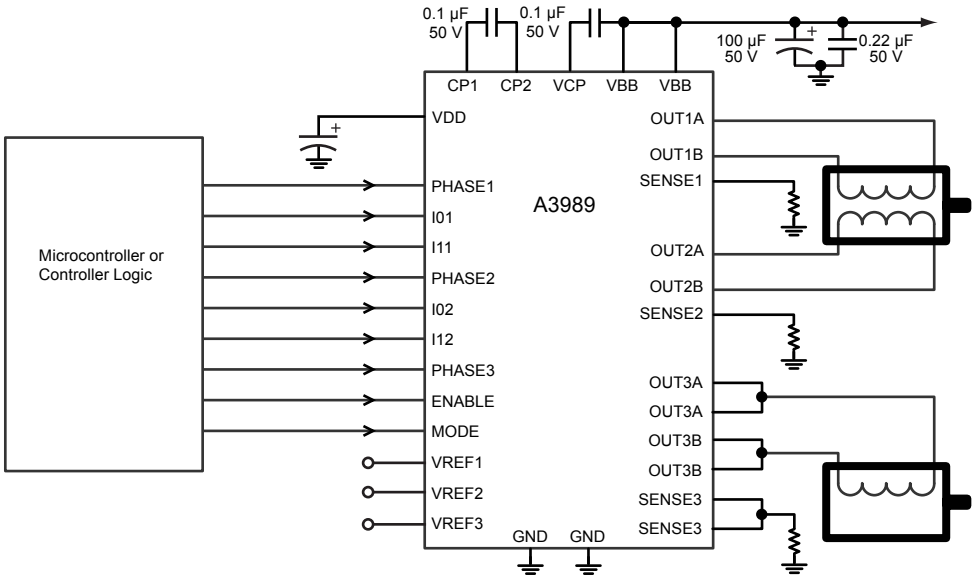


Figure 1. Typical application circuit

Selection Guide

Part Number	Packing
A3989SEV-T	61 pieces per tube
A3989SEVTR-T	1500 pieces per reel

Absolute Maximum Ratings

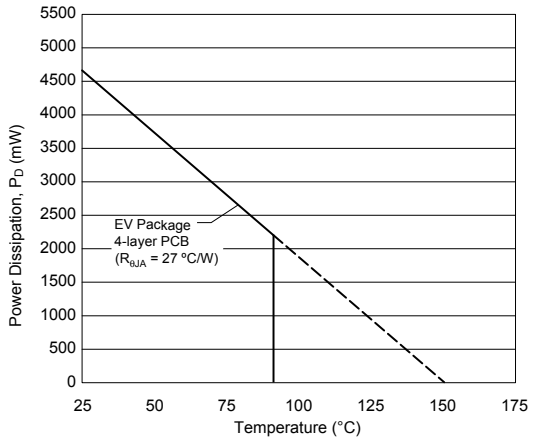
Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		-0.5 to 36	V
		Pulsed t_w < 1 µs	38	V
Logic Supply Voltage	V_{DD}		–0.4 to 7	V
Output Current*	I_{OUT}	Stepper motor driver, continuous	1.2	A
		Stepper motor driver, pulsed t_w < 1µs	2.8	A
		Dc motor driver, continuous	2.4	A
		Dc motor driver, pulsed t_w < 1µs	3.5	A
Logic Input Voltage Range	V_{IN}		–0.3 to 7	V
SENSEx Pin Voltage	V_{SENSEx}		0.5	V
		Pulsed t_w < 1µs	2.5	V
VREF*x* Pin Voltage	V_{REFx}		2.5	V
Operating Temperature Range	T_A	Range S	–20 to 85	ºC
Junction Temperature	T_J(max)		150	ºC
Storage Temperature Range	T_{stg}		–55 to 150	ºC

* May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a Junction Temperature of 150°C.

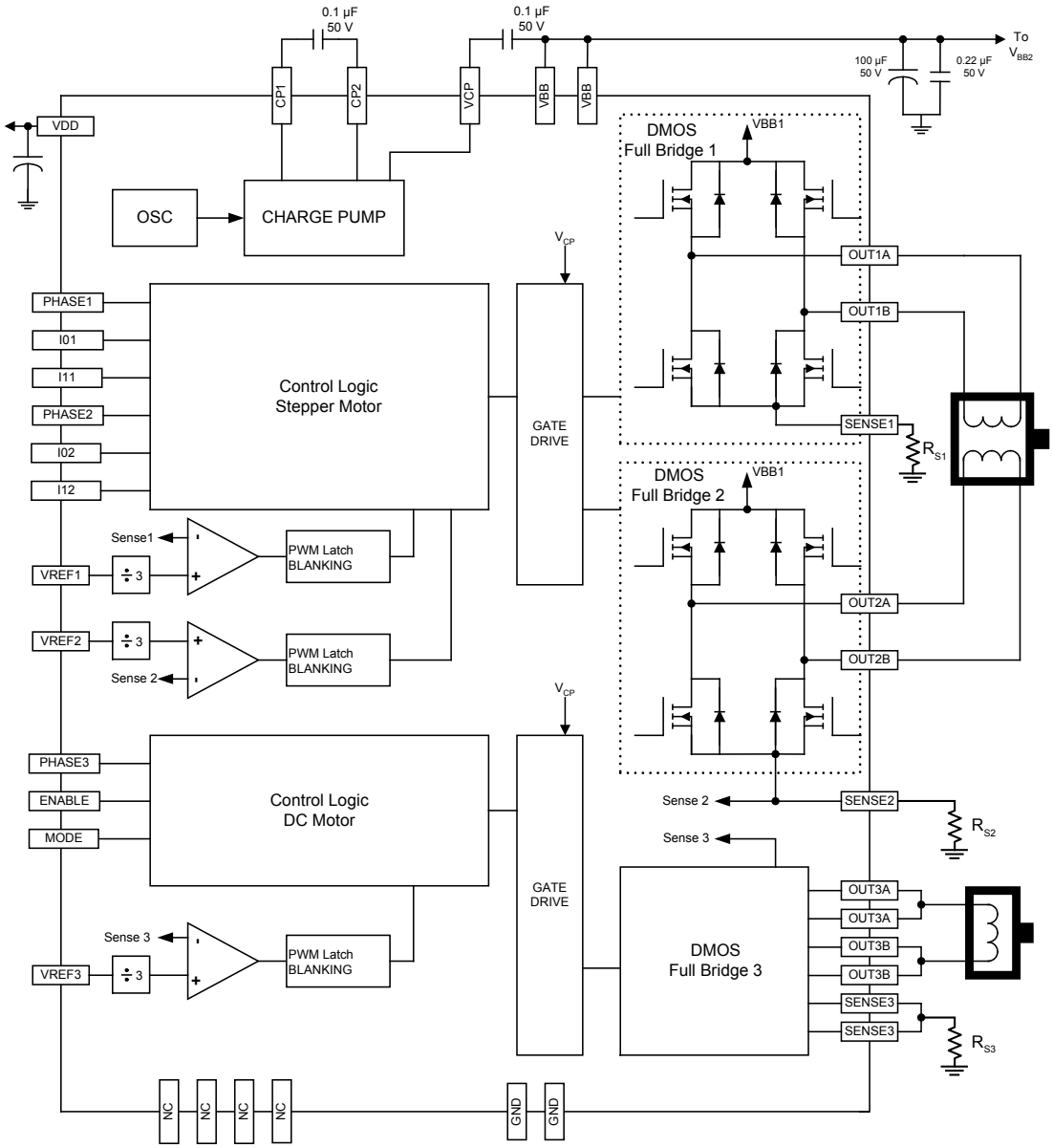
Thermal Characteristics (may require derating at maximum conditions)

Characteristic	Symbol	Test Conditions	Min.	Units
Package Thermal Resistance	$R_{\theta JA}$	EV package, 4 layer PCB based on JEDEC standard	27	ºC/W

Power Dissipation versus Ambient Temperature



Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1], **valid at T_A = 25 °C, V_{BB} = 36 V, unless otherwise noted**

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Load Supply Voltage Range	V_{BB}	Operating	8.0	–	36	V
Logic Supply Voltage Range	V_{DD}	Operating	3.0	–	5.5	V
VDD Supply Current	I_{DD}		–	7	10	mA
Output On Resistance (dc motor driver)	$R_{DS(on)dc}$	Source driver, I_{OUT} = –1.2 A, T_J = 25°C	–	350	450	mΩ
		Sink driver, I_{OUT} = 1.2 A, T_J = 25°C	–	350	450	mΩ
Output On Resistance (stepper motor driver)	$R_{DS(on)st}$	Source driver, I_{OUT} = –1.2 A, T_J = 25°C	–	700	800	mΩ
		Sink driver, I_{OUT} = 1.2 A, T_J = 25°C	–	700	800	mΩ
V_f, Outputs		I_{OUT} = 1.2 A	–	–	1.2	V
Output Leakage	I_{DSS}	Outputs, V_{OUT} = 0 to V_{BB}	–20	–	20	µA
VBB Supply Current	I_{BB}	I_{OUT} = 0 mA, outputs on, PWM = 50 kHz, DC = 50%	–	–	8	mA
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		0.7×V_{DD}	–	–	V
	$V_{IN(0)}$		–	–	0.3×V_{DD}	V
Logic Input Current	I_{IN}	V_{IN} = 0 to 5 V	–20	<1.0	20	µA
Input Hysteresis	V_{hys}		150	300	500	mV
Propagation Delay Times	t_{pd}	PWM change to source on	350	550	1000	ns
		PWM change to source off	35	–	300	ns
		PWM change to sink on	350	550	1000	ns
		PWM change to sink off	35	–	250	ns
Crossover Delay	t_{COD}		300	425	1000	ns
Blank Time (dc motor driver)	$t_{BLANKdc}$		2.5	3.2	4	µs
Blank Time (stepper motor driver)	$t_{BLANKst}$		0.7	1	1.3	µs
VREF*x* Pin Input Voltage Range	V_{REFx}	Operating	0.0	–	1.5	V
VREF*x* Pin Reference Input Current	I_{REF}	V_{REF} = 1.5	–	–	±1	µA
Current Trip-Level Error[3]	V_{ERR}	V_{REF} = 1.5, phase current = 100%	–5	–	5	%
		V_{REF} = 1.5, phase current = 67%	–5	–	5	%
		V_{REF} = 1.5, phase current = 33%	–15	–	15	%
Protection Circuits						
VBB UVLO Threshold	$V_{UV(VBB)}$	V_{BB} rising	7.3	7.6	7.9	V
VBB Hysteresis	$V_{UV(VBB)hys}$		400	500	600	mV
VDD UVLO Threshold	$V_{UV(VDD)}$	V_{DD} rising	2.65	2.8	2.95	V
VDD Hysteresis	$V_{UV(VDD)hys}$		75	105	125	mV
Thermal Shutdown Temperature	T_{JTSD}		155	165	175	°C
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[3]$V_{ERR} = [(V_{REF}/3) – V_{SENSE}] / (V_{REF}/3)$.

DC Control Logic

PHASE	ENABLE	MODE	OUTA	OUTB	Function
1	1	1	H	L	Forward (slow decay SR)
1	1	0	H	L	Forward (fast decay SR)
0	1	1	L	H	Reverse (slow decay SR)
0	1	0	L	H	Reverse (fast decay SR)
X	0	1	L	L	Brake (slow decay SR)
1	0	0	L	H	Fast decay SR*
0	0	0	H	L	Fast decay SR*

* To prevent reversal of current during fast decay SR – the outputs will go to the high impedance state as the current gets near zero.

Functional Description

Device Operation The A3989 is designed to operate one dc motor and one bipolar stepper motor. The currents in each of the full bridges, all N-channel DMOS, are regulated with fixed off-time pulse width modulated (PWM) control circuitry. The peak current in each full bridge is set by the value of an external current sense resistor, R_{Sx}, and a reference voltage, V_{REFx}.

If the logic inputs are pulled up to VDD, it is good practice to use a high value pullup resistor in order to limit current to the logic inputs should an overvoltage event occur. Logic inputs include: PHASEx, I0x, I1x, ENABLE, and MODE.

Internal PWM Current Control Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a user-specified value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and R_{Sx}. When the voltage across the current sense resistor equals the voltage on the VREFx pin, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting is set by the selection of R_S and the voltage at the VREF input with a transconductance function approximated by:

$$I_{TripMax} = V_{REF} / (3 \times R_S)$$

The stepper motor outputs will define each current step as a percentage of the maximum current, $I_{TripMax}$. The actual current at each step I_{Trip} is approximated by:

$$I_{Trip} = (\%\ I_{TripMax} / 100)\ I_{TripMax}$$

where $\%\ I_{TripMax}$ is given in the Step Sequencing table.

Note: It is critical to ensure that the maximum rating of ±500 mV on each SENSEx pin is not exceeded.

Fixed Off-Time The internal PWM current control circuitry uses a one shot circuit to control the time the drivers remain off. The one shot off-time, t_{off}, is internally set to 30 µs.

Blanking This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions, due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. Dc motors require more blank time than stepper motors. The stepper driver blank time, $t_{BLANKst}$, is approximately 1 µs. The dc driver blank time, $t_{BLANKdc}$, is approximately 3 µs.

Control Logic Stepper motor communication is implemented via industry standard I1, I0, and PHASE interface. This communication logic allows for full, half, and quarter step modes. Each bridge also has an independent V_{REF} input so higher resolution step modes can be programmed by dynamically changing the voltage on the corresponding VREFx pin. The dc motor is controlled using standard PHASE, ENABLE communication. Fast or slow current decay during the off-time is selected via the MODE pin.

Charge Pump (CP1 and CP2) The charge pump is used to generate a gate supply greater than the V_{BB} in order to drive the source-side DMOS gates. A 0.1 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 µF ceramic capacitor is required between VCP and VBBx to act as a reservoir to operate the high-side DMOS devices.

Shutdown In the event of a fault (excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers.

Synchronous Rectification When a PWM-off cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The A3989 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay. This effectively shorts the body diode with the low $R_{DS(on)}$ driver. This significantly lowers power dissipation. When a zero current level

is detected, synchronous rectification is turned off to prevent reversal of the load current.

Mixed Decay Operation The stepper driver operates in mixed decay mode. Referring to figure 2, as the trip point is reached, the device goes into fast decay mode for 30.1% of the fixed off-time period. After this fast decay portion, t_{FD}, the device switches to slow decay mode for the remainder of the off-time. The dc driver decay mode is determined by the MODE pin. During transitions from fast decay to slow decay, the drivers are forced off for approximately 600 ns. This feature is added to prevent shoot-through in the bridge. As shown in figure 2, during this "dead time" portion, synchronous rectification is not active, and the device operates in fast decay and slow decay only.

MODE Control input MODE is used to toggle between fast decay mode and slow decay mode for the dc driver. A logic high puts the device in slow decay mode. Synchronous rectification is always enabled when ENABLE is low.

Braking Driving the device in slow decay mode via the MODE pin and applying an ENABLE chop command implements the Braking function. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts the motor-generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by V_{BEMF}/R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst case braking situations: high speed and high inertia loads.

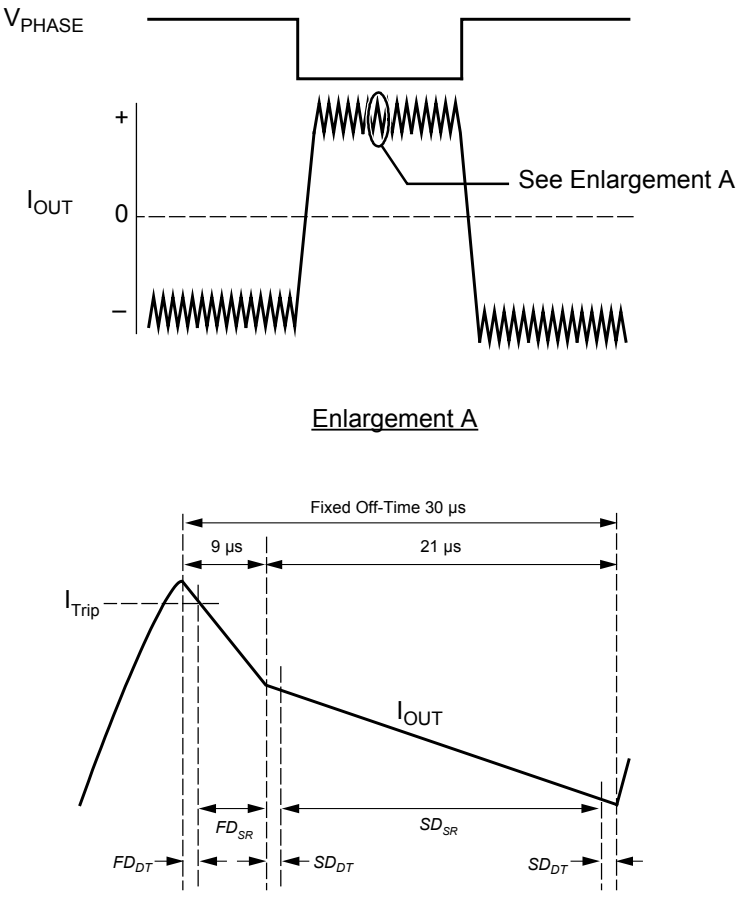


Figure 2. Mixed Decay Mode Operation

Step Sequencing Diagrams

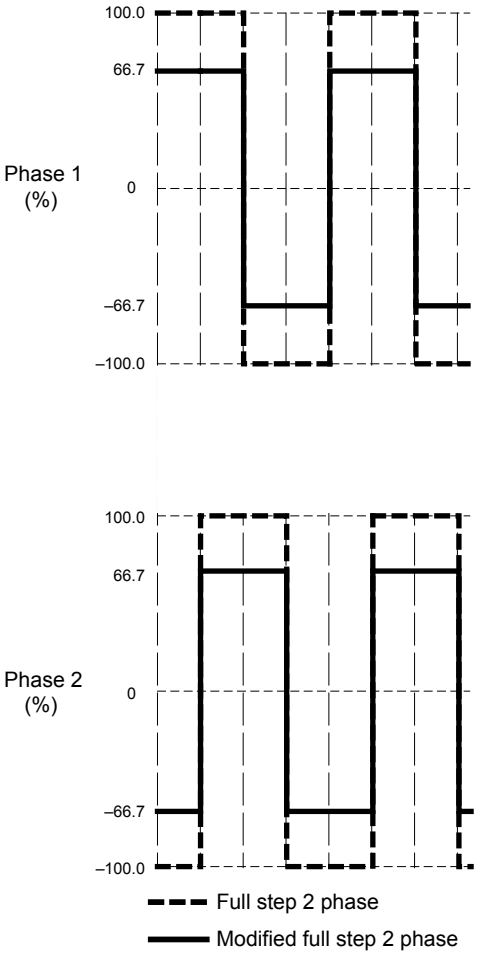


Figure 3. Step Sequencing for Full-Step Increments.

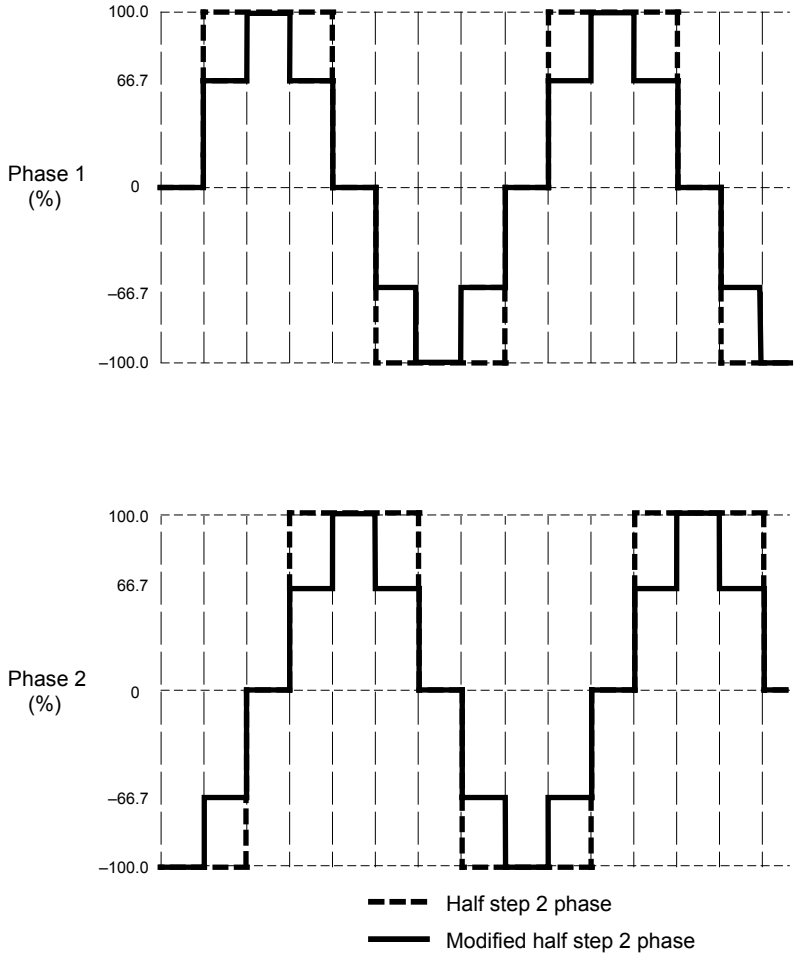


Figure 4. Step Sequencing for Half-Step Increments.

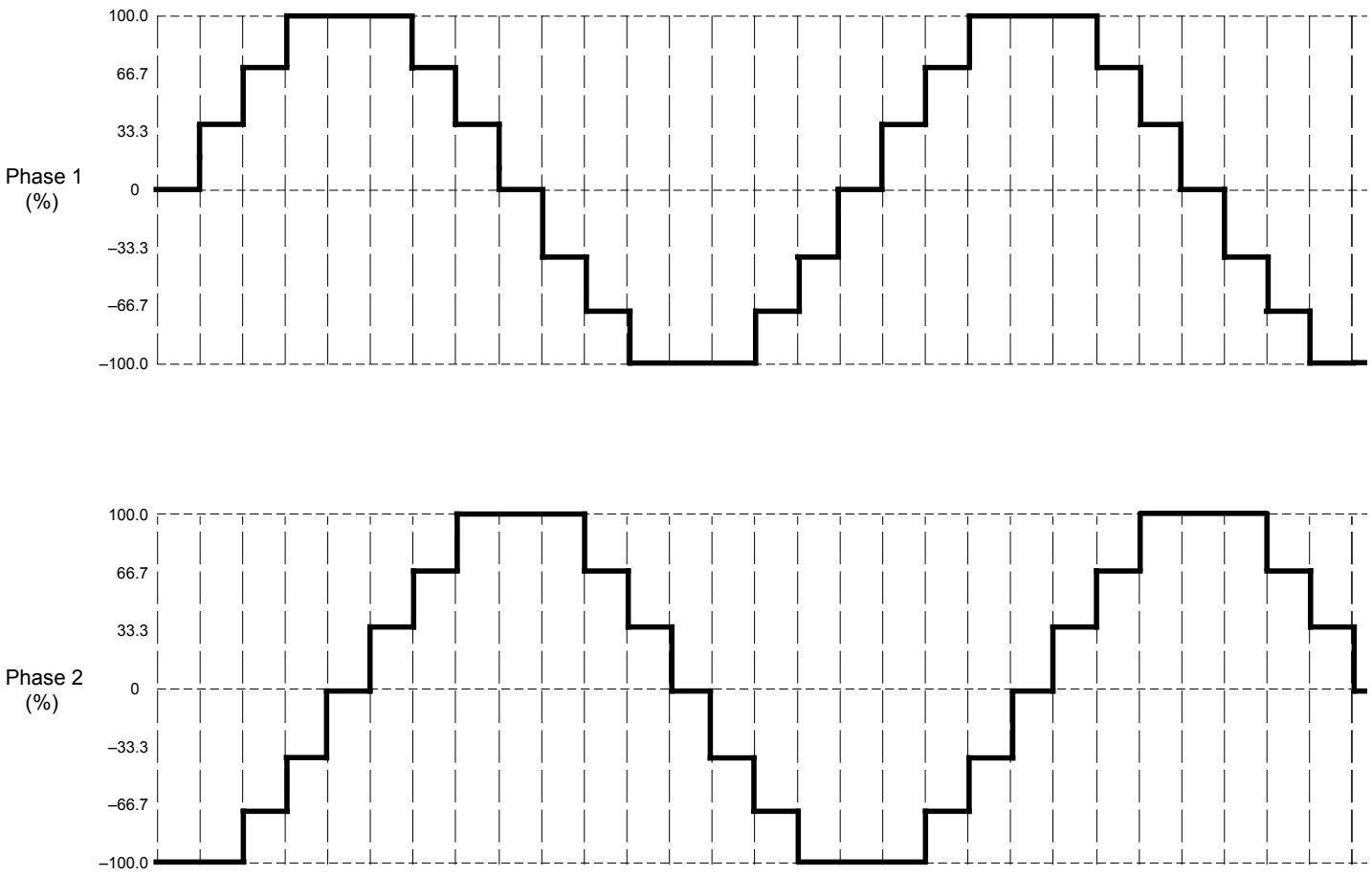


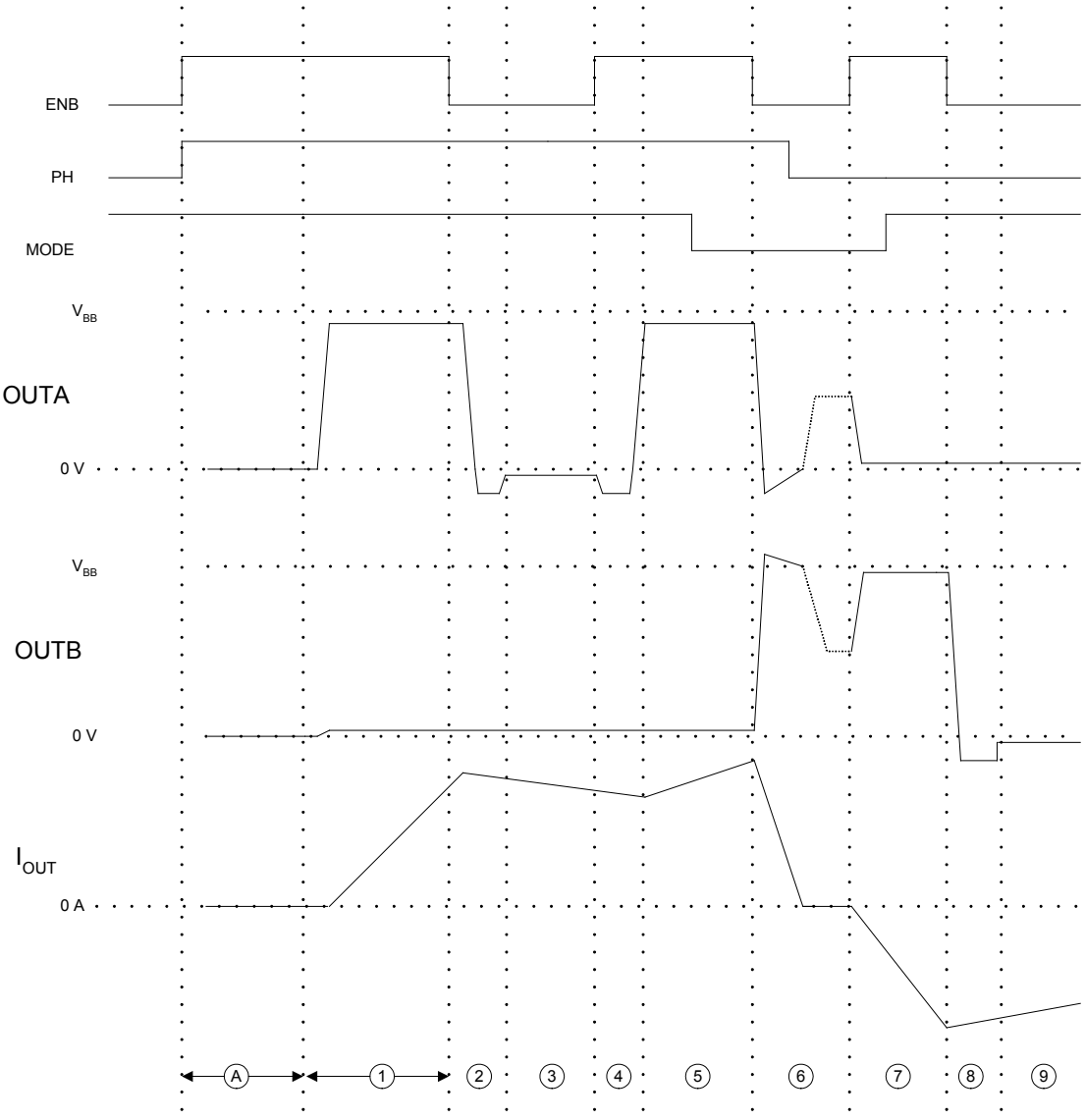
Figure 5. Decay Modes for Quarter-Step Increments

Step Sequencing Settings

Full	1/2	1/4	Phase 1 ($\%I_{TripMax}$)	I0x	I1x	PHASE	Phase 2 ($\%I_{TripMax}$)	I0x	I1x	PHASE
	1	1	0	H	H	x	100	L	L	1
		2	33	L	H	1	100	L	L	1
1	2	3	66*/100	H	L*/H	1	66*/100	H	L*/H	1
		4	100	L	L	1	33	L	H	1
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	0
2	4	7	66*/100	H	L*/H	1	66*/100	H	L*/H	0
		8	33	L	H	1	100	L	L	0
	5	9	0	H	H	x	100	L	L	0
		10	33	L	H	0	100	L	L	0
3	6	11	66*/100	H	L*/H	0	66*/100	H	L*/H	0
		12	100	L	L	0	33	L	H	0
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	1
4	8	15	66*/100	H	L*/H	0	66*/100	H	L*/H	1
		16	33	L	H	0	100	L	L	1

* Denotes modified step mode

Logic Timing Diagram, DC Driver



(A) Charge Pump and VREG Power-up Delay (≈200 µs)

Applications Information

Motor Configurations For applications that require either dual dc or dual stepper motors, Allegro offers the A3988 and A3995. Both devices are offered in a 36 pin QFN package. Please refer to the Allegro website for further information and datasheets for the devices.

Layout The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the A3989 must be soldered directly onto the board. On the underside of the A3989 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

Grounding In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the exposed thermal pad and the groundplane directly under the A3989, that area becomes an ideal location for a star ground point.

A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star ground under the device, to serve both as low impedance ground point and thermal path.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor. This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.

Sense Pins The sense resistors, RS*x*, should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the SENSE*x* pins have very short traces to the RS*x* resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the SENSE*x* pins of ±500 mV.

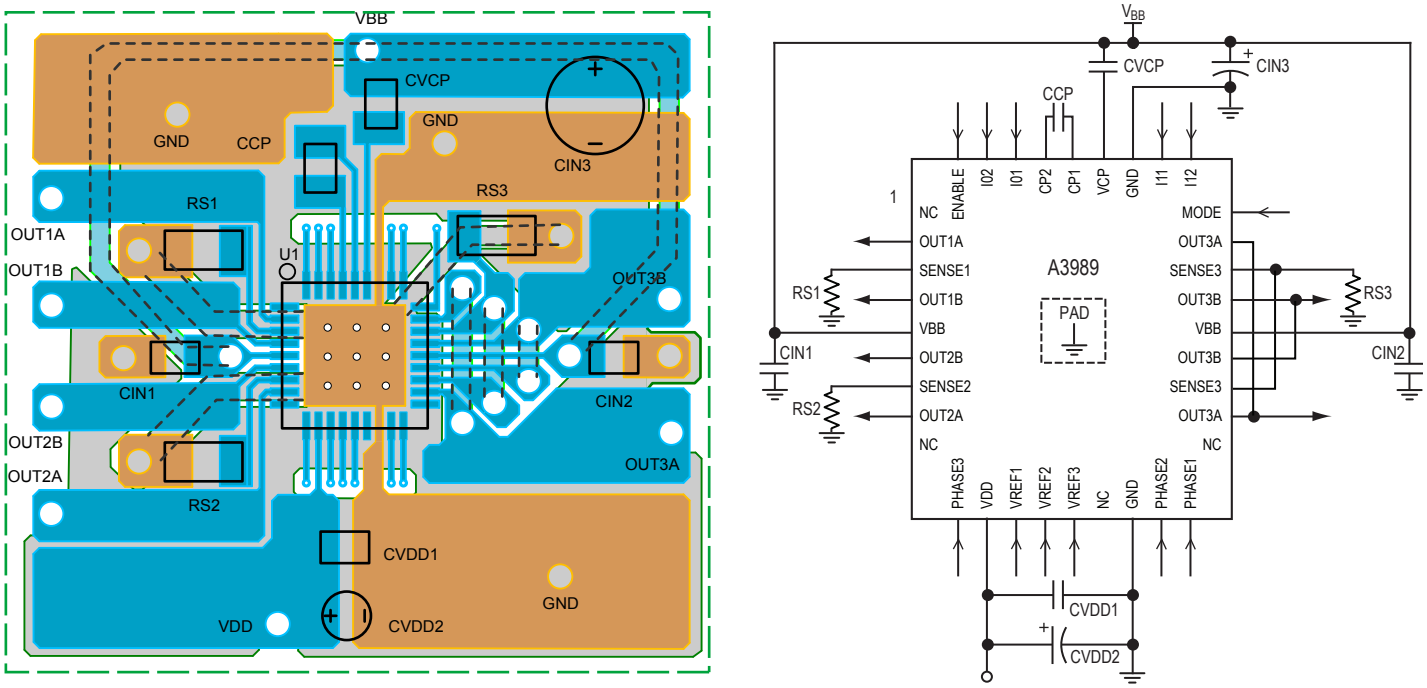
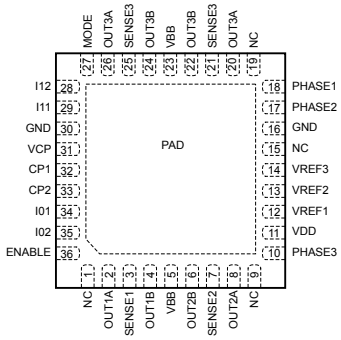


Figure 5. Printed circuit board layout with typical application circuit, shown at right. The copper area directly under the A3989 (U1) is soldered to the exposed thermal pad on the underside of the device. The thermal vias serve also as electrical vias, connecting it to the ground plane on the other side of the PCB , so the two copper areas together form the star ground.

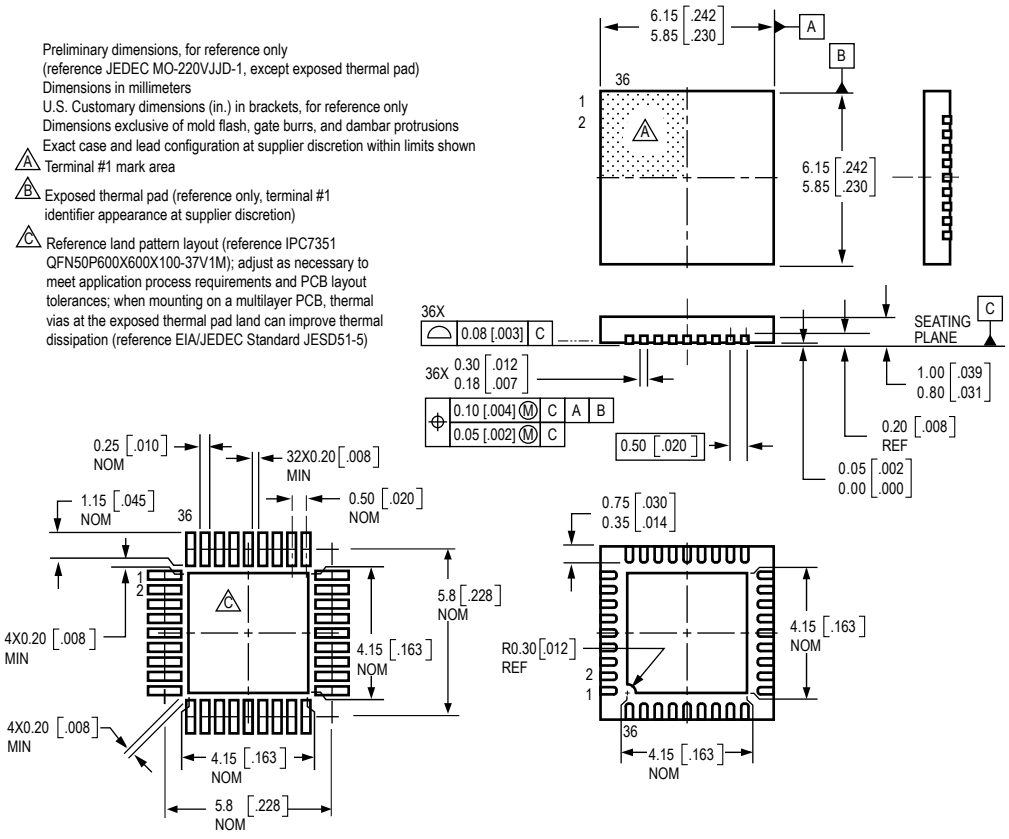
Pin-out Diagram



Terminal List Table

Number	Name	Description
1	NC	No Connect
2	OUT1A	DMOS Full Bridge 1 Output A
3	SENSE1	Sense Resistor Terminal for Bridge 1
4	OUT1B	DMOS Full Bridge 1 Output B
5	VBB	Load Supply Voltage
6	OUT2B	DMOS Full Bridge 2 Output B
7	SENSE2	Sense Resistor Terminal for Bridge 2
8	OUT2A	DMOS Full Bridge 2 Output A
9	NC	No Connect
10	PHASE3	Control Input
11	VDD	Logic Supply Voltage
12	VREF1	Analog Input
13	VREF2	Analog Input
14	VREF3	Analog Input
15	NC	No Connect
16	GND	Ground
17	PHASE2	Control Input
18	PHASE1	Control Input
19	NC	No Connect
20	OUT3A	DMOS Full Bridge 3 Output A
21	SENSE3	Sense Resistor Terminal for Bridge 3
22	OUT3B	DMOS Full Bridge 3 Output B
23	VBB	Load Supply Voltage
24	OUT3B	DMOS Full Bridge 3 Output A
25	SENSE3	Sense Resistor Terminal for Bridge 3
26	OUT3A	DMOS Full Bridge 3 Output B
27	MODE	Control Input
28	I12	Control Input
29	I11	Control Input
30	GND	Ground
31	VCP	Reservoir Capacitor Terminal
32	CP1	Charge Pump Capacitor Terminal
33	CP2	Charge Pump Capacitor Terminal
34	I01	Control Input
35	I02	Control Input
36	ENABLE	Control Input
–	PAD	Exposed pad for enhanced thermal performance. Should be soldered to the PCB

EV Package, 36 Pin QFN with Exposed Thermal Pad



The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copyright© 2006 AllegroMicrosystems, Inc.

For the latest version of this document, visit our website:
www.allegromicro.com