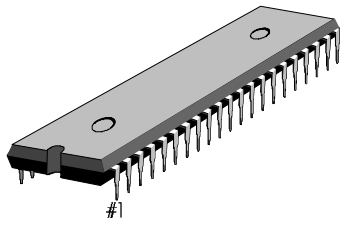
## DEFLECTION PROCESSOR

The S1D2147A01is a monolithic integrated circuit assembled in a 42 pins shrunk dual in line plastic package.
The goal of this IC is to control all the functions related to the horizontal and vertical deflection in multimodes or multisync monitors.

42-SDIP-600




## FUNCTIONS

- Positive or Negative sync polarities
- Auto-sync horizontal processing
- H-PLL lock/unlock identification
- Auto-sync Vertical processing
- East/West signal processing block
- B+ controller
- Safety blanking output

## ORDERING INFORMATION

| Device | Package | Operation Temperature |
|---|---|---|
| S1D2147A01-A0B0 | 42-SDIP | 0 °C — 70°C |

## FEATURES

**(HORIZONTAL)**

- Dual Pll concept
- Self-adaptative (30 to 70kHz)
- X-ray protection input
- DC adjustable duty-cycle
- Internal 1st PLL lock/unlock information
- Wide range DC controlled H-position
- ON/OFF switch (for PWR management)
- Two H-drive polarities

**(VERTICAL)**

- Vertical ramp generator
- 50 to 120Hz AGC Loop
- DC controlled V-amp, V-pos, S-amp & S-centring
- ON/OFF Switch

**(B+ REGULATOR)**

- Internal PWM generator for B+ current mode step-up conveter
- DC adjustable B+ voltage
- Output pulse synchronised on horizontal frequency
- Internal MAX current limitation

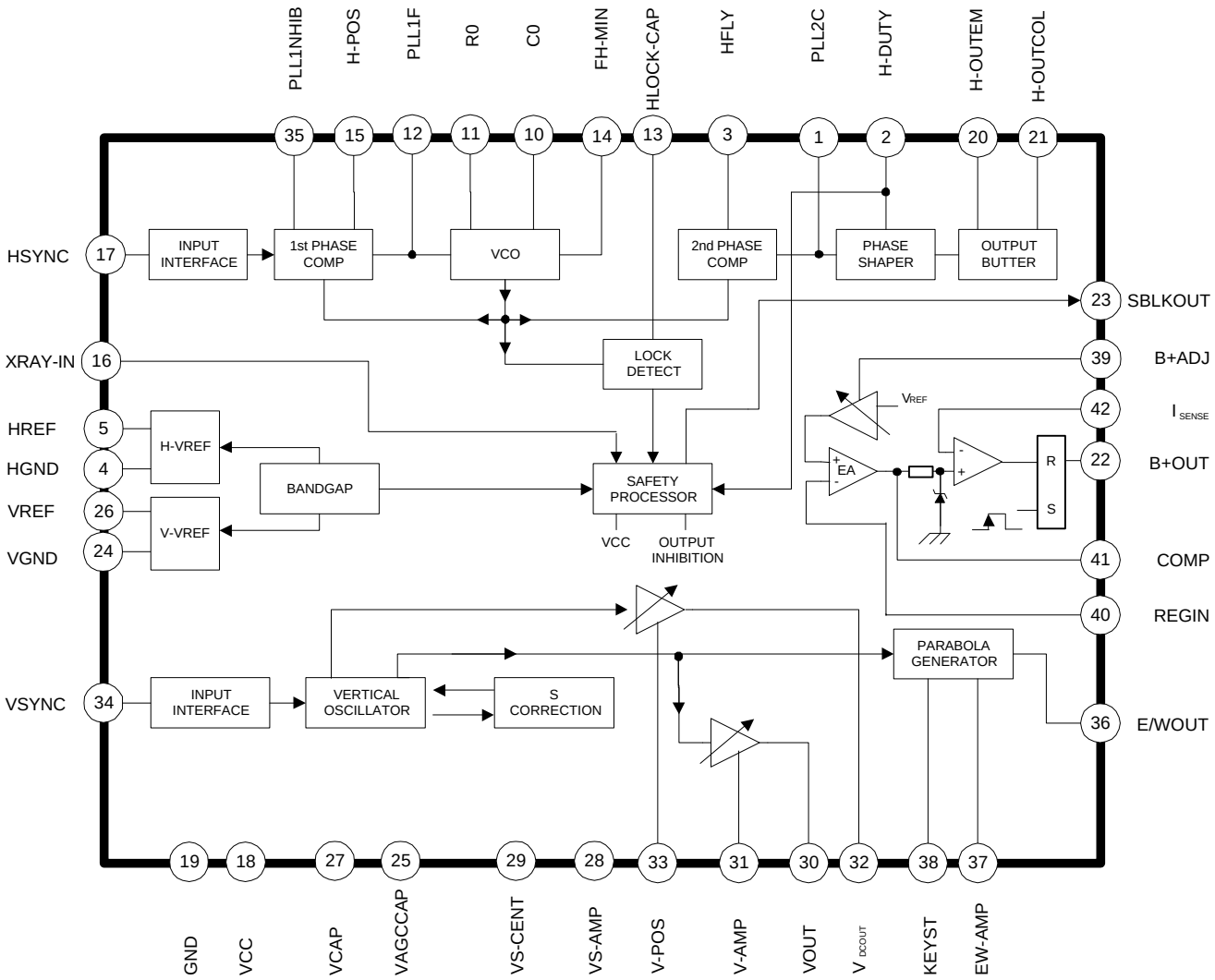
**(GENERAL)**

- Accept Positive or Negative Horizontal & Vertical sync polarities
- Separate H & V TTL input
- Safety blanking output

**($E_{WPCC}$)**

- Vertical parabola generator with DC
- controlled keystone & amplitude

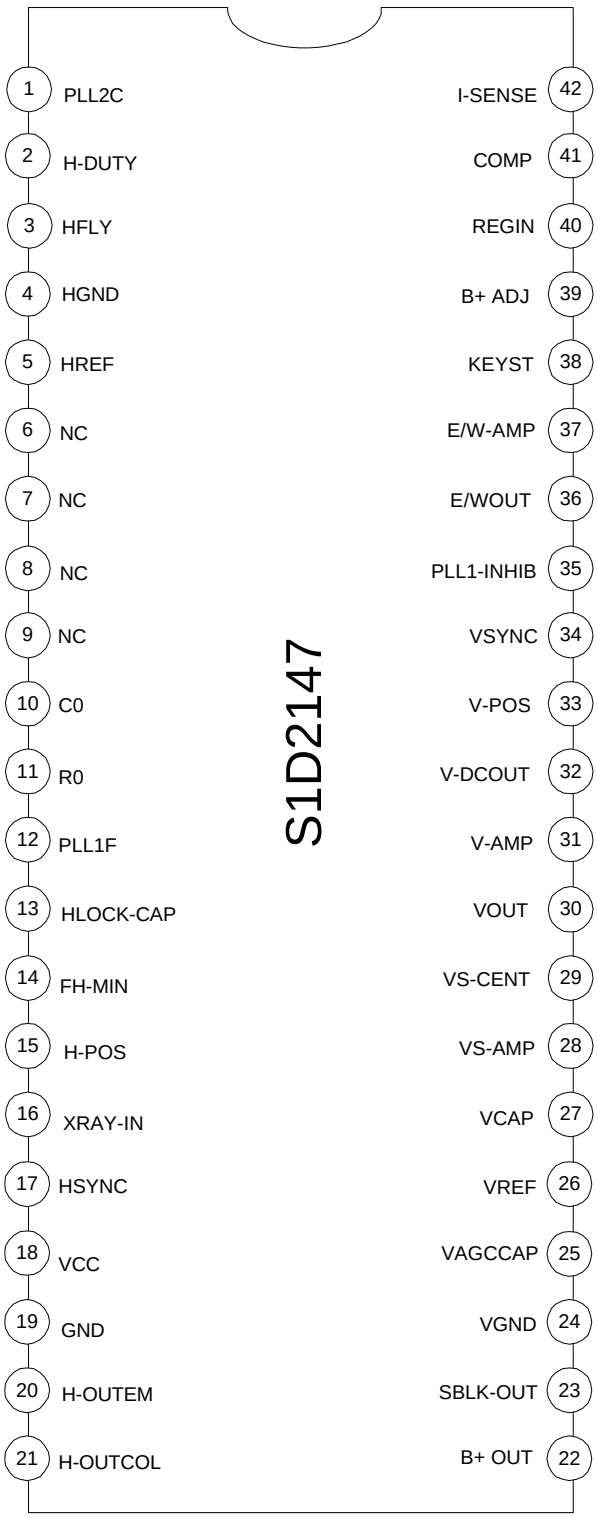
## BLOCK DIAGRAM






SAMSUNG ELECTRONICS

## PIN CONFIGURATIONS



## PIN DESCRIPTION

**Table 1. Pin Description**

| Pin No | Pin Name | Description |
|---|---|---|
| 1 | PLL2C | Second PLL Loop Filter |
| 2 | H-DUTY | DC Control of Horizontal Drive Output Pulse Duty-cycle.<br>If this pin grounded, the horizontal and vertical outputs are inhibited. By connecting a capacitor on the this pin a soft-start function may be realized on h-drive output. |
| 3 | H-FLY | Horizontal Flyback Input (Positive Polarity) |
| 4 | H-GND | Horizontal section ground. Must be connected only to components related to H blocks. |
| 5 | H-REF | Horizontal section reference voltage. Must be filtered by capacitor to pin 4. |
| 6 | NC | |
| 7 | NC | |
| 8 | NC | |
| 9 | NC | |
| 10 | C0 | Horizontal Oscillator Capacitor. To be connected to pin 4. |
| 11 | R0 | Horizontal Oscillator Resistor. To be connected to pin 4. |
| 12 | PLL1F | First PLL Loop filter. To be connected to pin 4. |
| 13 | HLOCK-CAP | First PLL Lock/Unlock Time Constant Capacitor. Capacitor filtering the freqency change detected on pin 13. When frequency is changing, a blanking pulse is generated on pin 23, the duration of this pulse is proportionnal to the capacitor on pin 13. To be connected to pin 4. |
| 14 | FH-MIN | DC Control for free running frequency setting. Comming from DAC output or DC voltage generated by a resistor bridge connected between pin 5 and 4. |
| 15 | H-POS | DC Control for Horizontal Centering |
| 16 | XRAY-IN | X-RAY Protection input (with Internal latch function) |
| 17 | H-SYNC | TTL Horizontal Sync Input |
| 18 | Vcc | Supply Voltage (12V Typical) |
| 19 | GND | Ground |
| 20 | H-OUTEM | Horizontal Drive Output (emiter of internal transistor) |
| 21 | H-OUTCOL | Horizontal Drive Output (open collector of internal transistor) |
| 22 | B+OUT | B+ PWM Regulator output |
| 23 | SBLK OUT | Safety Blanking output. Activated during frequency changes, when X-RAY input is triggered or when VS is too low. |
| 24 | VGND | Vertical Section Signal Ground |
| 25 | VAGCCAP | Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator |
| 26 | $V_{REF}$ | Vertical Section Reference Voltage |

**Table 1. Pin Description (Continued)**

| Pin No | Pin Name | Description |
|---|---|---|
| 27 | VCAP | Vertical Sawtooth Generator Capacitor |
| 28 | VS-AMP | DC Control of Vertical S-Shape Amplitude |
| 29 | VS-CENT | DC Control of Vertical S-Centering |
| 30 | V-OUT | Vertical Ramp Output (with frequency independant amplitude and S-Correction) |
| 31 | V-AMP | DC Control of Vertical Amplitude Adjustment |
| 32 | VDCOUT | Vertical Position Reference Voltage Output Temperature matched with V-AMP output |
| 33 | V-POS | DC Control of Vertical Position Adjustment |
| 34 | V-SYNC | Vertical TTL Sync Input |
| 35 | PLL1INHIB | TTL Input for PLL1 Output Current Inhibition (To be used in case of comp sync input signal) |
| 36 | E/WOUT | East/West Pincushion Correction Parabola Output |
| 37 | E/W-AMP | DC Control East/West Pincushion Correction Amplitude |
| 38 | KEYST | DC Control of Keystone Correction |
| 39 | B+ADJ | DC Control of B+ Adjustment |
| 40 | REGIN | Regulation Input of B+ Control Loop |
| 41 | COMP | B+ Error Amplifier Output for Frequency Compensation and Gain Setting |
| 42 | $I_{SENSE}$ | Sensing of External B+ Switching Transistor Emitter Current |

## ABSOLUTE MAXIMUM RATINGS

| NO | Item | Symbol | Spec | Unit |
|---|---|---|---|---|
| 1 | Supply Voltage (Pin 18) | $V_{CC}$ | 13.5 | V |
| 2 | Maximum Voltage on Pins 2, 14,15, 28, 29, 31, 33, 37, 38, 39<br>Pin 3<br>Pins 17, 34<br>Pin 40<br>Pin 42<br>Pin 16 | $V_{IN}$ | 8<br>1.8<br>6<br>8<br>8<br>6 | V |
| 3 | ESD Succeptibility<br>Human Body Model, 100pF Discharge through 1.5kΩ<br>EIAJ Norm, 200pF Discharge through 0Ω | VESD | <br>2<br>300 | <br>kV<br>V |
| 4 | Storage Temperature | $T_{stg}$ | -40, +150 | °C |
| 5 | Maximum Operating Junction Temperature | $T_j$ | 150 | °C |
| 6 | Operating Temperature | $T_{opr}$ | 0, +70 | °C |

## THERMAL CHARACTERISTICS

| NO | Item | Symbol | Spec | Unit |
|---|---|---|---|---|
| 1 | Junction-Ambient Thermal Resistance | θja | 65 | °C/W |

## HORIZONTAL SECTION

### OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCO** | | | | | | |
| Oscillator Resistor Min Value (Pin 11) | R0min | | 6 | | | kΩ |
| Oscillator Capacitor Min Value (Pin 10) | C0min | | 390 | | | pF |
| Maximum Oscillator Frequency | Fmax | | | | 70 | kHz |
| Horizontal Sync Input Voltage (Pin 17) | HsVR | | 0 | | 5.5 | V |
| **INPUT SECTION** | | | | | | |
| Minimum Input Pulses Duration (Pin 17) | MinD | | 1 | | | µS |
| Maximum Input Signal Duty Cycle (Pin 17) | Mduty | | | | 25 | % |
| **OUTPUT SECTION** | | | | | | |
| Maximum Input Peak Current (Pin 3) | I3m | | | | 2 | mA |
| Horizontal Drive Output Max Current<br>Pin 20<br>Pin 21 | <br>HOI1<br>HOI2 | <br>Sourced current<br>Sink current | | | <br>20<br>20 | <br>mA<br>mA |
| **DC CONTROL VOLTAGE** | | | | | | |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Voltage Range on DC Controls (Pins 2-14-15) | DCadj | $V_{REF-H}$ = 8V | 2 | | 6 | V |

## ELECTRICAL CHARACTERISTICS

(Vcc = 12 V, Tamb = 25 °C)

**Table 2. Horizontal Section Electrical Characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY AND REFERENCE VOLTAGES** | | | | | | |
| Supply Voltage (Pin 18) | $V_{CC}$ | | 10.8 | 12 | 13.2 | V |
| Supply Current (Pin 18) | $I_{CC}$ | See Figure 1 | | 40 | 60 | mA |
| Reference Voltage for Horizontal Section (Pin 5) | $V_{REF-H}$ | | 7.4 | 8 | 8.6 | V |
| Max Sourced Current on $V_{REF-H}$ (Pin 5) | $I_{REF-H}$ | | | | 2 | mA |
| Reference Voltage for Vertical Section (Pin 26) | $V_{REF-V}$ | | 7.4 | 8 | 8.6 | V |
| Max Sourced Current on $V_{REF-V}$ (Pin 26) | $I_{REF-V}$ | | | | 2 | mA |
| **INPUT SECTION/PLL1** | | | | | | |
| Horizontal Input Threshold Voltage (Pin 17) | $V_{INTH}$ | Low level voltage<br>High level voltage | <br>2 | | 0.8 | V |
| VCO Control Voltage (Pin 12) | $V_{VCO}$ | $V_{REF-H}$ = 8V | 1.6 to 6.2 | | | V |
| VCO Gain, dF/dV (Pin 12) | $V_{COG}$ | R0 = 6.49kΩ,<br>C0 = 680pF | | 15 | | kHz/V |
| Horizontal Phase Adjustment (Pin 15) | Hph | % of Horizontal period | | ±10 | | % |
| Free running frequency adjustment (pin 14) | FFadj | Without H-sync signal | | ±20 | | % |
| PLL1 Capture Range<br>Fh Min<br>Fh Max | CR | See conditions on Figure 1 | <br>70 | | 28 | <br>kHz<br>kHz |
| PLL 1 Inhibition (Pin 35)<br>PLL ON<br>PLL OFF | PLLinh | <br>$V_{35}$<br>$V_{35}$ | <br><br>2 | | 0.8 | <br>V<br>V |
| **SECOND PLL AND HORIZONTAL OUTPUT SECTION** | | | | | | |
| Flyback Horizontal Threshold Voltage (Pin 3) | FBth | | 0.65 | 0.75 | | V |
| Horizontal Jitter | Hjit | | | 150 | | ppm |
| Horizontal Drive Output Duty-cycle (Pin 20 or 21)<br>Minimum<br>Maximum | HDmin HDmax | <br>$V_2$ = 2V<br>$V_2$ = 2V | <br><br>45 | <br>30<br>50 | <br>35 | <br>%<br>% |
| Horizontal Drive Low Level Output Voltage | HDvd | Pin 20 to GND,<br>$V_{21}$-$V_{20}$, $I_{OUT}$ = 20mA | | 1.1 | 1.7 | V |

**Table 2. Horizontal Section Electrical Characteristics (Continued)**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Horizontal Drive High Level Output Voltage (output on Pin 20) | HDem | Pin 21 to $V_{CC}$, $I_{OUT}$ = 20mA | 9.5 | 10 | | V |
| X-RAY Protection Input Threshold Voltage (Pin 16) | XRAYth | | | 1.6 | 1.8 | V |
| Maximum Output Current on Safety Blanking Output | ISblkO | $I_{23}$ | | | 10 | mA |
| Low-Level Voltage on Safety Blanking output | VSblkO | $V_{23}$ with $I_{23}$ = 10mA | | 0.25 | 0.5 | V |
| Internal Clamping Voltage on 2nd PLL Loop Filter Output (Pin 1) | Vphi2 | Vmin<br>Vmax | | 1.6<br>3.2 | | V |
| Pin2 Threshold Voltage to Stop H-out, V-out<br>B+out and to Activate S-BLK<br>(OFF Mode when $V_2 < V_{OFF}$) | $V_{OFF}$ | $V_2$ | | 1 | | V |

## VERTICAL SECTION

### OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Vertical Sync Input Voltage (Pin 34) | VSVR | | 0 | | 5.5 | V |

### ELECTRICAL CHARACTERISTICS

(VCC = 12V, Tamb = 25 °C)

**Table 3. Vertical Section Electrical Characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Pin 23-28-29 bias current<br>(Currnt sourced by PNP base) | IBIASP | For V23-28-29 = 2V | | 2 | | °C |
| Pin 31 bias Current<br>(Current sunk by PNP base) | IBIASN | For V31 = 6V | | 0.5 | | °C |
| Vertical sync input threshold voltage | VSth | Pin 34; High-level<br>Low -level | 2 | | <br>0.8 | V<br>V |
| Vertical sync input bias current<br>(Current sourced by PNP base) | VSBI | V34 = 0.8V | | 1 | | µA |
| Voltage at ramp bottom point | VRB | On Pin 27 | | 2/8 | | VREF-V |
| Voltage at ramp top point (with sync) | VRT | On Pin 27 | | 5/8 | | VREF-V |
| Voltage at ramp top point (without sync) | VRTF | On Pin 27 | | VRT-0.1 | | V |

**Table 3. Vertical Section Electrical Characteristics (Continued)**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output current range on pin 27 during ramp charging time. Current to charge capacitor between pin 27 and ground | IR27 | V28 = 2V (2), 2V < V27 < 5V<br>Min current<br>Max current | <br><br>100 | <br><br>15<br>135 | <br><br>20 | <br><br>µA<br>µA |
| Minimum Vertical sync pulse width | VSW | Pin 34 | 5 | | | µS |
| Vertical sync input maximum duty-cycle | VSmDut | Pin 34 | | | 15 | % |
| Vertical Sawtooth discharge time duration | VSTD | On pin 27, with 150nF cap | | 85 | | µS |
| Vertical Free running frequency ( V28 = 2V ) | VFRF | Measured on pin 27<br>Cosc (pin 27) = 150nF | | 100 | | Hz |
| AUTO-SYNC frequency see (3) | ASFR | With C27 = 150nF ±5% | 50 | | 120 | Hz |
| Ramp Amplitude Thermal Drift | RATD | On pin 30 see (1)<br>(0°C < Tamp < 70°C ) | | 100 | | ppm/ °C |
| Ramp Amplitude Drift Versus Frquency | RAFD | V31 = 6V, C27 = 150nF<br>50Hz < F < 120Hz | | 200 | | ppm/ Hz |
| Ramp Linearity on Pin 27 127 / I27 | RIin | V28 = 2V, V25 = X = 4.3V<br>2.5V < V27 < 4.5V | | 0.5 | | % |
| Minimum Load on Pin 25 for less than 1% Vertical Amplitude Drift | RIoad | | 50 | | | kΩ |
| Vertical Position Adjustment Votlage on pin 32 | Vpos | V33 = 2V<br>V33 = 4V<br>V33 = 6V | <br><br>3.65 | 3.2<br>3.5<br>3.8 | 3.3 | V<br>V<br>V |
| Max Current on Vertical Position Control output (pin32) | IVPOS | | | ±2 | | mA |
| Vertical Output Votlage (on pin 30) (peak to peak voltage on pin 30) | Vor | V31 = 2V<br>V31 = 4V<br>V31 = 6V | <br><br>3.75 | 2<br>3<br>4 | 2.2 | V<br>V<br>V |
| DC Votlage on Vertical Output (pin 30) | VOUTDC | See (4) | | 7/16 | | VREF-V |
| Vertical output maximum output current | V0I | On Pin 30 | | ±5 | | mA |
| Max vertical S-Correction Amplifitude (V28 = 2V inhibits S-CORR; V28 = 6V gives maximum S-CORR) (see figure 3) | dVS | ΔV/V30pp at T/4<br>ΔV/V30pp at 3T/4 | | -4<br>+4 | | %<br>% |
| C-Correction adjustment range voltage on pin 27 for maximum slope on the ramp (with S-Correstion ) (see figure 4) | Ccorr | V29 = 2V<br>V29 = 4V<br>V29 = 6V | | 3<br>3.5<br>4 | | V<br>V<br>V |

## B+ SECTION

### OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum Error Amplifier Output Current | EAOI | Source by pin 14<br>Sunk by pin 41 | | | 0.5<br>2 | mA<br>mA |
| Minimum Feedback Resistor | FeedRes | Resistor between pins 40 and 41 | 5 | | | kΩ |

### ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 12V, Tamb = 25 °C)

**Table 4. B+ Section Electrical Characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error Amplifier Open loop gain | OLG | At low frequency<br>see (1) | | 85 | | dB |
| Unity gain bandwidth | UGBW | see (1) | | 6 | | MHz |
| Regulation input bias current | IRI | Current sourced by pin 40 (PNP base) | | 0.2 | | µA |
| Maximum guaranted error amplifier output current | EAOI | Current sourced by pin 41<br>Current sink by pin 41 | 0.5<br>2 | | | mA<br>mA |
| Current Sense Input Voltage Gain | CSG | Pin 42 | | 3 | | |
| Max Current Sense Input Threshold Votlage | MCEth | Pin 42 | | 1.2 | | V |
| Current Sense Input Bias Current | ISI | Current sunk by pin 42 (NPN base) | | 1 | | µA |
| Maximum External Power Transistor on Time | Tonmax | % of H-period @ f0 = 27kHz | | 75 | | % |
| B+ Output Low Level Saturation voltage | B+OSV | $V_{22}$ with $I_{22}$ = 10mA | | 0.25 | | V |
| Internal Reference voltage | IVref | On error amp (+) input for $V_{39}$ = 4V | | 4.9 | | V |
| Internal Reference Voltage Adjustment | $V_{RERADJ}$ | 2V < V39 < 6V | | ±14 | | % |

## EAST/WEST PARABOLA GENERATOR

### ELECTRICAL CHARACTERISTICS

(VCC = 12V, Tamb = 25 °C)

**Table 5. East/West Parabola Generator Electrical Characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Parabola symetry adjustment capability (for Keystone adjustment; with pin 38) | Vsym | See figure 2; Internal voltage<br>V38 = 2V<br>V38 = 4V<br>V38 = 6V | | <br><br>3.2<br>3.5<br>3.8 | | V |

**Table 5. East/West Parabola Generator Electrical Characteristics (Continued)**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Keystone adjustment capability<br>B/A ratio<br>A/B ratio | Kadj | See figure 2; V37 = 4V<br>V38 = 2V<br>V38 = 6V | | <br>2.3<br>2.0 | | |
| Parabola amplitude adjustment capability<br>Maximum amplitude on pin 36<br>Maximum ratio between max and min | Paramp | V38 = 4.3V, V28 = 2V<br>V37 = 2V<br>2V < V37 < 6V | <br>3.3<br>2.4 | <br>3.8<br>3 | <br>4.3 | V |

**NOTES:**

1. These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from comers of our processes and also temperature characterization.
2. When 2V are applied on pin 28 (Vertical S-Correction control), then the S-Correction is inhibited, consequently the sawtooth have a linear shape.
3. It is the frequency range for which the VERTICAL OSCILLATOR will automatically synchorize, using a single capacitor value on Pin 27 and with a constant ramp amplitude.
4. Typically 3.5V for vertical reference voltage typical value (8V).

## APPLICATION CIRCUIT

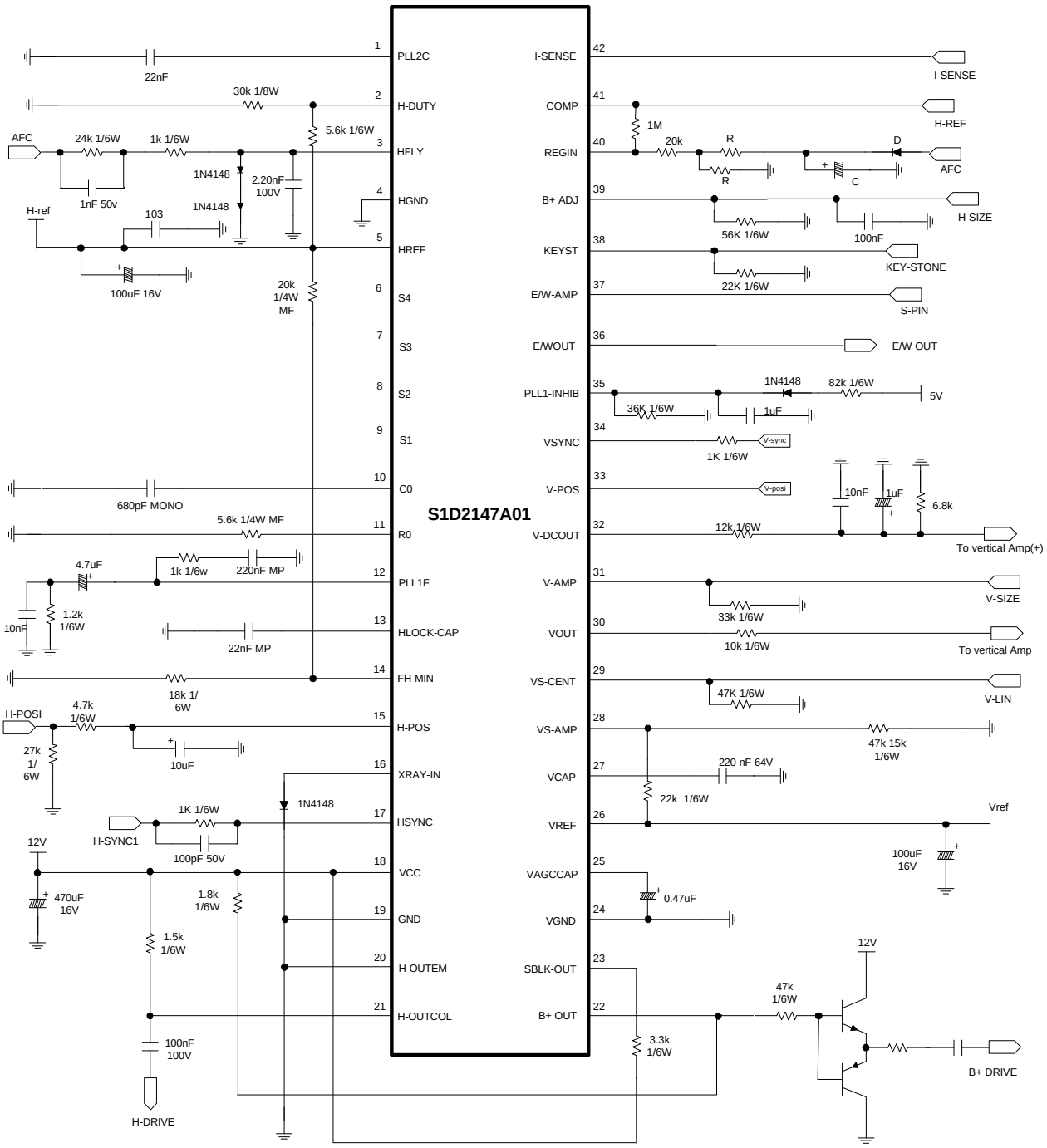



**Figure 1. Application Circuit**

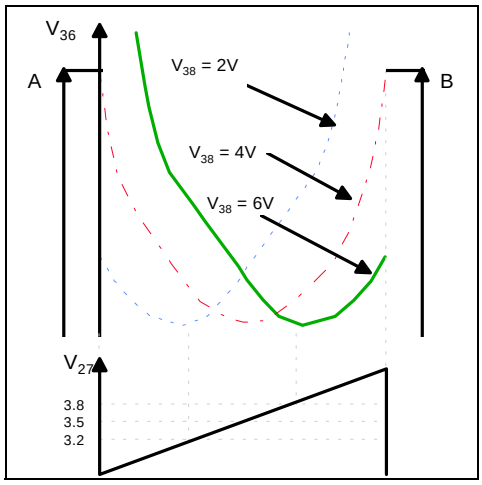



**Figure 2. Keystone Adjusment**

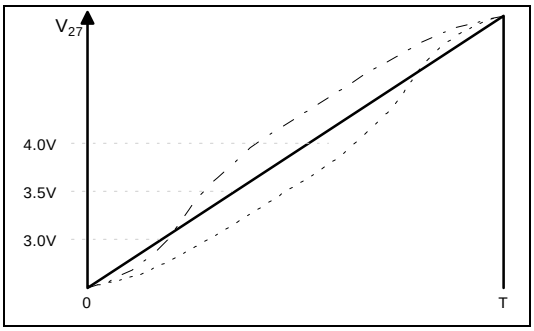



**Figure 3. Amplitude Adjusment**

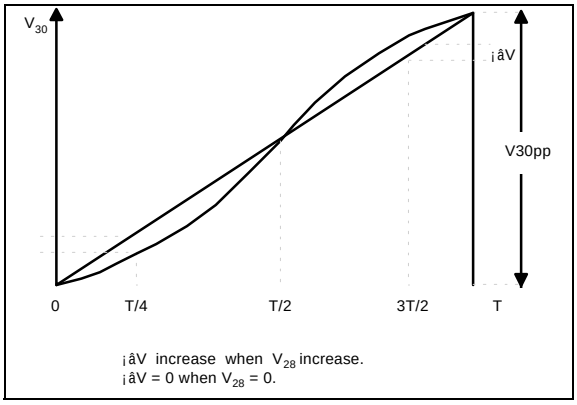



**Figure 4. Correction Adjusment**