P4C165
ULTRA HIGH SPEED 8K x 8
RESETTABLE STATIC CMOS RAM

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  – 15/20/25 ns (Commercial)
  – 20/25/35 (Industrial)
- **Low Power Operation**
- **Chip Clear Function**
- **Output Enable and Dual Chip Enable Control Functions**
- **Single 5V±10% Power Supply**
- **Common Data I/O**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  – 28-Pin Plastic DIP (300 mil)

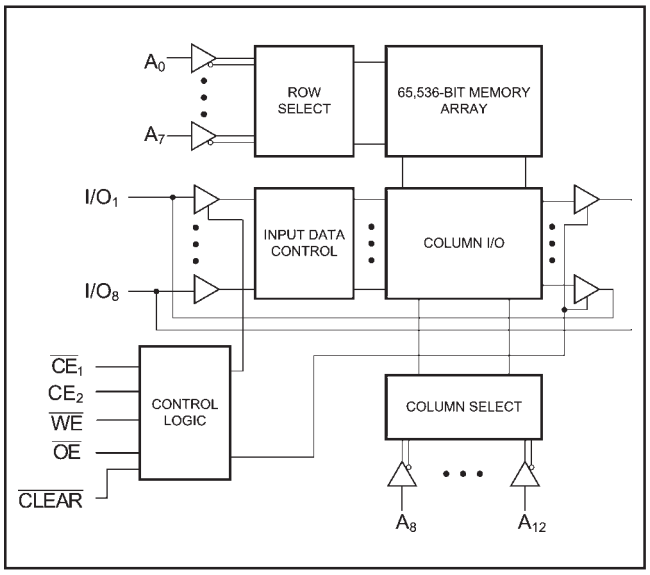
DESCRIPTION

The P4C165 is a 65,536-bit ultra high-speed static RAM organized as 8K x 8. The RAM features a reset control to enable clearing all words to zero within two cycle times. The CMOS memory requires no clocks or refreshing and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

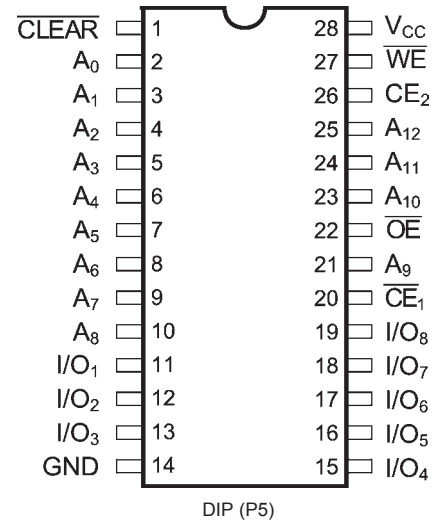
Access times as fast as 15 nanoseconds are available, permitting greatly enhanced system operating speeds. In full standby mode with CMOS inputs, power consumption is only 5.5 mW for the P4C165.

The P4C165 is available in a 28-pin 300 mil DIP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP (P5)

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade(2)	Ambient Temperature	GND	V_{cc}
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	–40°C to +85°C	0V	5.0V ± 10%

CAPACITANCES[4]

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C165 Min	P4C165 Max	Unit
V_{IH}	Input High Voltage			2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage			–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC} –0.2	V_{CC} +0.5	V
V_{LC}	CMOS Input Low Voltage			–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.			0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	Ind./Com'l.	–5	+5	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Ind./Com'l.	–5	+5	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ or $CE_2 \leq V_{IL}$, V_{CC}= Max f = Max., Outputs Open	Ind./Com'l.	——	30	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$ or $CE_2 \leq V_{LC}$, V_{CC}= Max f = 0, Outputs Open $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Ind./Com'l.	——	15	mA

n/a = Not Applicable

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	–15	–20	–25	–35	Unit
I_{CC}	Dynamic Operating Current*	Commercial	160	155	150	N/A	mA
		Industrial	N/A	160	155	150	mA

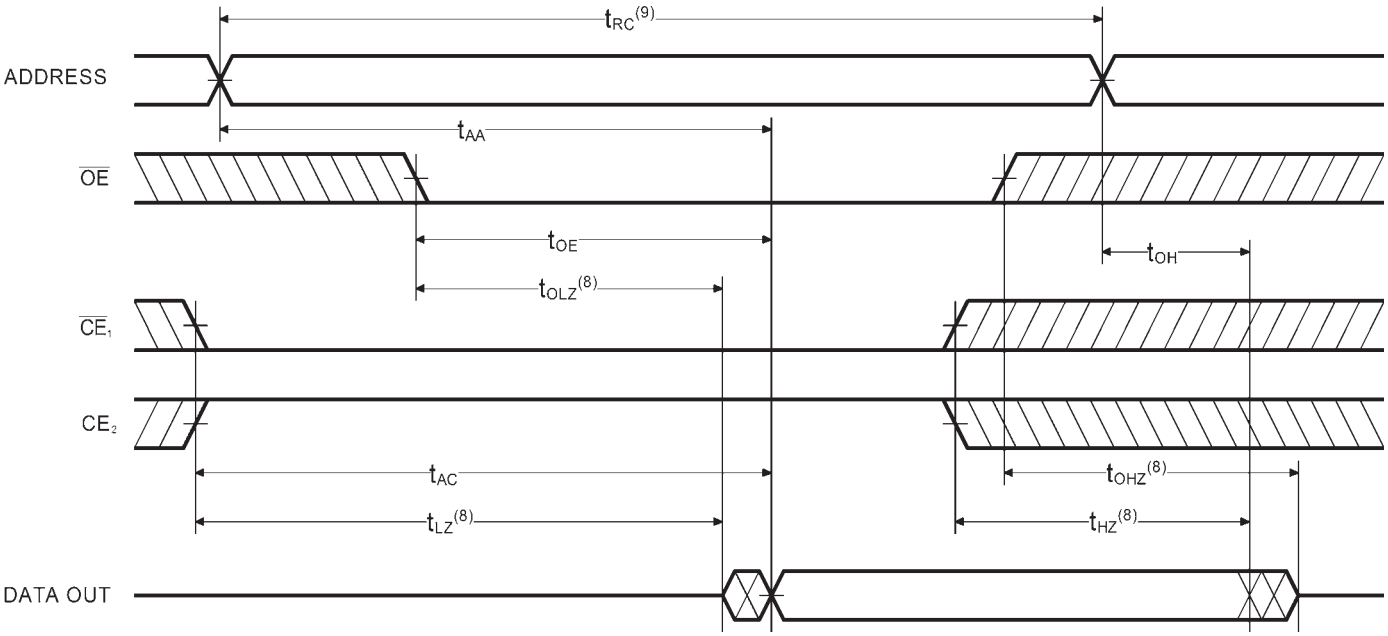
*V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}, $\overline{OE}$ = V_{IH}

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

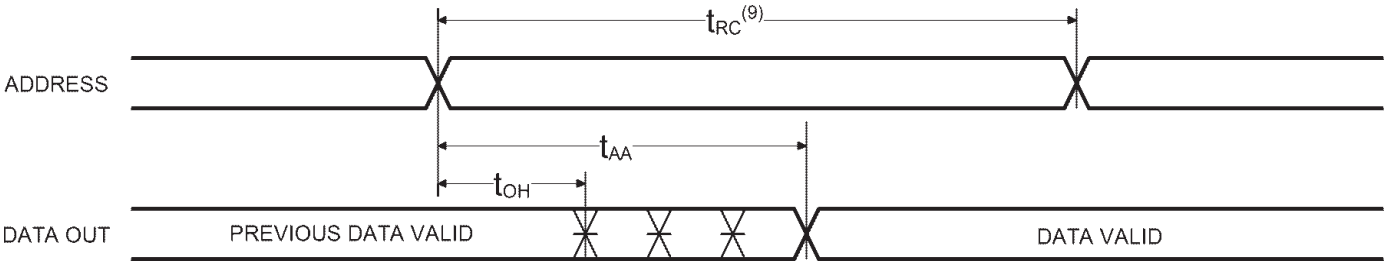
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address Access Time		15		20		25		35	ns
t_{AC}	Chip Enable Access Time		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		8		8		10		15	ns
t_{OE}	Output Enable Low to Data Valid		9		10		13		18	ns
t_{OLZ}	Output Enable Low to Low Z	2		2		2		2		ns
t_{OHZ}	Output Enable High to High Z		9		9		12		15	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		15		20		20		20	ns

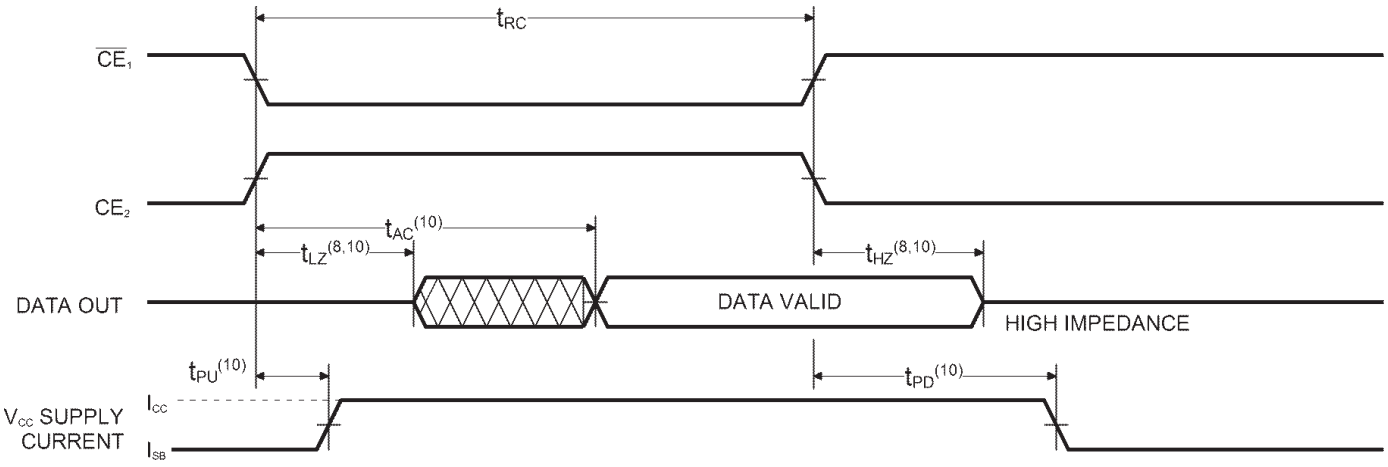
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,6]



READ CYCLE NO. 3 ($\overline{CE}_1$, CE_2 CONTROLLED)[5,7,10]



Notes:

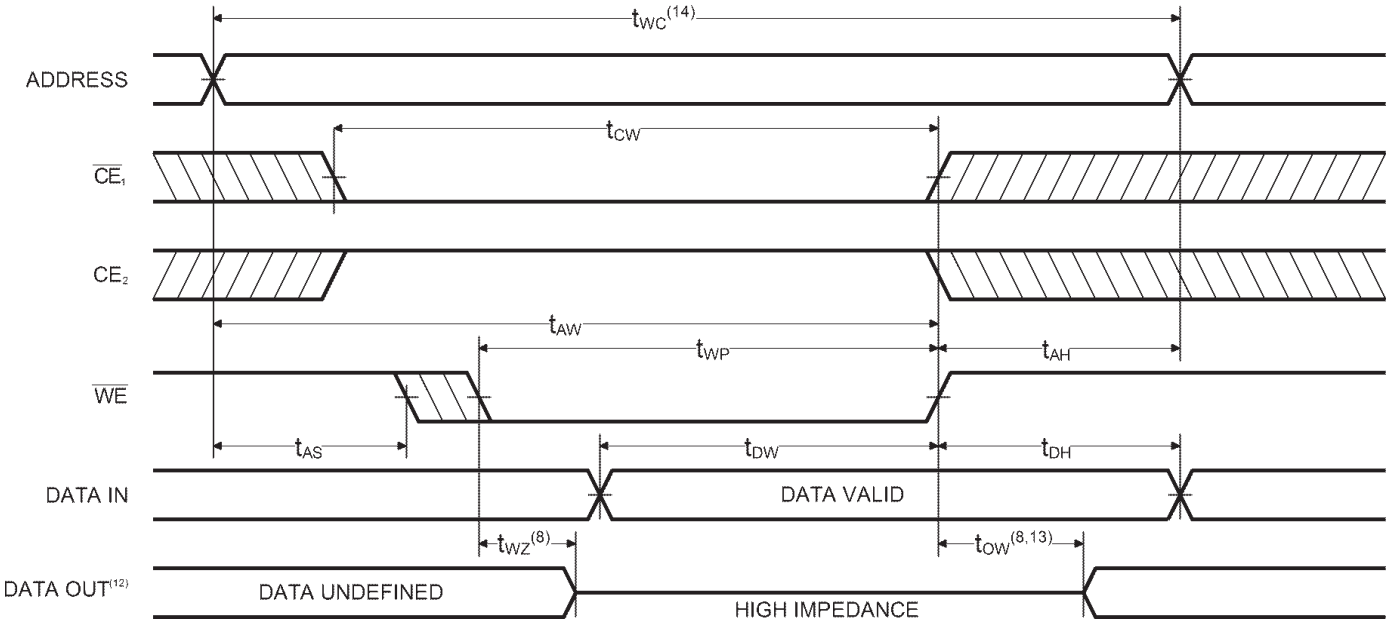
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. READ Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		25		35		ns
t_{CW}	Chip Enable Time to End of Write	12		15		18		25		ns
t_{AW}	Address Valid to End of Write	12		15		18		25		ns
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	12		15		18		20		ns
t_{AH}	Address Hold Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	9		11		13		15		ns
t_{DH}	Date Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		8		10		14	ns
t_{OW}	Output Active from End of Write	3		3		3		3		ns

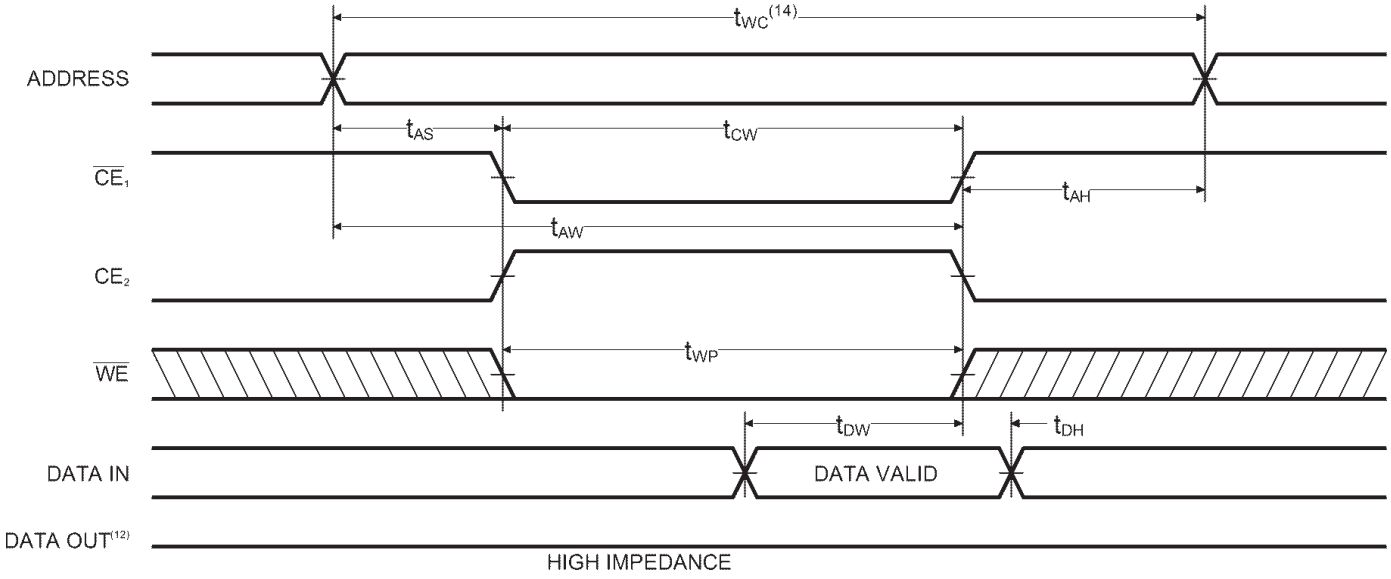
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[11]



Notes:

11. $\overline{CE_1}$ and $\overline{WE}$ must be LOW, and CE_2 HIGH for WRITE cycle.
12. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE_1}$ goes HIGH, or CE_2 goes LOW, simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[11]

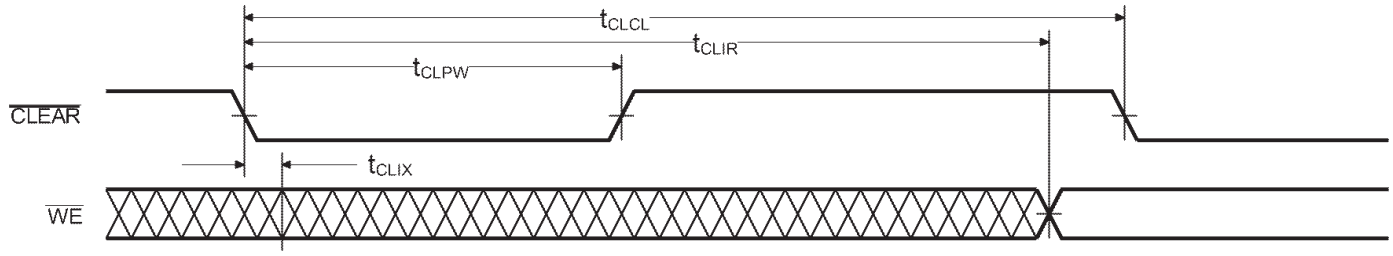


AC CHARACTERISTICS—CLEAR CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLCL}	$\overline{CLEAR}$ Cycle Time	30		40		50		70		ns
t_{CLPW}	$\overline{CLEAR}$ Pulse Width	12		15		15		20		ns
t_{CLIX}	$\overline{CLEAR}$ Low to Inputs Don't Care	0		0		0		0		ns
t_{CLIR}	$\overline{CLEAR}$ Low to Inputs Recognized		30		40		50		70	ns

TIMING WAVEFORM OF $\overline{CLEAR}$ CYCLE



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CLEAR}$	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Reset	L	X	X	X	X	---	Active
Standby	H	H	X	X	X	High Z	Standby
Standby	H	X	L	X	X	High Z	Standby
Output Disabled	H	L	H	H	H	High Z	Active
Read	H	L	H	L	H	D_{OUT}	Active
Write	H	L	H	X	L	High Z	Active

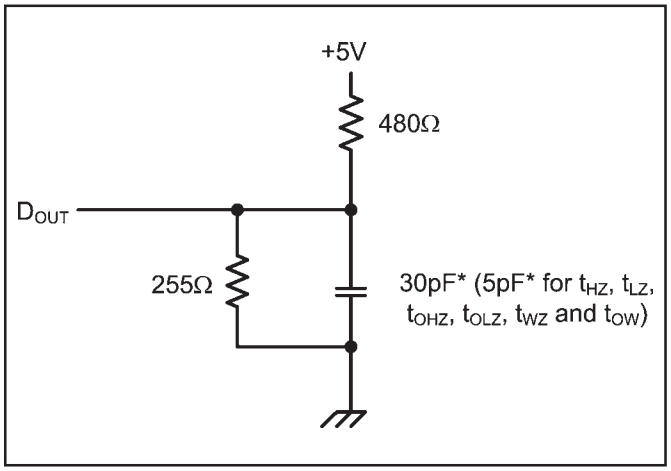


Figure 1. Output Load

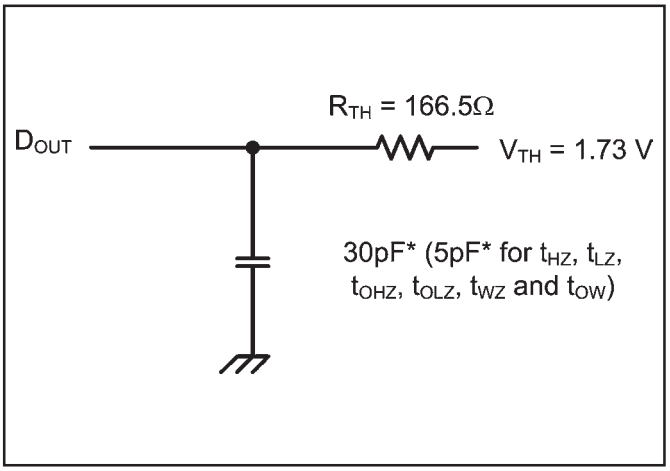


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C165, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION

P4C165 — xx x x

- P4C165 — Device Type
- xx — Speed
  - 15, 20, 25, 35 ns
- x — Package
  - P — Plastic DIP, 300 mil
- x — Processing
  - C — 0°C to +70°C
  - I — -40°C to +85°C

8K x 8 RESETTABLE SRAM

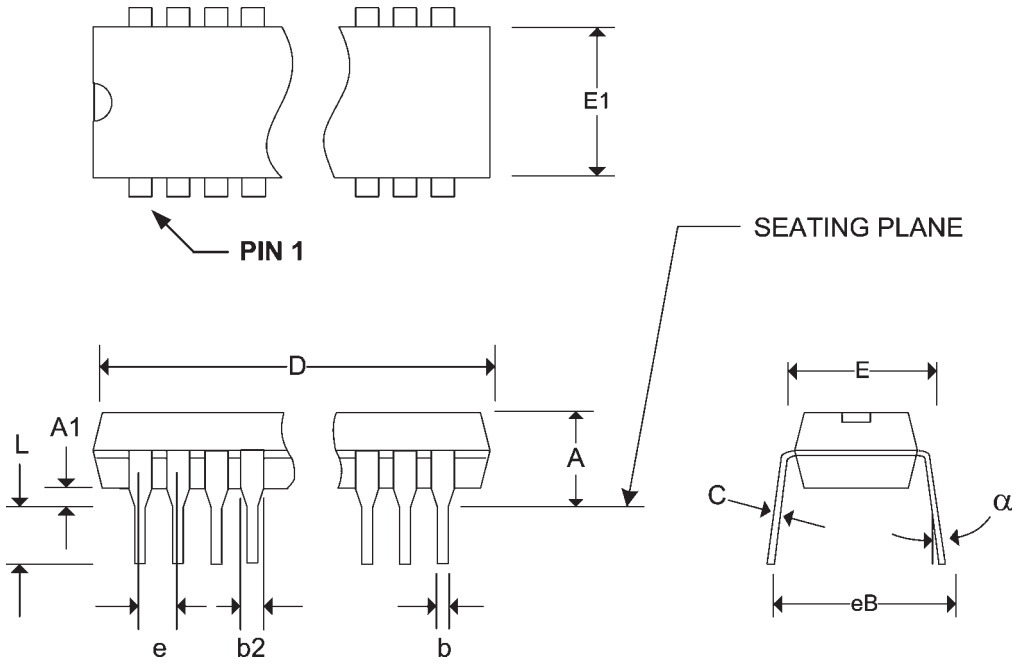
SELECTION GUIDE

The P4C165 is available in the following temperature, speed and package options.

Temperature Range	Package	Speed			
		15	20	25	35
Commercial	Plastic DIP	-15PC	-20PC	-25PC	-35PC
Industrial	Plastic DIP	-15PI	-20PI	-25PI	-35PI

Pkg #	P5	
# Pins	28 (300 mil)	
Symbol	Min	Max
A	-	0.210
A1		-
b	0.014	0.023
b2	0.045	0.070
C	0.008	0.014
D	1.345	1.400
E1	0.270	0.300
E	0.300	0.380
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



REVISIONS

DOCUMENT NUMBER: SRAM117
DOCUMENT TITLE: P4C165 ULTRA HIGH SPEED 8K x 8 RESETTABLE STATIC CMOS RAM

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	Oct-05	JDB	New Data Sheet