FAIRCHILD SEMICONDUCTOR®

May 2001

FM24C128 – 128K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

FM24C128 is a 128Kbit CMOS non-volatile serial EEPROM organized as 16K x 8 bit memory. This device confirms to Extended IIC 2-wire protocol that allows accessing of memory in excess of 16Kbit on an IIC bus. This serial communication protocol uses a Clock signal (SCL) and a Data signal (SDA) to synchronously clock data between a master (e.g. a microcontroller) and a slave (EEPROM). FM24C128 is designed to minimize pin count and simplify PC board layout requirements.

FM24C128 offers hardware write protection where by the entire memory array can be write protected by connecting WP pin to V_{CC}. The entire memory then becomes unalterable until the WP pin is switched to V_{SS}.

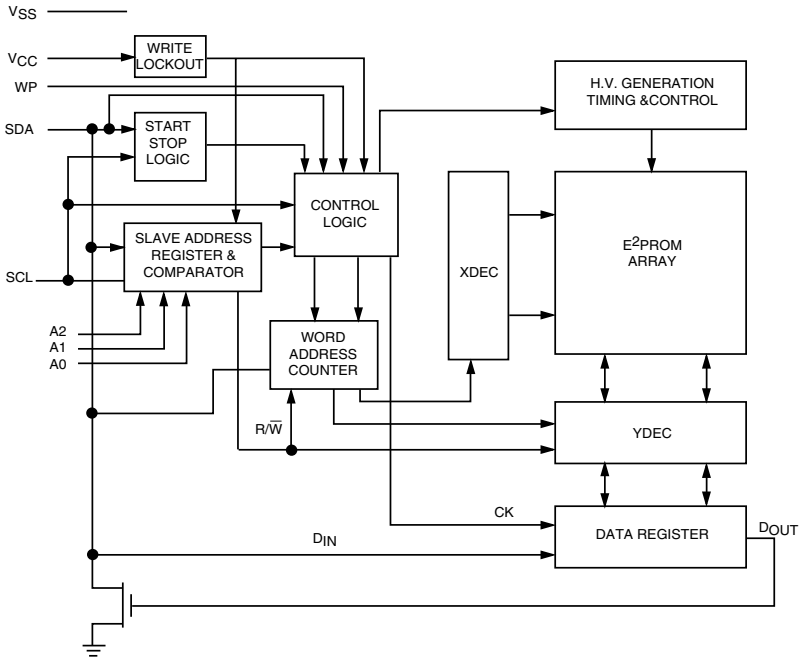
"LZ" and "L" versions of FM24C128 offer very low standby current making them suitable for low power applications. This device is offered in SO, TSSOP and DIP packages.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

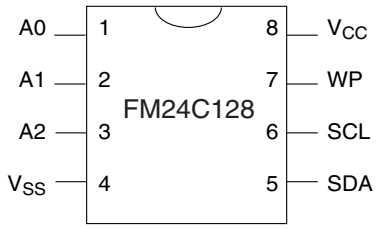
- Extended operating voltage: 2.5V to 5.5V
- Up to 400 KHz clock frequency at 2.5V to 5.5V
- Low power consumption
  - —0.5mA active current typical
  - —10μA standby current typical
  - —1μA standby current typical (L version)
  - —0.1μA standby current typical (LZ version)
- Schmitt trigger inputs
- 64 byte page write mode
- Self timed write cycle (6ms max)
- Hardware Write Protection for the entire array
- Endurance: up to 100K data changes
- Data Retention: Greater than 40 years
- Packages: 8-Pin DIP, 8-Pin SO and 8-Pin TSSOP
- Temperature range
  - —Commercial: 0°C to +70°C
  - —Industrial (E): -40°C to +85°C
  - —Automotive (V): -40°C to +125°C

Block Diagram



Connection Diagram

Dual-in-Line Package (N), SO Package (MW8) and TSSOP Package (MT8)

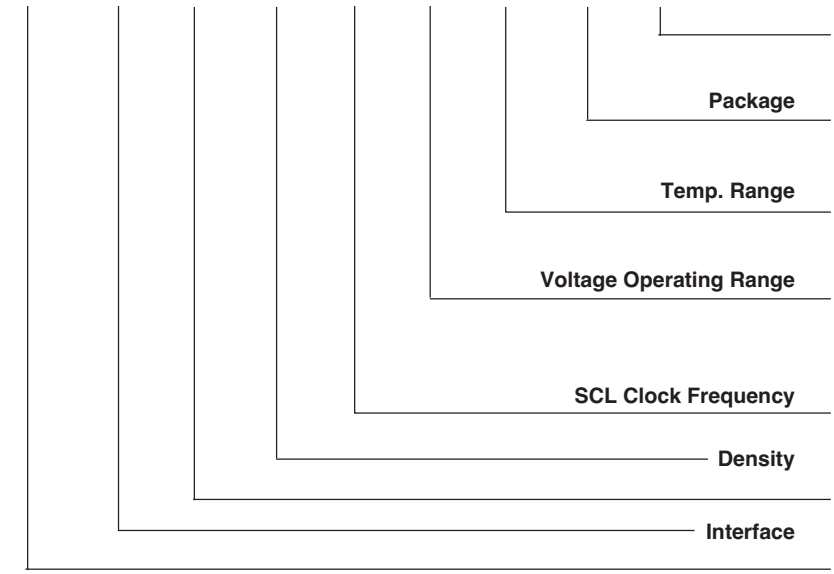


See Package Number N08E, M08D and MTC08

Pin Names

V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
A0, A1, A2	Device Address Inputs

Ordering Information



	Letter	Description
	Blank	Tube
	X	Tape and Reel
Package	N	8-pin DIP
	MW8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	Blank	0 to 70°C
	E	-40 to +85°C
	V	-40 to +125°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.5V to 5.5V
	LZ	2.5V to 5.5V and <1µA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	128	128K with write protect
	C	CMOS
Interface	24	IIC - 2 Wire
	FM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
FM24C128	0°C to +70°C
FM24C128E	-40°C to +85°C
FM24C128V	-40°C to +125°C
Positive Power Supply	
FM24C128	4.5V to 5.5V
FM24C128L	2.5V to 5.5V
FM24C128LZ	2.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz		0.5	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V

Low V_{CC} (2.5V to 5 .5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.5	1.0	mA
I_{SB} (Note 3)	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.5V - 4.5V (L)		1	10	µA
			V_{CC} = 2.5V - 4.5V (LZ)		0.1	1	µA
			V_{CC} = 4.5V - 5.5V		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

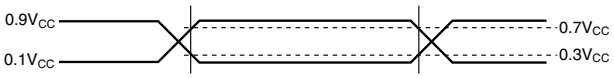
Note 2: This parameter is periodically sampled and not 100% tested.

Note 3: The "L" and "LZ" versions can be operated in the 2.5V to 5.5V V_{CC} range. However the I_{SB} values for L and LZ are applicable only when V_{CC} is in the 2.5V to 4.5V range.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms

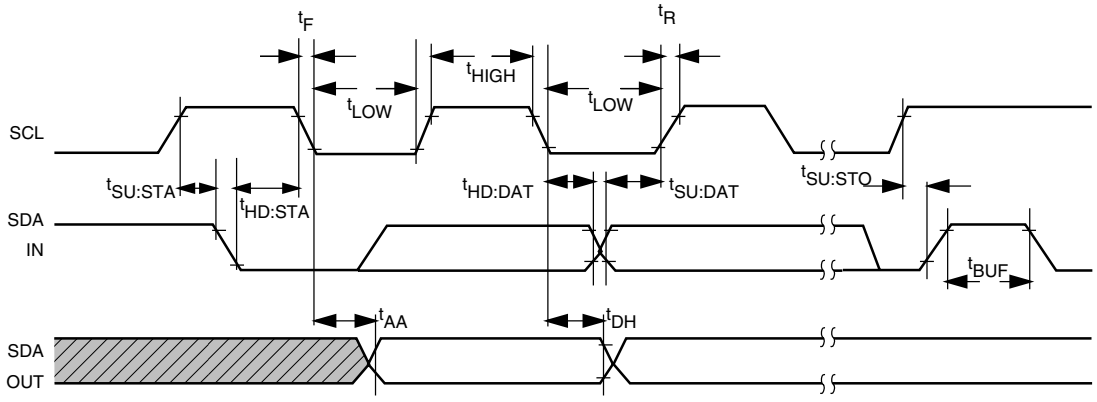


Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.5V - 5.5V)

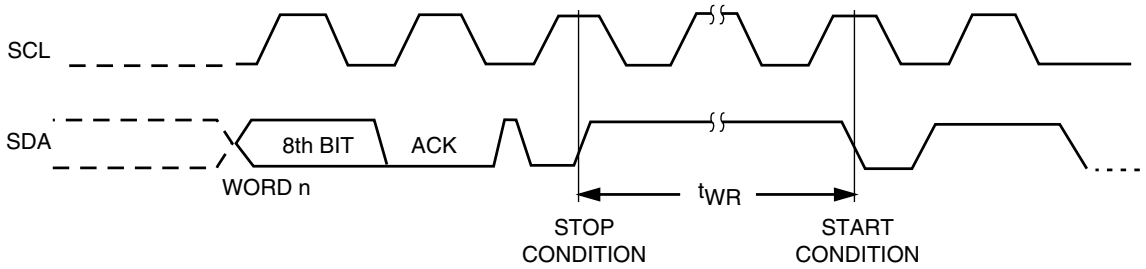
Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	250		120		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR}	Write Cycle Time		6		6	ms

Note 4: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the FM24C128 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address. Refer "Write Cycle Timing" diagram.

Bus Timing

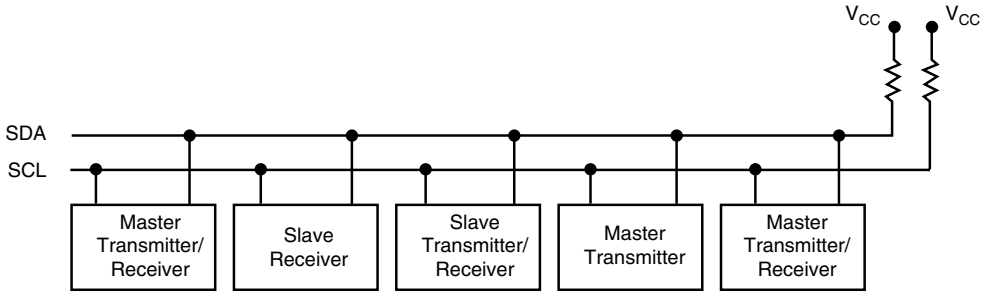


Write Cycle Timing



Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Typical System Configuration



Note: Due to open drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

Background Information (IIC Bus)

Extended IIC specification is an extension of Standard IIC specification to allow addressing of EEPROMs with more than 16Kbits of memory on an IIC bus. The difference between the two specifications is that Extended IIC specification defines two bytes of "Array Address" information while Standard IIC specification defines only one. All other aspects are identical between the two specifications. Using two bytes of Array Address and 3 address signals (A2, A1 and A0), it is now possible to address up to 4 Mbits ($2^8 * 2^8 * 2^3 * 8 = 4$ Mbits) of memory on an IIC bus.

Note that due to format difference, it is not possible to have peripherals which follow Standard IIC specification (e.g. 16K bit EEPROM) and peripherals which follow Extended IIC specification (e.g. 128K bit EEPROM) on a common IIC bus.

IIC bus allows synchronous bi-directional communication between a TRANSMITTER and a RECEIVER using a Clock signal (SCL) and a Data signal (SDA). Additionally there are up to three Address signals (A2, A1 and A0) which collectively serve as "chip select signal" to a device (e.g. EEPROM) on the bus.

All communication on the IIC bus must be started with a valid START condition (by a MASTER), followed by transmittal (by the MASTER) of byte(s) of information (Address/Data). For every byte of information received, the addressed RECEIVER provides a valid ACKNOWLEDGE pulse to further continue the communication unless the RECEIVER intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the RECEIVER can be a SLAVE or the MASTER. A typical IIC communication concludes with a STOP condition (by the MASTER).

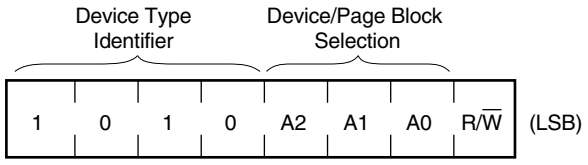
Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—[ARRAY ADDRESS#1]—[ARRAY ADDRESS#0]

Slave Address

Slave Address is an 8-bit information consisting of a Device type field (4bits), Device/Page block selection field (3bits) and Read/Write bit (1bit).

Slave Address Format



Device Type

IIC bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMS. Hence to properly identify various devices on the IIC bus, a 4-bit "Device Type" identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own "Device Type" string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g. multiple EEPROMS) are present on the IIC bus, then the A2, A1 and A0 address information bits are used in device selection. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A2, A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the "Device Type" comparison.

In addition to selecting an EEPROM, these 3 bits are also used to select a "page block" within the selected EEPROM. Each page block is 512Kbit (64 K Bytes) in size. If an EEPROM contains more than one page bock then the selection of a page block within the EEPROM is by using A2, A1 and A0 bits.

Read/Write Bit

Last bit of the Slave Address indicates if the intended access is Read or Write. If the bit is "1," then the access is Read, whereas if the bit is "0," then the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8-bits of data. The receiver provides an ACK pulse for every 8-bits of data received. This handshake mechanism is done as follows: After transmitting 8-bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the 9th clock and releases the SDA line back (to the transmitter). Refer *Figure 3*.

Array Address#1

This is an 8-bit information containing the most significant 8-bits of 16-bit memory array address of a location to be selected within a page block of the device.

Array Address#0

This is an 8-bit information containing the least significant 8-bits of 16-bit memory array address of a location to be selected within a page block of the device.

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP)

If tied to V_{CC}, PROGRAM operations onto the entire memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the entire memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin is tied to V_{SS}.

Device Selection Inputs A2, A1 and A0 (as appropriate)

These inputs collectively serve as “chip select” signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs should be connected to V_{CC} or V_{SS} in a unique manner to allow proper selection of an EEPROM amongst multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3 bit “Device/Page block selection” information (part of slave address) to determine a valid selection. For e.g. if the 3 bit “Device/Page block selection” is 1-0-1, then the EEPROM whose “Device Selection inputs” (A2, A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC} respectively, is selected.

Device Operation

The FM24C128 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the FM24C128 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer *Figure 1*.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The FM24C128 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. Refer *Figure 2*.

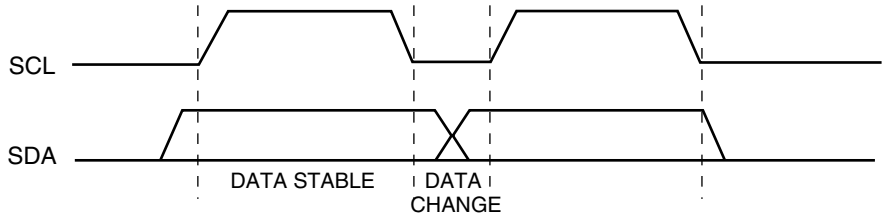
Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the FM24C128 to place the device in the standby power mode. Refer *Figure 2*.

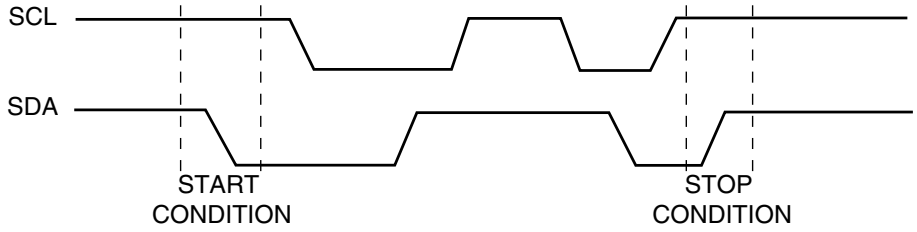
FM24C128 Array Addressing

During Read/Write operations, addressing the EEPROM memory array involves in providing 2 address bytes, “Word Address 1” and “Word Address 0." However on FM24C128 only the 6 least significant bits (LSB) of “Word Address 1” byte are used in decoding the access location. The remaining 2 bits are not used and are recommended to be set to “0." All 8 bits of the “Word Address 0” byte are used in decoding the access location.

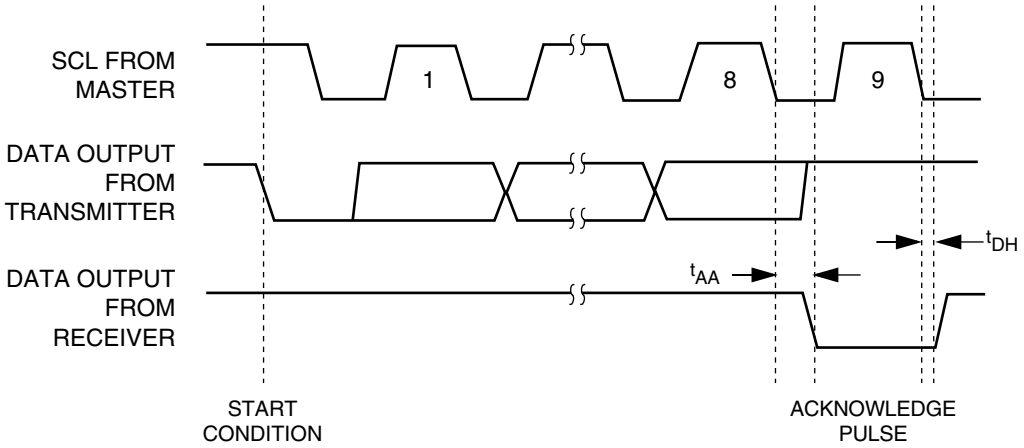
Data Validity (Figure 1)



Start and Stop Definition (Figure 2)



Acknowledge Response from Receiver (Figure 3)



Write Operations

BYTE WRITE

For byte write operation, two bytes of address are required after the slave address. These two bytes select 1 out of the 16,384 locations in the memory. The master provides these two address bytes and for each address byte received, FM24C128 responds with an acknowledge pulse. Master then provides a byte of data to be written into the memory. Upon receipt of this data, FM24C128 responds with an acknowledge pulse. The master then terminates the transfer by generating a stop condition, at which time the FM24C128 begins the internal write cycle to the memory. While the internal write cycle is in progress the FM24C128 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer Figure 4 for the address, acknowledge and data transfer sequence.

PAGE WRITE

To minimize write cycle time, FM24C128 offers Page Write feature, which allows simultaneous programming of up to 64 contiguous bytes. To facilitate this feature, the memory array is organized in terms of "Pages". A Page consists of 64 contiguous byte locations starting at every 64-Byte address boundary (for example, starting at array address 0x0000, 0x0040, 0x0080 etc.). Page Write operation is confined to a single page. In other words a Page Write operation will not cross over to locations on the next page but will "roll over" to the beginning of the same page whenever end of page is reached and additional data bytes are a continued to be provided. A Page Write operation can be initiated to begin at any location within a page (starting address of the Page Write operation need not be the starting address of a Page).

Page Write is initiated in the same manner as the Byte Write operation; but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 63 more bytes. After the receipt of each byte, FM24C128 will respond with an acknowledge pulse, increment the internal address counter to the next address, and is ready to accept the next data. If the master should transmit more than 64 bytes prior to generating the STOP condition, the address counter will "roll over" and previously loaded data will be re-loaded. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. Refer *Figure 5* for the address, acknowledge, and data transfer sequence.

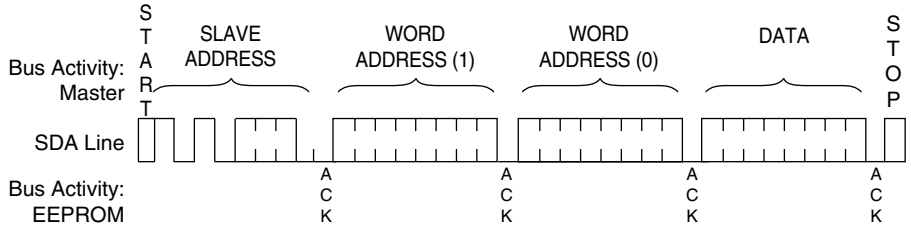
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation, the FM24C128 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the FM24C128 is still busy with the write operation, no ACK will be returned. If the FM24C128 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

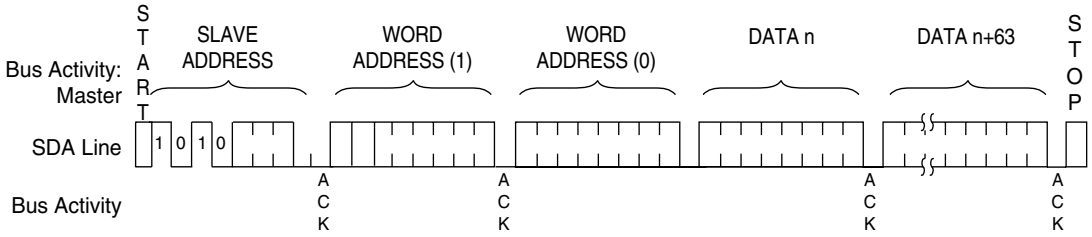
Write Protection

Programming of the entire memory will not take place if the WP pin of the FM24C128 is connected to V_{CC}. The FM24C128 will respond to slave and byte addresses; but if the memory accessed is write protected by the WP pin, the FM24C128 will not generate an acknowledge after the first byte of data has been received. Thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 4)



Page Write (Figure 5)



Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the FM24C128 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to "1," the FM24C128 issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the FM24C128 discontinues transmission. Refer *Figure* 6 for the sequence of address, acknowledge and data transfer.

Random Read

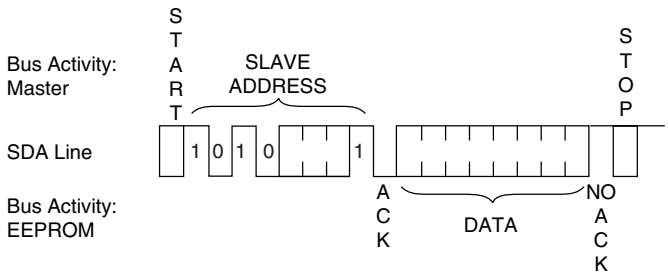
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to "1," the master must first perform a “dummy” write operation. The master issues the start condition, slave address with the R/$\overline{W}$ bit set to "0" and then the byte address. After the byte address acknowledge, the master immediately issues another start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the FM24C128 and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the FM24C128 discontinues transmission. Refer *Figure 7* for the address, acknowledge, and data transfer sequence.

Sequential Read

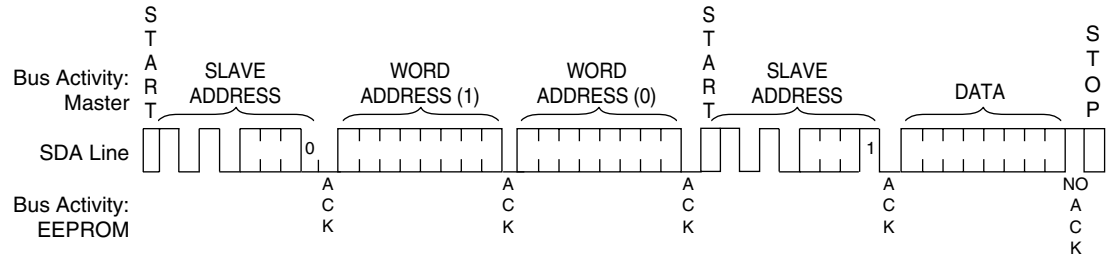
Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The FM24C128 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. FM24C128 continues to output data for each acknowledge received. Refer *Figure 8* for the address, acknowledge, and data transfer sequence.

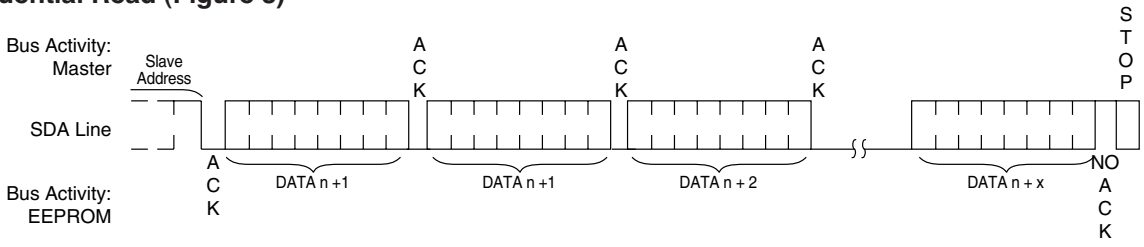
Current Address Read (Figure 6)



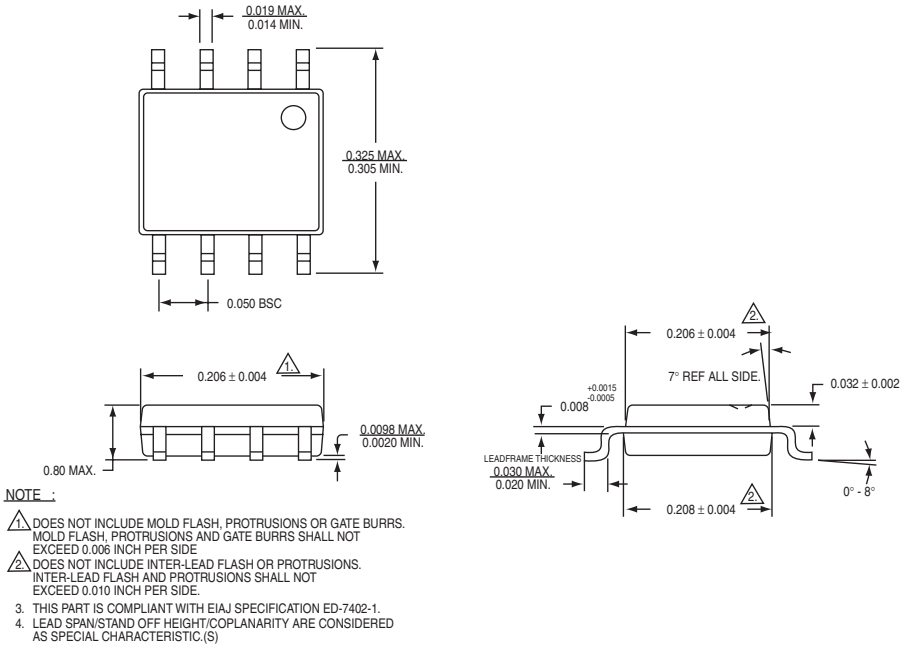
Random Read (Figure 7)



Sequential Read (Figure 8)



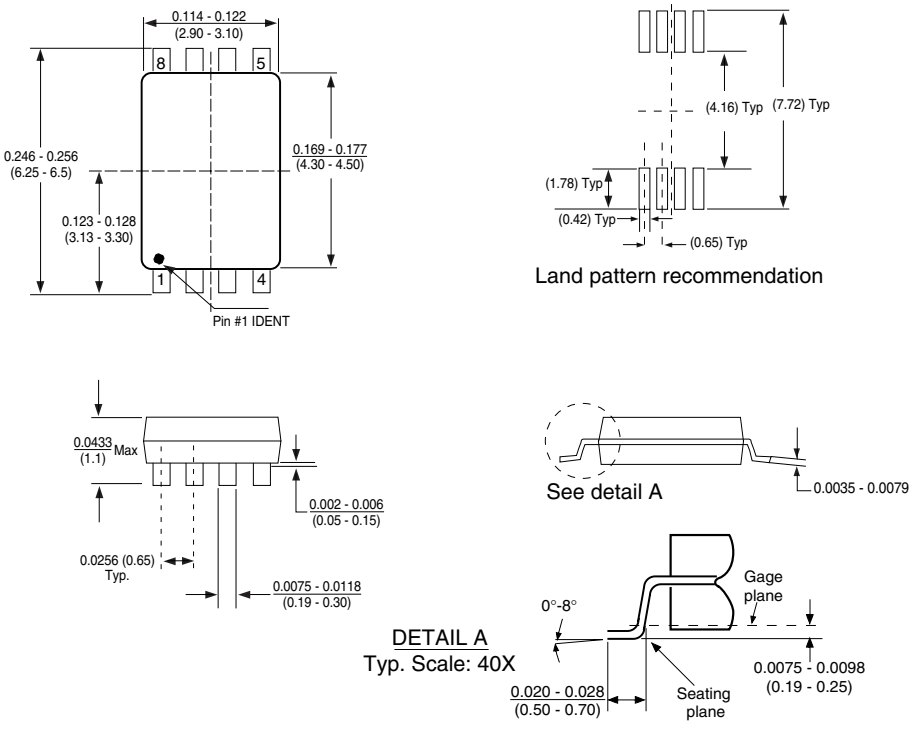
Physical Dimensions inches (millimeters) unless otherwise noted



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION ED-7402-1.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)

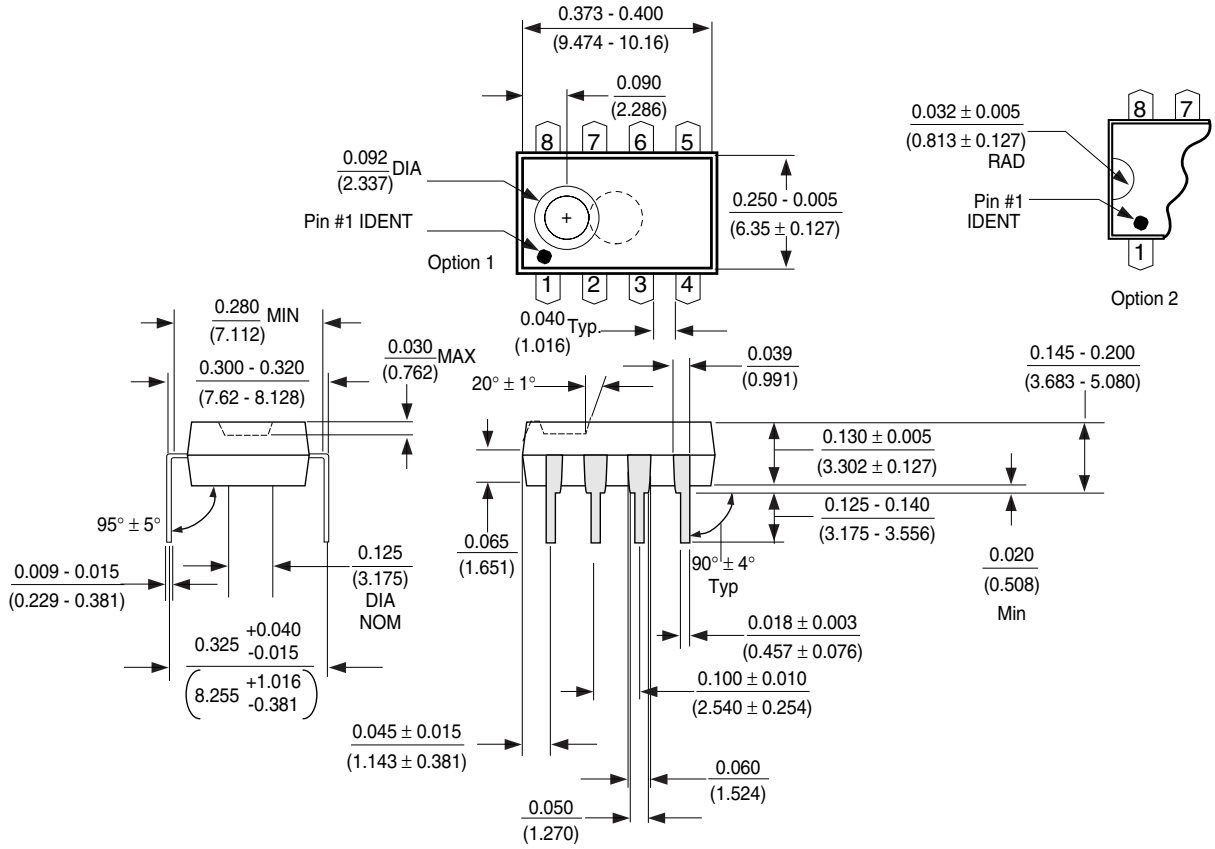
8-Pin Molded Small Outline Package (MW8)
Package Number M08D



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Lead Molded Thin Shrink Small Outline Package (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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