IS25LP256

256MBIT
3V SERIAL FLASH MEMORY WITH 166MHZ MULTI I/O SPI & DTR INTERFACE

ADVANCED DATA SHEET

256MBIT

3V SERIAL FLASH MEMORY WITH 166MHZ MULTI I/O SPI & DTR INTERFACE

ADVANCED INFORMATION

FEATURES

- **Industry Standard Serial Interface**
  - IS25LP256: 256Mbit/32Mbyte
  - 3 or 4 Byte Addressing Mode
  - Supports Standard SPI, Fast, Dual, Dual I/O, Quad, Quad I/O, SPI DTR, Dual I/O DTR, Quad I/O DTR, and QPI
  - Software & Hardware Reset
  - Supports Serial Flash Discoverable Parameters (SFDP)

- **High Performance Serial Flash (SPI)**
  - 80MHz Normal Read
  - Up to166Mhz Fast Read
  - Up to 80MHz DTR (Dual Transfer Rate)
  - Equivalent Throughput of 664 Mb/s
  - Selectable Dummy Cycles
  - Configurable Drive Strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 Erase/Program Cycles
  - More than 20-year Data Retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform: Sector/Block Erase (4/32/64 Kbyte)
  - Program 1 to 256 Byte per Page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous Read 8/16/32/64 Byte Burst
  - Selectable Burst Length
  - QPI for Reduced Instruction Overhead
  - AutoBoot operation

- **Low Power with Wide Temp. Ranges**
  - Single 2.30V to 3.60V Voltage Supply
  - 10 mA Active Read Current
  - 8 µA Standby Current
  - 1 µA Deep Power Down
  - Temp Grades:
    Extended: -40°C to +105°C
    Extended+: -40°C to +125°C
    Auto Grade: up to +125°C

    Note: Extended+ should not be used for Automotive

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Advanced Sector Protection
  - Top/Bottom Block protection and Complement
  - Individual Block/Sector unlock
  - Power Supply Lock Protection
  - 4x256 Byte Dedicated Security Area with User-lockable Bits, (OTP) One Time Programmable Memory
  - 128 bit Unique ID for Each Device (call factory)

- **Industry Standard Pin-out & Packages**
  - M =16-pin SOIC 300mil
  - L = 8-contact WSON 8x6mm
  - G = 24-ball TFBGA 6x8mm (4x6 ball array)
  - KGD (Call Factory)

GENERAL DESCRIPTION

The IS25LP256 Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 166MHz allow for equivalent clock rates of up to 664MHz (166MHz x 4) which equates to over 80Mbytes/data throughput. The IS25xP series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256 bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

GLOSSARY

Standard SPI
In this operation, a 4-wire SPI Interface is utilized, consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. Instructions are sent via the SI pin to encode instructions, addresses, or input data to the device. The SO pin is used to read data or to check the status of the device. This device supports SPI bus operation modes (0,0) and (1,1).

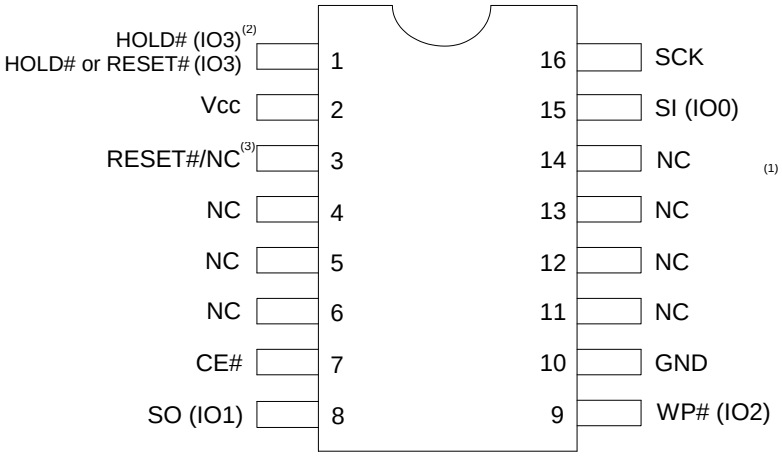
Mutil I/O SPI
Multi-I/O operation utilizes an enhanced SPI protocol to allow the device to function with Dual Output, Dual Input and Output, Quad Output, and Quad Input and Output capability. Executing these instructions through SPI mode will achieve double or quadruple the transfer bandwidth for READ and PROGRAM operations.

Quad I/O QPI
The device enables QPI protocol by issuing an "Enter QPI mode (35h)" command. The QPI mode uses four IO pins for input and output to decrease SPI instruction overhead and increase output bandwidth. SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during QPI mode. Issuing an "Exit QPI (F5h) command will cause the device to exit QPI mode. Power Reset or Hardware/Software Reset can also return the device into the standard SPI mode.

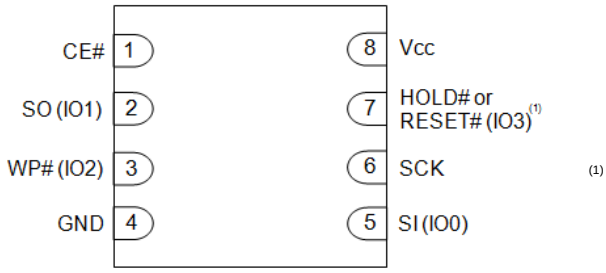
DTR
In addition to SPI and QPI features, the device also supports SPI DTR READ. SPI DTR allows high data throughput while running at lower clock frequencies. SPI DTR READ mode uses both rising and falling edges of the clock to drive output, resulting in reducing the input and output cycles by half.

Programmable drive strength and Selectable burst setting.
The IS25LP256 offers programmable output drive strength and selectable burst (wrap) length features to increase the efficiency and performance of READ operation. The driver strength and burst setting features are controlled by setting the Read Registers. A total of six different drive strengths and four different burst sizes (8/16/32/64 Byte) are available for selection.

PIN CONFIGURATION



16-pin SOIC 300mil

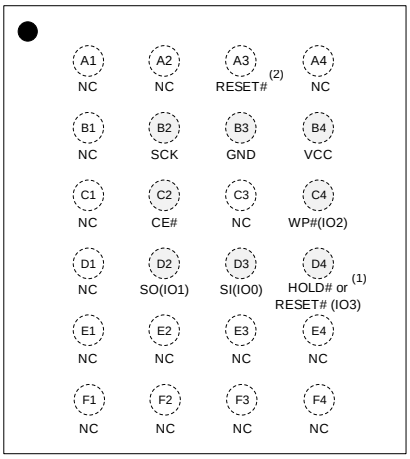


8-contact WSON 8x6mm

Notes:

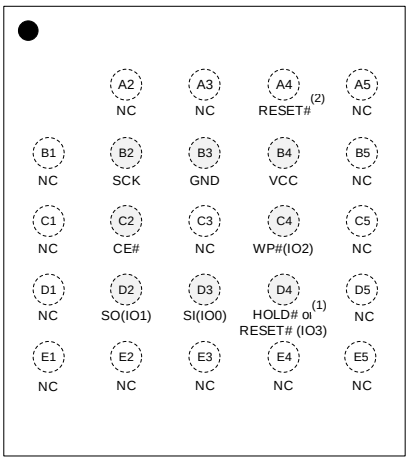
1. **According to the P7 bit setting in Read Register, either HOLD# (P7=0) or RESET# (P7=1) pin can be selected.**
2. **For the dedicated parts that don't have the additional RESET# pin on pin3, either HOLD# or RESET# pin can be selected on pin1 by the P7 bit setting in Read Register when QE=0. For the dedicated parts with additional RESET# pin on pin3, only HOLD# pin is selected for pin1 regardless of the P7 bit of Read Register when QE=0.**
3. **The dedicated parts have additional RESET# pin (pin3) on 16-pin SOIC 300mil package. For the parts, Function Register Bit0 (RESET# Enable/Disable) will be set to "0". The RESET# pin is independent of the P7 bit of Read Register and QE bit of Status Register. The RESET# pin has an internal pull-up resistor and may be left floating if not used. Call Factory for the RESET# pin option.**

Top View, Balls Facing Down



4x6 Ball Array

Top View, Balls Facing Down



5x5 Ball Array

24-ball TFBGA 6x8mm

Notes:

1. **For the dedicated parts that don't have the additional RESET# pin on ball A3, either HOLD# (P7=0) or RESET# (P7=1) pin can be selected on ball D4 by the P7 bit setting in Read Register when QE=0. For the dedicated parts with additional RESET# pin on ball A3, only HOLD# pin is selected for ball D4 regardless of the P7 bit of Read Register when QE=0.**
2. **The dedicated parts have additional RESET# pin (ball A3) on 24-ball TFBGA 6x8mm package. For the parts, Function Register Bit0 (RESET# Enable/Disable) will be set to "0". The RESET# pin is independent of the P7 bit of Read Register and QE bit of Status Register. The RESET# pin has an internal pull-up resistor and may be left floating if not used. Call Factory for the RESET# pin option.**

PIN DESCRIPTIONS

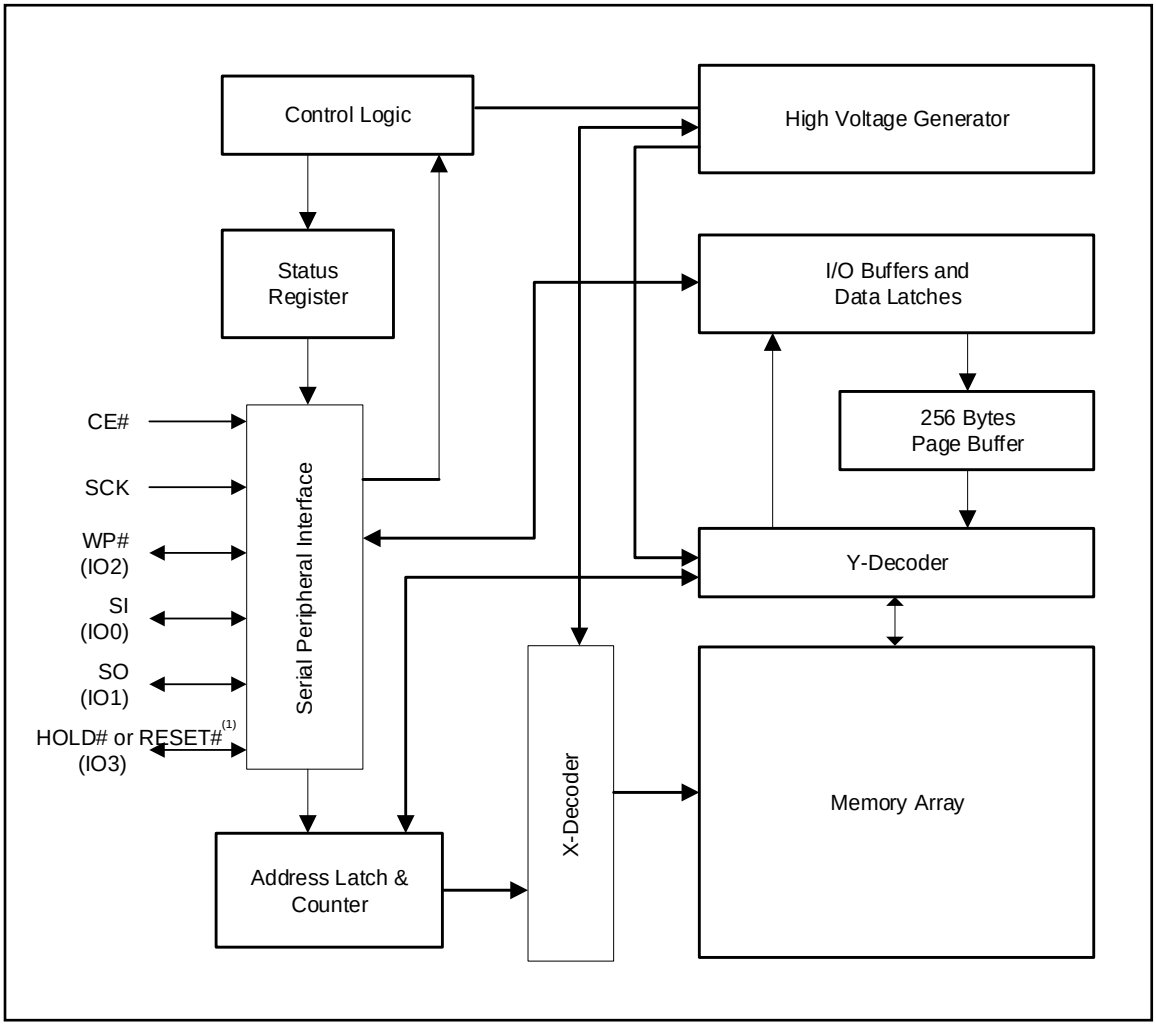
For all other packages except 16-pin SOIC 300mil with additional RESET# pin option

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to "1" and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP# high. When the SRWD is set to "0", the Status Register is not write-protected regardless of WP# state. When the QE bit is set to "1", the WP**#** pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# or RESET# (IO3)	INPUT/OUTPUT	**HOLD# or RESET#/Serial Data IO (IO3):** When the QE bit of Status Register is set to "1", HOLD**#** pin or RESET**#** is not available since it becomes IO3. When QE=0, the pin acts as HOLD# or RESET# and either one can be selected by the P7 bit setting in Read Register. HOLD# will be selected if P7=0 (Default) and RESET# will be selected if P7=1. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled "NC" stand for "No Connect" and should be left unconnected.

For 16-pin SOIC 300mil package with additional RESET# pin option
- RESET# pin will be added to another pin without sharing with HOLD# pin (Call Factory for the parts)

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Same as the description in previous page
SI (IO0), SO (IO1)	INPUT/OUTPUT	Same as the description in previous page
WP# (IO2)	INPUT/OUTPUT	Same as the description in previous page
HOLD# (IO3)	INPUT/OUTPUT	**HOLD#/Serial Data IO (IO3):** When the QE bit of Status Register is set to "1", HOLD# pin is not available since it becomes IO3. When QE=0 the pin acts as HOLD# regardless of the P7 bit of Read Register. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state.
RESET#	INPUT/OUTPUT	**RESET:** This pin is available only for dedicated parts (Call Factory). The RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	Same as the description in previous page
Vcc	POWER	Same as the description in previous page
GND	GROUND	Same as the description in previous page
NC	Unused	Same as the description in previous page

BLOCK DIAGRAM



Note1: In case of 16-pin SOIC package, RESET# pin will be added to another pin without sharing with HOLD# pin for the dedicated parts. Call Factory for the additional RESET# pin option.

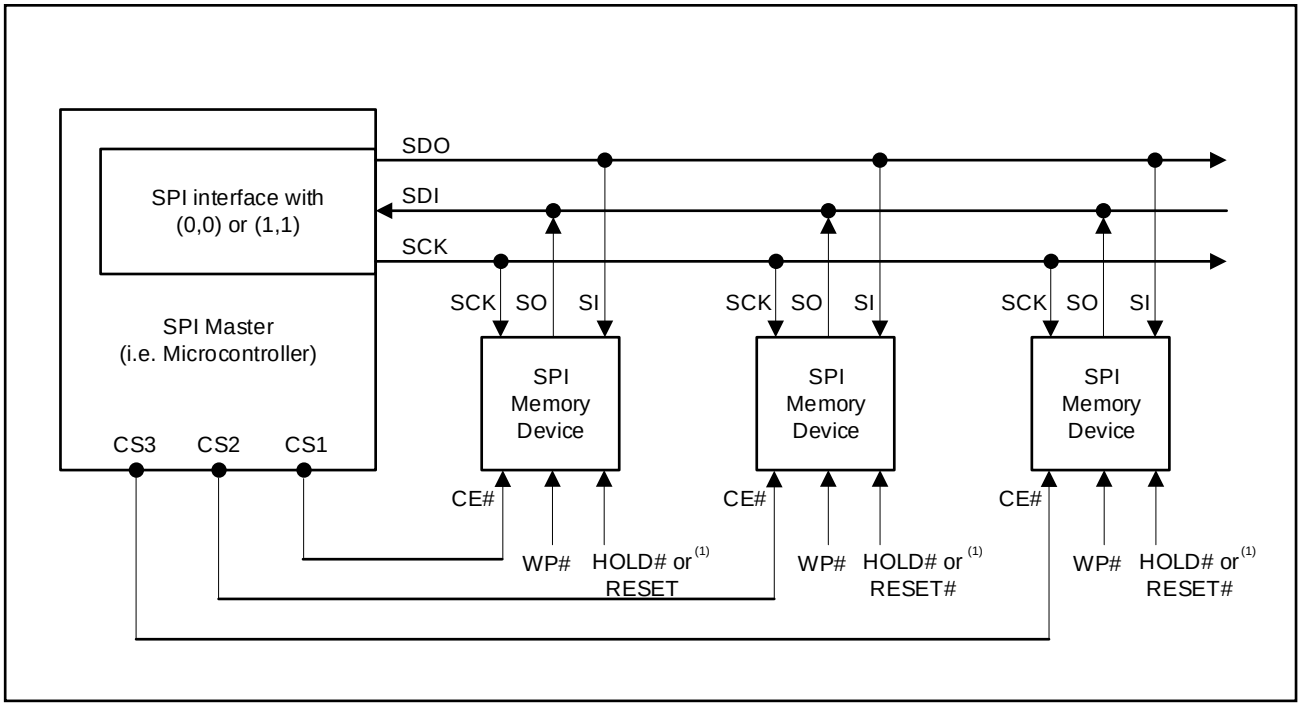
SPI MODES DESCRIPTION

Multiple IS25LP256 devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:

1. **In case of 16-pin SOIC package, RESET# pin will be added to another pin without sharing with HOLD# pin for the dedicated parts. Call Factory for the additional RESET# pin option.**
2. **SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during QPI mode.**

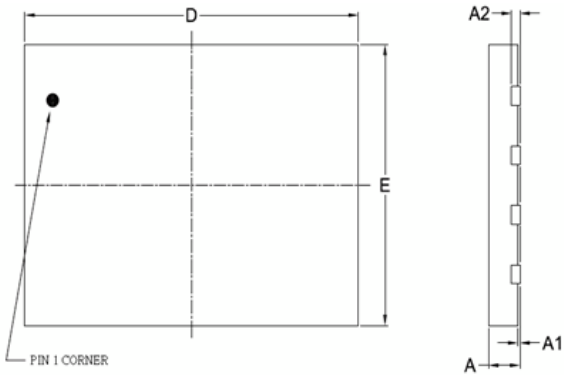
BLOCK/SECTOR ADDRESSES

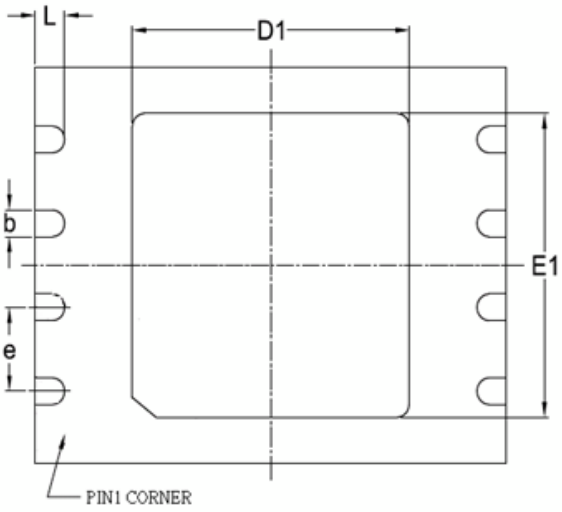
Table Block/Sector Addresses of IS25LP256

Memory Density	Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
256 Mbit	Block 0	Block 0	Sector 0	4	000000h - 000FFFh
			:	:	:
		Block 1	:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	Block 2	Sector 16	4	010000h - 010FFFh
			:	:	:
		Block 3	:	:	:
			Sector 31	4	01F000h - 01FFFFh
	Block 2	Block 4	Sector 32	4	020000h - 020FFFh
			:	:	:
		Block 5	:	:	:
			Sector 47	4	02F000h - 02FFFFh
	:	:	:	:	:
	Block 254	Block 508	Sector 4064	4	FE0000h – FE0FFFh
			:	:	:
		Block 509	:	:	:
			Sector 4079	4	FEF000h – FEFFFFh
	Block 255	Block 510	Sector 4080	4	FF0000h – FF0FFFh
			:	:	:
		Block 511	:	:	:
			Sector 4095	4	FFF000h – FFFFFFh
	:	:	:	:	:
	Block 510	Block 1020	Sector 8160	4	1FE0000h – 1FE0FFFh
			:	:	:
		Block 1021	:	:	:
			Sector 8175	4	1FEF000h – 1FEFFFFh
	Block 511	Block 1022	Sector 8176	4	1FF0000h – 1FF0FFFh
			:	:	:
		Block 1023	:	:	:
			Sector 8191	4	1FFF000h – 1FFFFFFh

PACKAGE TYPE INFORMATION

8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 8X6MM (JL)

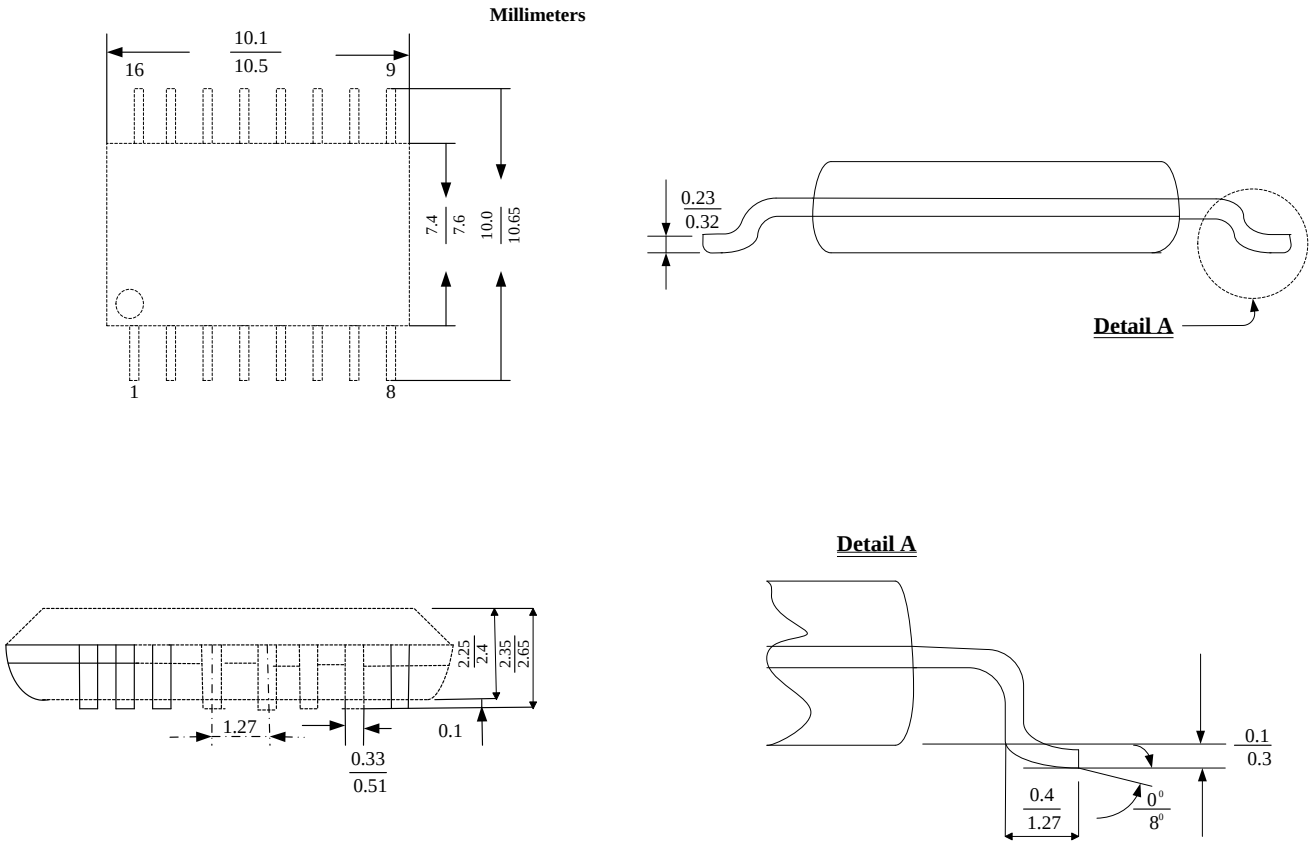




SYMBOL	DIMENSION IN MM		
	MIN.	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	- - -	0.20	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	4.65	4.70	4.75
E1	4.55	4.60	4.65
e	- - -	1.27	- - -
b	0.35	0.40	0.48
L	0.4	0.50	0.60

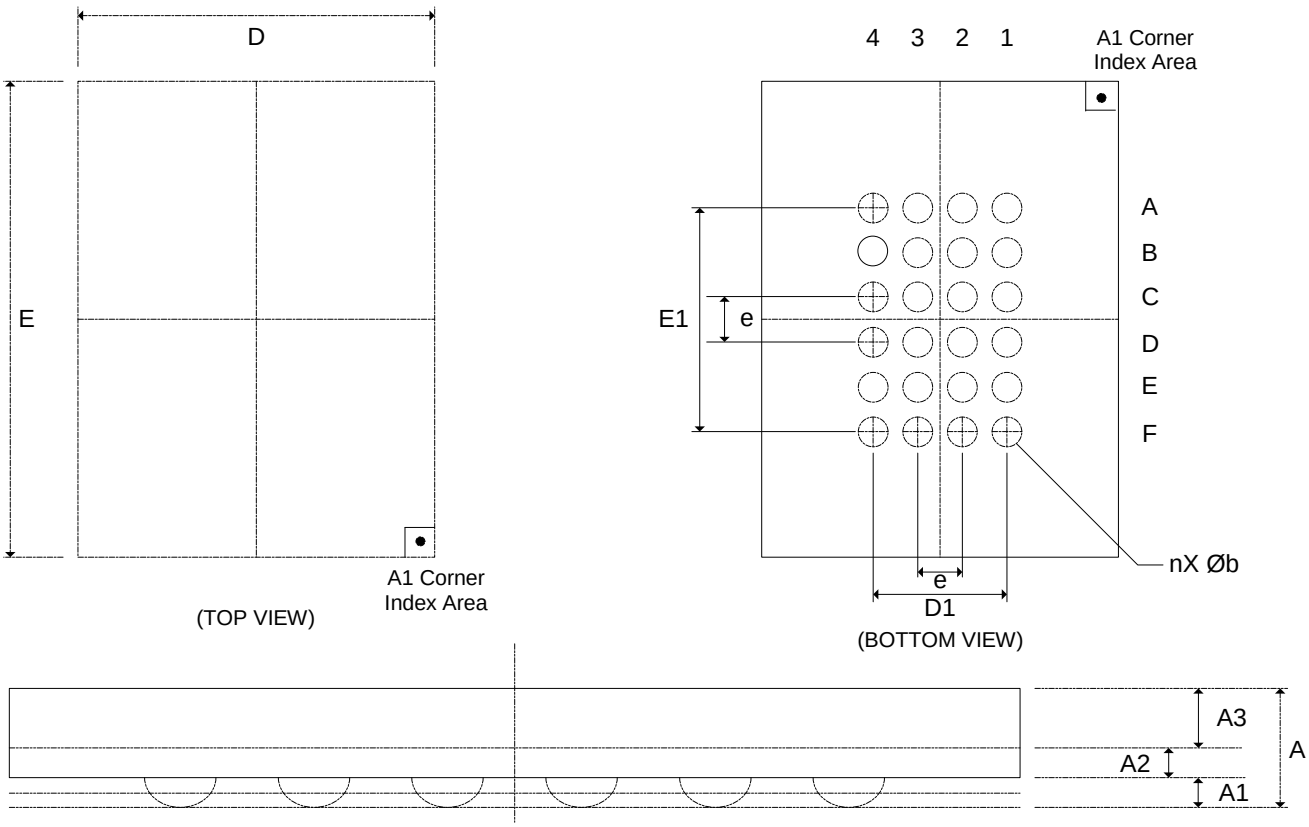
Note: All dimensions are in millimeters.

16-LEAD PLASTIC SMALL OUTLINE PACKAGE (300 MILS BODY WIDTH) (JM)



Note: All dimensions are in millimeters.

24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 4X6 BALL ARRAY (JG)



SYMBOL	DIMENSIONS (MM)		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.27	-	0.37
A2	0.21 REF		
A3	0.54 REF		
D	6 BSC		
E	8 BSC		
D1	-	3.00	-
E1	-	5.00	-
e	-	1.00	-
b	-	0.40	-

Note: All dimensions are in millimeters.

ORDERING INFORMATION- Valid Part Numbers

IS25LP256 - J M L E

TEMPERATURE RANGE
E = Extended (-40°C to +105°C)
E1 = Extended+ (-40°C to +125°C)
A1 = Automotive Grade (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)
A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT
L = **RoHS compliant**

PACKAGE Type[1]
L = 8-contact WSON (8x6mm)
M = 16-pin SOIC 300mil
G = 24-ball TFBGA (6x8mm) 4x6 ball array
W = KGD (Call Factory)

Options
J = Standard
R = additional RESET# pin option for 16-pin SOIC 300mil

Die Revision
Blank = First Revision

Density
256 = 256 Megabit

BASE PART NUMBER
IC = Integrated Silicon Solution Inc.
25LP = FLASH, 2.30V ~ 3.60V, QPI

Note:
1. For the additional RESET# pin option, call Factory

Density	Frequency (MHz)	Order Part Number[1]		Package
256Mb	166	IS25LP256-JLLE	IS25LP256-JLLE1	8-contact WSON (8x6mm)
		IS25LP256-JMLE	IS25LP256-JMLE1	16-pin SOIC 300mil
		IS25LP256-JGLE	IS25LP256-JGLE1	24-ball TFBGA (6x8mm) 4x6 ball array
		IS25LP256-RMLE	IS25LP256-RMLE1	16-pin SOIC 300mil[2]
		IS25LP256-JLLA*		8-contact WSON (8x6mm) (Call Factory)
		IS25LP256-JMLA*		16-pin SOIC 300mil (Call Factory)
		IS25LP256-JGLA*		24-ball TFBGA (6x8mm) 4x6 ball array (Call Factory)
		IS25LP256-RMLA*		16-pin SOIC 300mil[2] (Call Factory)
		IS25LP256-JWLE		KGD (Call Factory)

Notes:
1. A*= A1, A2, A3: Meets AEC-Q100 requirements with PPAP, E1= Extended+ non-Auto qualified
Temp Grades: E= -40 to 105°C, E1= -40 to 125°C, A1= -40 to 85°C, A2= -40 to 105°C, A3= -40 to 125°C
2. The dedicated parts have additional RESET# pin on pin3.