# 10-Bit, 170 MSPS, DAC

# AD9731

## 1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD9731

**2.0 Part Number**. The complete part numbers per Table I of this specification follow:

| Part Number | Description |
|---|---|
| **AD9731-703D** | 10-bit, 170 MSPS, DAC |
| **AD9731-713D** | Radiation tested, 10-bit, 170 MSPS, DAC |
| **AD9731-703F** | 10-bit, 170 MSPS, DAC |
| **AD9731-713F** | Radiation tested, 10-bit, 170 MSPS, DAC |

**2.1 Case Outline**.

| Letter | Descriptive designator [1] | Case Outline (Lead Finish per MIL-PRF-38535) |
|---|---|---|
| D | CDIP2-T28 | 28-Lead Ceramic Side Brazed DIP package |
| F | CDFP3-F28 | 28-Lead Ceramic Bottom Brazed Flatpack |

[1] See MIL-STD-1835

**3.0 Absolute Maximum Ratings**. ($T_A$ = 25°C, unless otherwise noted)

$+V_S$ ..... +6V
$-V_S$ ..... -7V
Analog Output ..... $-V_S$ to $+V_S$
Digital Inputs ..... -0.7V to $+V_S$
Analog Output Current ..... 30 mA
Control Amplifier Input Voltage Range ..... 0V to -4V
Control Amplifier Output Current ..... ±2.5 mA
Reference Input Voltage Range ..... 0V to $-V_S$
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Maximum Junction Temperature ($T_J$) ..... +150°C


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### 3.1 Thermal Characteristics:

Thermal Resistance, SIDEBRAZED (D) Package
Junction-to-Case ($\Theta_{JC}$) = 12 °C/W Max
Junction-to-Ambient ($\Theta_{JA}$) = 40 °C/W Max
Thermal Resistance, BOTTOMBRAZED (F) Package
Junction-to-Case ($\Theta_{JC}$) = 22 °C/W Max
Junction-to-Ambient ($\Theta_{JA}$) = 66 °C/W Max

### 4.0 Electrical Table:

**TABLE I**

| Parameter<br>See notes at end of table | Symbol | Conditions<br>Note 1 | Sub-group | Limit Min | Limit Max | Units |
|---|---|---|---|---|---|---|
| Differential Nonlinearity | DNL | | 1 | | 1 | LSB |
| | | | 2, 3 | | 1.5 | |
| Integral Nonlinearity | INL | | 1 | | 1 | LSB |
| | | | 2, 3 | | 1.5 | |
| Zero Scale Offset Error | IOS | | 1 | | 70 | µA |
| | | | 2, 3 | | 100 | |
| Full Scale Gain Error (Note 2) | Ae | | 1, 2, 3 | | ±5 | % FS |
| Internal Reference Voltage | $V_{REF}$ | $I_{REF}$ = -50 µA to 500 µA | 1 | -1.35 | -1.15 | V |
| | | | 2, 3 | -1.37 | -1.13 | |
| Input Logic "1" Voltage | $V_{IH}$ | | 1, 2, 3 | 2 | | V |
| Input Logic "0" Voltage | $V_{IL}$ | | 1, 2, 3 | | 0.8 | |
| Input Logic "1" Current | $I_{IH}$ | | 1, 2, 3 | | 50 | µA |
| Input Logic "0" Current | $I_{IL}$ | | 1, 2, 3 | | 100 | |
| Positive Digital Supply Current | $+I_{DIG}$ | | 1 | | 20 | mA |
| | | | 2, 3 | | 22 | |
| Negative Digital Supply Current | $-I_{DIG}$ | | 1 | | 42 | mA |
| | | | 2, 3 | | 47 | |
| Negative Analog Supply Current | $-I_{ANA}$ | | 1 | | 53 | mA |
| | | | 2, 3 | | 66 | |

NOTES:

1 $+V_S$ = +5V, $-V_S$ = -5.2V, Clock = 125 MHz, $R_{SET}$ = 1.96 KΩ for 20.4 mA $I_{OUT}$, $V_{REF}$ = -1.25V, unless otherwise specified.

2 Measured as an error in ratio of full-scale current to current through RSET (640 µA nominal); ratio is nominally 32. DAC load is virtual ground.

**4.1 Electrical Test Requirements**:

**Table II**

| Test Requirements | Subgroups (in accordance with MIL-PRF-38535, Table III) |
|---|---|
| Interim Electrical Parameters | 1 |
| Final Electrical Parameters | 1, 2, 3 1/ 2/ |
| Group A Test Requirements | 1, 2, 3 |
| Group C end-point electrical parameters | 1 2/ |
| Group D end-point electrical parameters | 1 |
| Group E end-point electrical parameters | 1 |

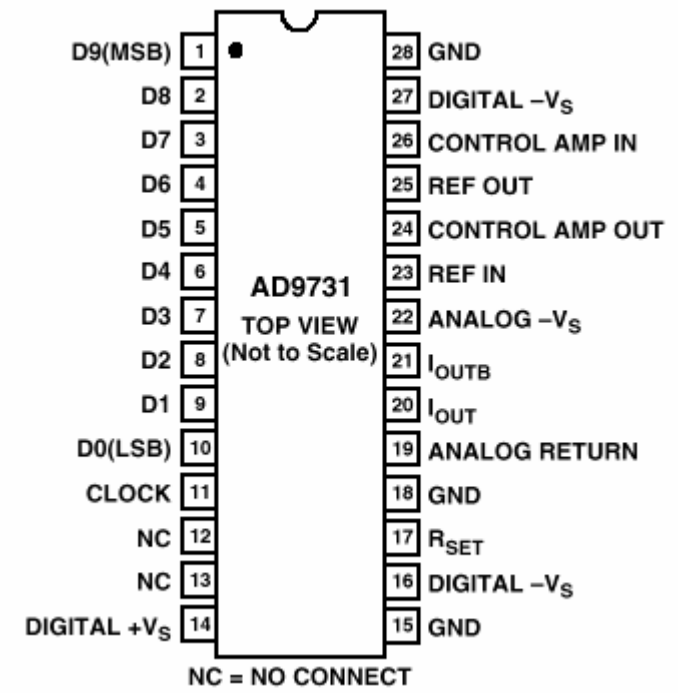
1/ PDA applies to Subgroup 1. Deltas excluded from PDA
2/ See table III for delta parameters and limits.

**4.2 Table III. Burn-in test delta limits**.

**Table III**

| TEST TITLE | ENDPOINT LIMIT | DELTA LIMIT | UNITS |
|---|---|---|---|
| $-I_{DIG}$ | 42 | ±4.2 | mA |
| $I_{ANA}$ | 53 | ±5.3 | mA |
| $+I_{DIG}$ | 20 | ±2.0 | mA |
| IOS | ±70 | ±35 | µA |
| Ae | ±5.0 | ±2.0 | %FS |

**5.0 Package Pin-out**:




**6.0 Microcircuit Technology Group:** The microcircuit is covered by technology group 80.

**7.0 Life Test/Burn-In Circuit:** Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition B.

**8.0 MIL-STD-38535 QMLV exceptions:**

**8.1** Full WLA per MIL-STD-883 TM 5007 is not available for this product fabricated in a QMLQ wafer process facility. SEM Inspection only is available per MIL-STD-883, TM2018.

| Rev | Description of Change | Date |
|---|---|---|
| A | Initiate | June 30, 2000 |
| B | Delete output compliance from Table I - guaranteed by design | Nov. 28, 2000 |
| C | Update paragraph 1.0, added web address | Feb. 7, 2002 |
| D | Update web address. | Mar. 18, 2003 |
| E | Delete Burn-In circuit. | Aug. 5, 2003 |
| F | Add AD9731-703F & AD9731-713F (flatpack version) | Oct. 27, 2003 |
| G | Clarify SEM vs. WLA availability for QMLQ fab process | Sep. 21, 2007 |
| H | Update header/footer & add to 1.0 Scope description | Feb. 22,2008 |
| I | Add descriptive designator to 2.1- Case Outline | Aug. 18, 2009 |
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