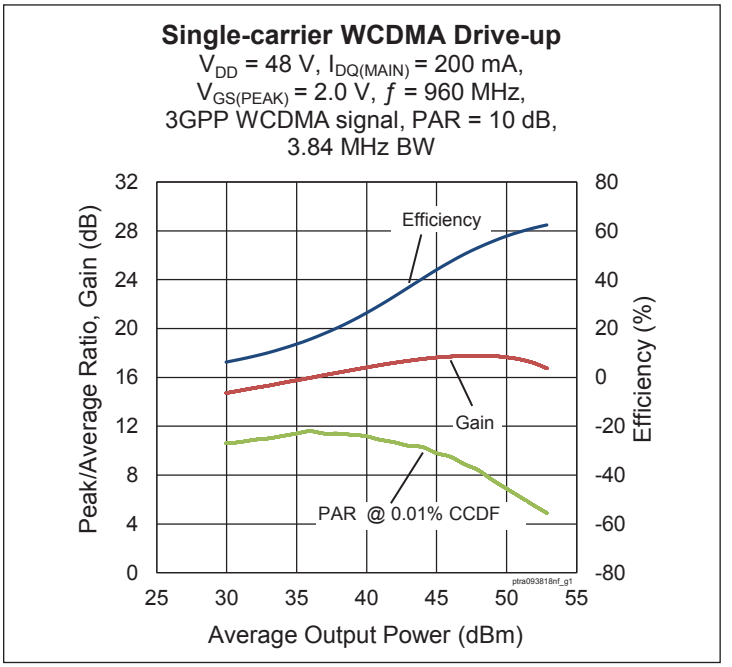
Thermally-Enhanced High Power RF LDMOS FET
415 W, 48 V, 925 – 960 MHz

Description

The PTRA093818NF is a 415-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 925 to 960 MHz frequency band. Features include input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTRA093818NF
Package PG-HBSOF-6-2



Features

- Broadband internal input matching
- Asymmetrical design
  - Main : P_{1dB} = 165 W Typ
  - Peak : P_{1dB} = 250 W Typ
- Typical Pulsed CW performance, 960 MHz, 48 V, Doherty configuration
  - Output power at P_{3dB} = 375 W
  - Efficiency = 55%
  - Gain = 18 dB
- Capable of handling 10:1 VSWR @ 48 V, 81.4 W CW output power
- Integrated ESD protection
- Human Body Model class 1C (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Infineon Doherty production test fixture)
V_{DD} = 48 V, I_{DQ} = 200 mA, $V_{GS(PEAK)}$ = 2.0 V, P_{OUT} = 81.3 W avg, f = 960 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	16.5	17	—	dB
Drain Efficiency	η_D	49	52	—	%
Adjacent Channel Power Ratio	ACPR	—	–30	–28.5	dBc
Output PAR@0.01% CCDF	OPAR	7	7.7	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
	V_{DS} = 105 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA
On-State Resistance (Main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.12	—	Ω
(Peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.08	—	Ω
Operating Gate Voltage (Main)	V_{DS} = 48 V, I_{DQ} = 0.9 A	V_{GS}	3	3.5	4	V
(Peak)	V_{DS} = 48 V, I_{DQ} = 0 A	V_{GS}	—	2	—	V

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	105	V
Gate-Source Voltage	V_{GS}	–6 to +12	V
Operating Voltage	V_{DD}	0 to +55	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance (Main, T_{CASE} = 70°C, 81.3 W CW)	$R_{\theta JC}$	0.57	°C/W

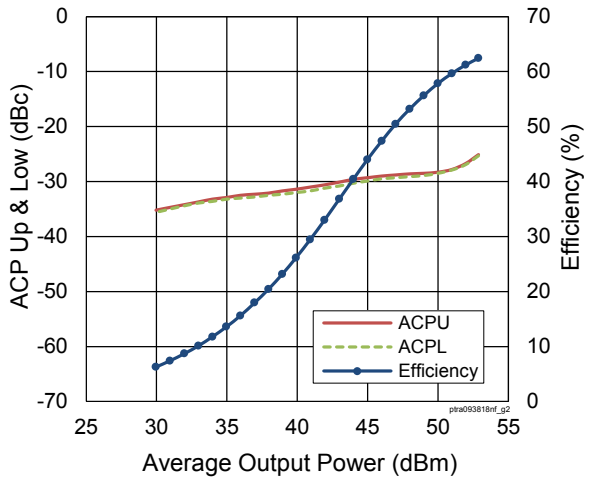
Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTRA093818NF V1 R5	PTRA093818NFV1R5XUMA1	PG-HBSOF-6-2	Tape & Reel, 500 pcs

Typical RF Performance (data taken in production test fixture)

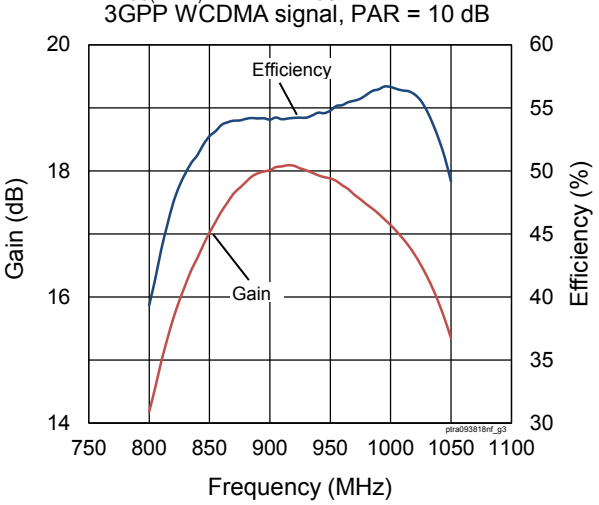
Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V, f = 960 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz



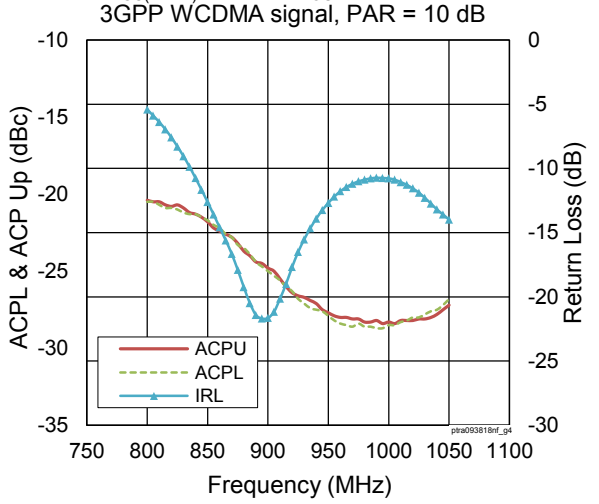
Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V, P_{OUT} = 49.1 dBm,
3GPP WCDMA signal, PAR = 10 dB



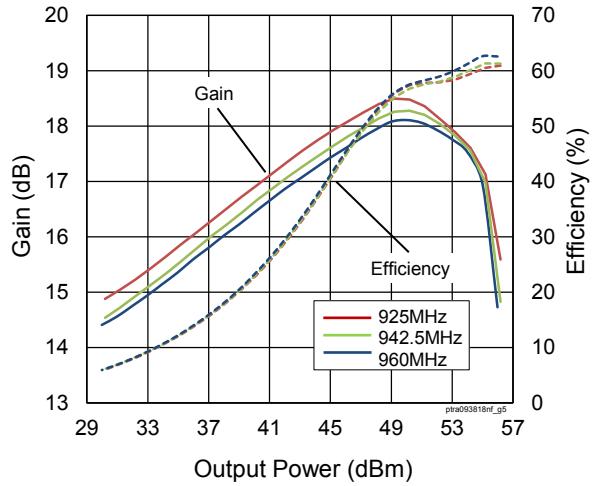
Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V, P_{OUT} = 49.1 dBm,
3GPP WCDMA signal, PAR = 10 dB



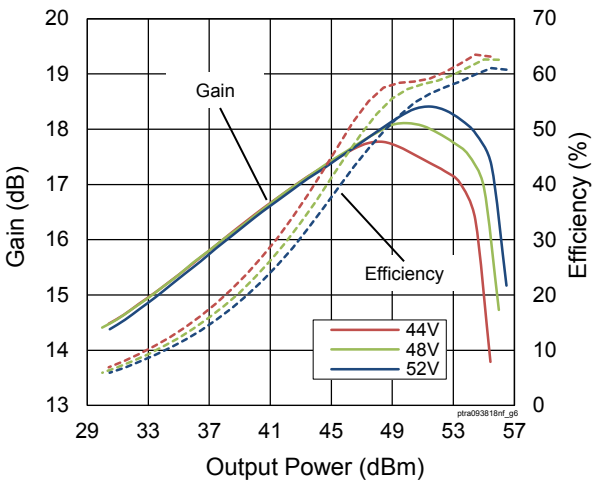
CW Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V

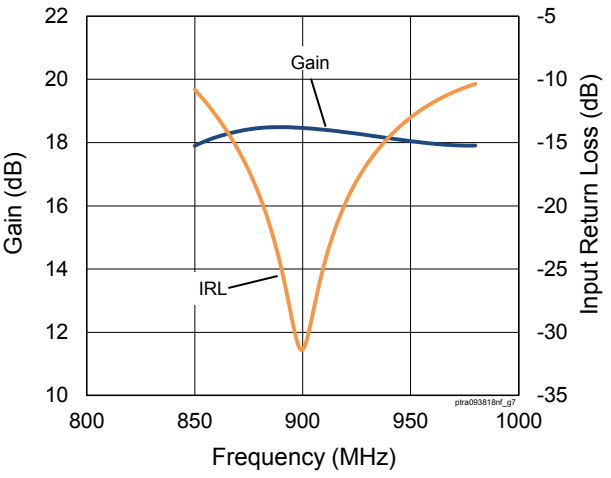


Typical RF Performance (cont.)

CW Performance at various V_{DD}
$I_{DQ(MAIN)}$ = 200 mA, $V_{GS(PEAK)}$ = 2.0 V,
f = 960 MHz



CW Performance Small Signal Gain & Input Return Loss
V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 2.0 V



Load Pull Performance

Main Side Load Pull Performance – Pulsed CW signal: 10 µsec, 10% duty cycle, V_{DD} = 48 V, I_{DQ} = 350 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
925	2.34-j5.57	2.03-j1.79	19.7	53.30	216	60.0	3.40-j0.14	21.4	52.00	159	70.6
940	2.38-j5.42	2.09-j1.85	19.8	53.10	206	59.0	3.44-j0.44	21.5	51.70	147	69.3
960	3.96-j5.20	2.07-j1.66	20	53.10	205	61.0	3.33-j0.07	21.5	51.60	144	69.2

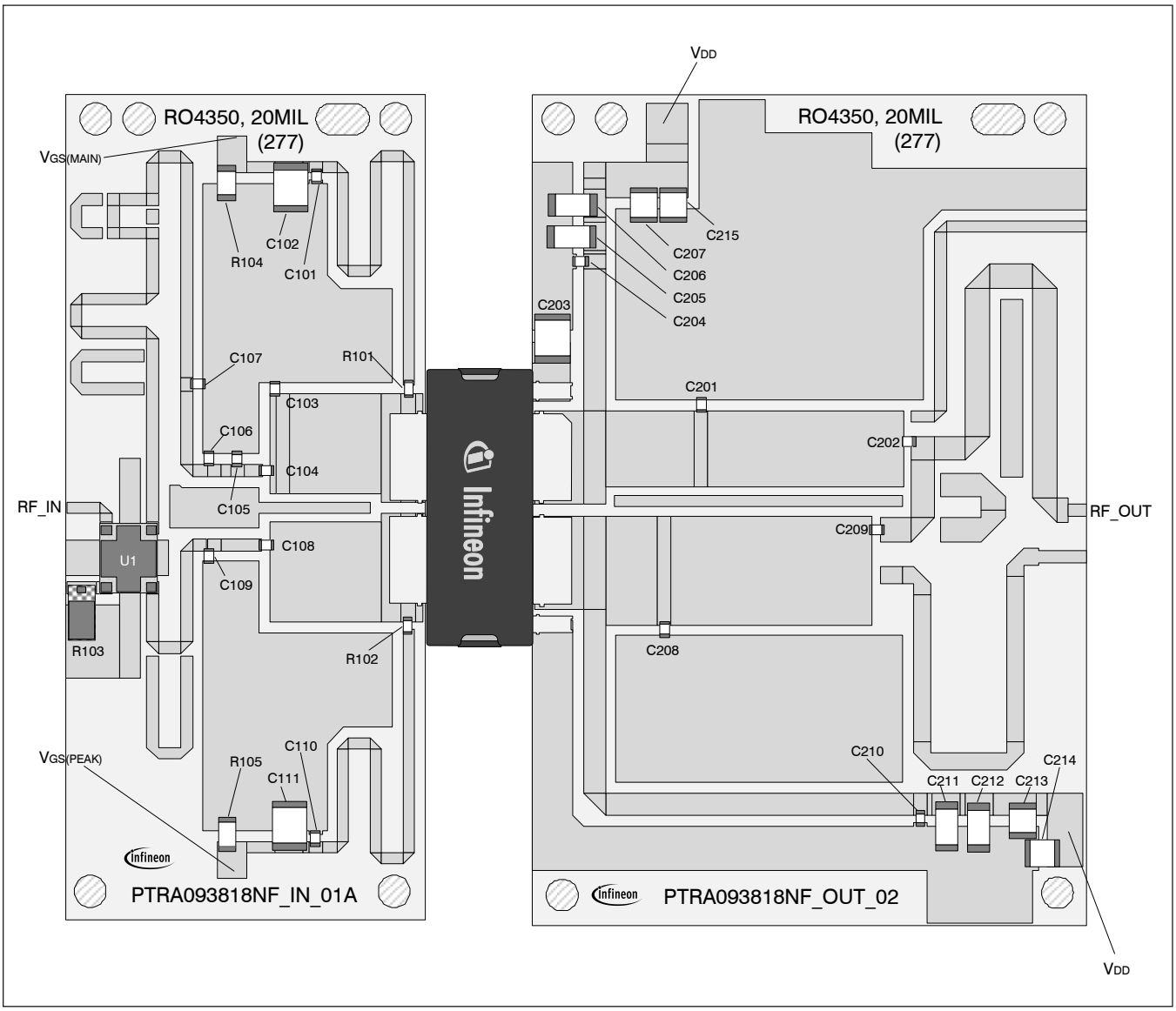
		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
925	2.34-j5.57	2.13-j2.00	17.8	54.13	259	62.6	3.49-j0.40	19.4	52.76	189	72.1
940	2.38-j5.42	2.14-j2.24	17.8	53.91	246	60.0	4.01-j0.08	19.8	52.04	160	70.6
960	3.96-j5.20	2.19-j2.31	17.9	53.87	244	60.6	3.44-j0.18	19.5	52.28	169	70.7

Peak Side Load Pull Performance – Pulsed CW signal: 10 µsec, 10% duty cycle, V_{DD} = 48 V, $V_{GS(PEAK)}$ = 2 V, class C

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
925	1.92-j4.34	1.06-j2.15	15.3	55.05	320	59.7	1.0-j0.86	16.4	52.56	180	72.8
940	2.49-j4.58	1-j2.17	15.48	55.05	320	59.4	1-j0.84	16.4	52.20	166	71.9
960	3.20-j5.21	1.12-j2.37	15.54	55.00	316	59.0	1.06-j1.12	16.5	52.67	185	70.4

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P3dB [W]	ηD [%]
925	1.92-j4.34	1.33-j2.18	13.5	55.74	375	63.5	1.09-j0.98	14.4	53.57	228	72.7
940	2.49-j4.58	1.38-j2.45	13.3	55.70	372	59.4	1.04-j0.95	14.47	53.20	209	71.5
960	3.20-j5.21	1.04-j2.47	13.4	55.67	369	59.1	1.1-j1.26	14.57	53.50	224	70.0

Reference Circuit, 925 – 960 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

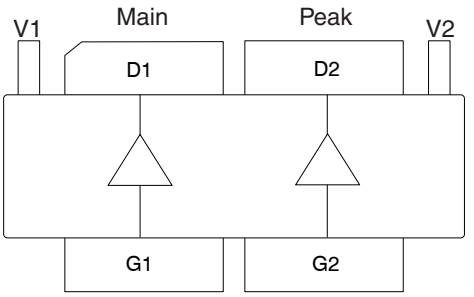
Reference Circuit Assembly

DUT	PTRA093818NF V1
Test Fixture Part No.	LTA/PTRA093818NF V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 925 – 960 MHz
Find Gerber files for this test fixture on the Infineon Web site at http://www.infineon.com/rfpower	

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C104, C108, C110	Capacitor, 43 pF	ATC	ATC600F430JW250T
C102, C111	Capacitor, 4.7 µF	TDK Corporation	C4532X7S2A475M230KB
C103	Capacitor, 3.3 pF	ATC	ATC600F3R3CW250T
C105	Capacitor, 2.2 pF	ATC	ATC600F2R2CW250T
C106, C109	Capacitor, 6.2 pF	ATC	ATC600F6R2CW250T
C107	Capacitor, 1.8 pF	ATC	ATC600F1R8CW250T
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-3GEYJ100V
R103	Resistor, 50 ohms	ANAREN	C16A50Z4
R104, R105	Resistor, 1K ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
U1	Hybrid Coupler	ANAREN	X3C09P1-04S
Output			
C201, C208	Capacitor, 6.2 pF	ATC	ATC600F6R2CW250T
C202	Capacitor, 10 pF	ATC	ATC600F100JW250T
C203, C205, C206, C211, C212	Capacitor, 4.7 µF	TDK Corporation	C4532X7S2A475M230KB
C204, C209, C210	Capacitor, 43 pF	ATC	ATC600F430JW250T
C207, C213, C214, C215	Capacitor, 10 µF	MURATA	GRM32EC72A106KE05

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1	Drain video decoupling, no DC bias
V2	NC or connected to GRD

Package Outline Specifications

Package PG-HBSOF-6-2 (top view)

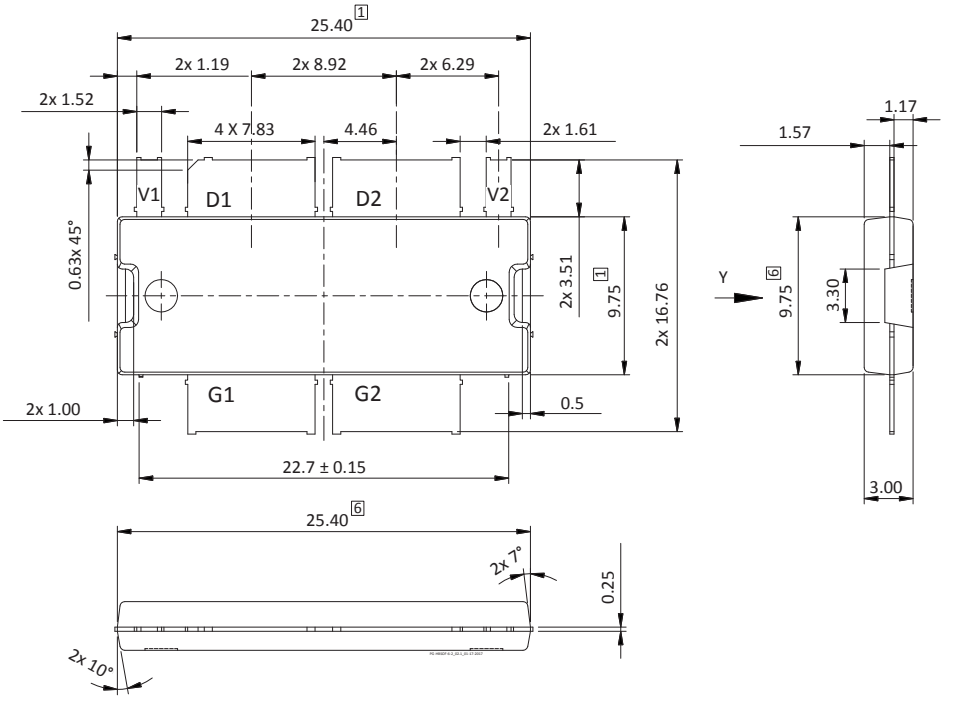


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Does not include mold/dam bar and metal protrusion.
7. Exposed metal surface is tin-plated, may not be covered by mold compound.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces are tin-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D1, D2 = drain; G1, G2 = gate; S = source; V1 = drain video decoupling, no DC Bias, V2 = NC or connected to GRD

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Package Outline Specifications (cont.)

Package PG-HBSOF-6-2 (bottom view)

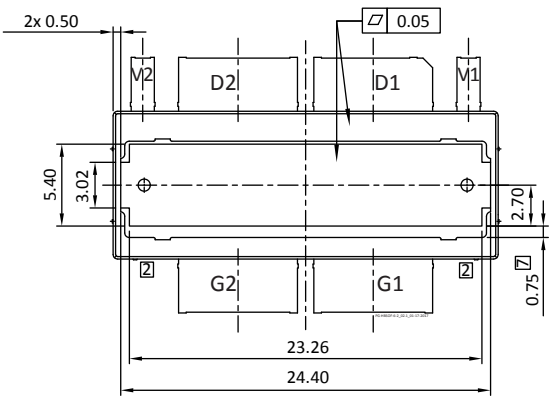


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Revision History

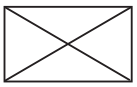
Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2016-05-04	Advance	All	Data Sheet reflects advance specification for product development
02	2016-08-22	Advance	All	Revised package (3D rendering, package number and package outline)
03	2016-10-21	Production	All	Data Sheet reflects released product specification
03.1	2016-12-07	Production	All	Revised Maximum Ratings table
03.2	2016-01-12	Production	8, 9	Revised typo in package outline
03.3	2016-01-24	Production	7, 8, 9	Updated pinout diagram and package outline
04	2017-02-01	Production	2 8, 9	Updated Thermal Characteristics Updated Package Outline
04.1	2017-03-30	Production	3, 4	Fixed missing labels on CW performance graphs
05	2017-08-10	Production	6, 7	Updated circuit drawing and components information
05.1	2017-08-16	Production	6	Revised PCB layout

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