9-Bit address/data Futurebus transceiver, ADT 74F8965/74F8966

FEATURES

- 9–bit transceiver (both directions)
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1V to 2V) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 futurebus standards and IEEE 1194 BTL standard
- Built–in precision band–gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch–free power up/power down operation
- Guaranteed skew of less than 2ns

DESCRIPTION

The 74F8965 and 74F8966 are 9–bit bidirectional latchable transceivers and are intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a precision band gap references for improved noise margins.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F8965 and 74F8966 A ports have TTL 3–state drivers and TTL receivers.
The B ports have standard BTL I/O with 100mA current sink capability. The B–to–A path is a simple inverted buffered path. When going from A–to–B the user may choose between a buffered path or a latching function.

The 74F8966 also has an idle arbitrator/multiple competitors output. The $\overline{IAMC}$ output compares, using a wired–OR configuration, the data on the bus to the latched data presented to the bus. If the bus data matches the data presented by the 74F8966 then $\overline{IAMC}$ is high. If the data doesn't match then $\overline{IAMC}$ goes low.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8965	3.5ns	80mA
74F8966	3.5ns	80mA

ORDERING INFORMATION

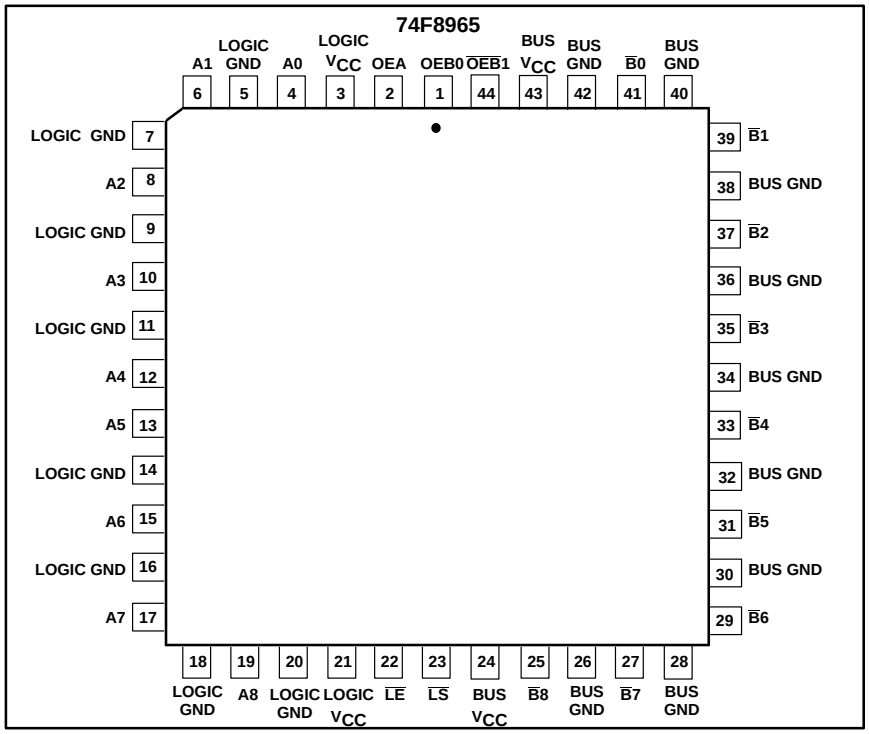
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
44–pin PLCC	N74F8965A, N74F8966A

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

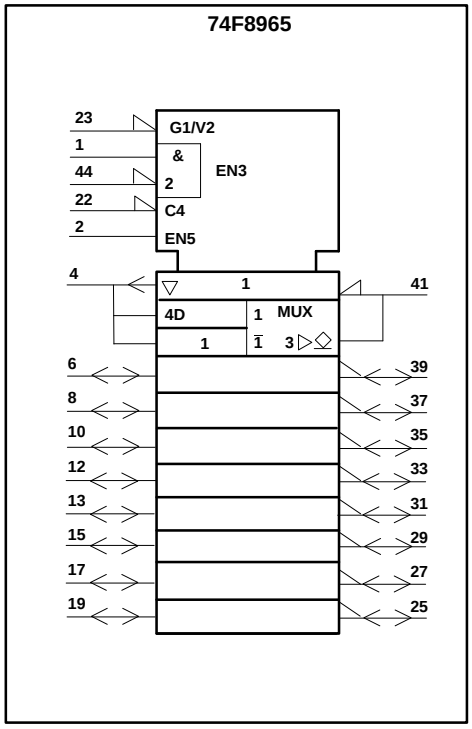
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A8	TTL data inputs	1.0/0.033	20µA/20µA
$\overline{B0}$ – $\overline{B8}$	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA, OEB0, $\overline{OEB1}$	Output enable inputs	1.0/0.167	20µA/100µA
$\overline{LS}$	Latch select (active low) ('F8965)	1.0/0.167	20µA/100µA
$\overline{IAREQ}$	Idle arbitration request (active low) ('F8965)	1.0/0.167	20µA/100µA
$\overline{LE}$	Latch enable input (active low)	1.0/0.167	20µA/100µA
A0 – A8	3–state TTL outputs	150/40	3mA/24mA
$\overline{B0}$ – $\overline{B8}$	Open collector BTL outputs	OC/166.7	OC/100mA
$\overline{IAMC}$	Idle arbitration/multiple competitors output ('F8966)	OC/80	OC/48mA

Notes to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC = Open collector.

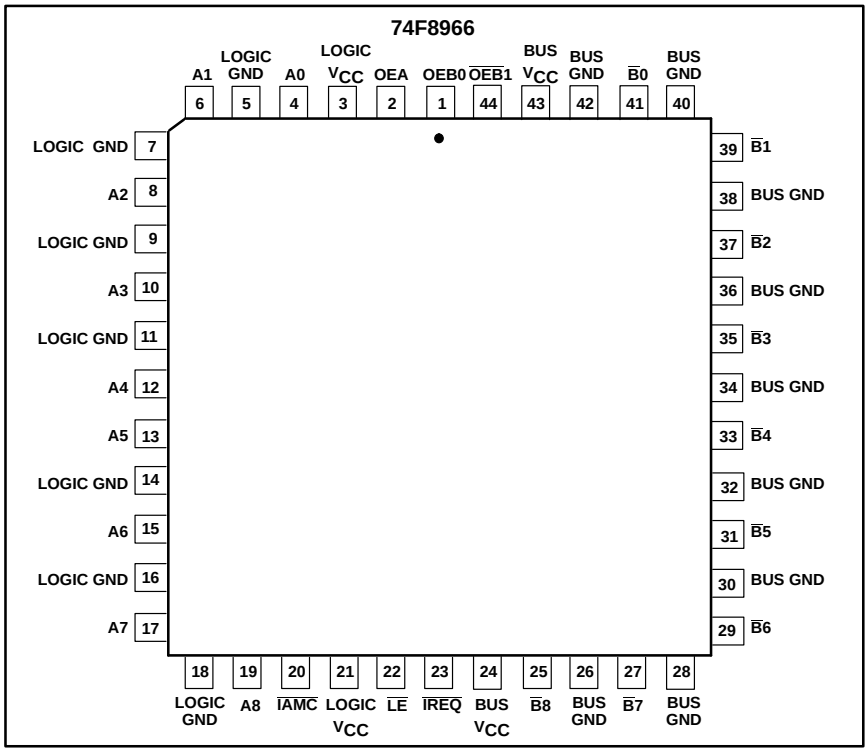
PIN CONFIGURATION PLCC



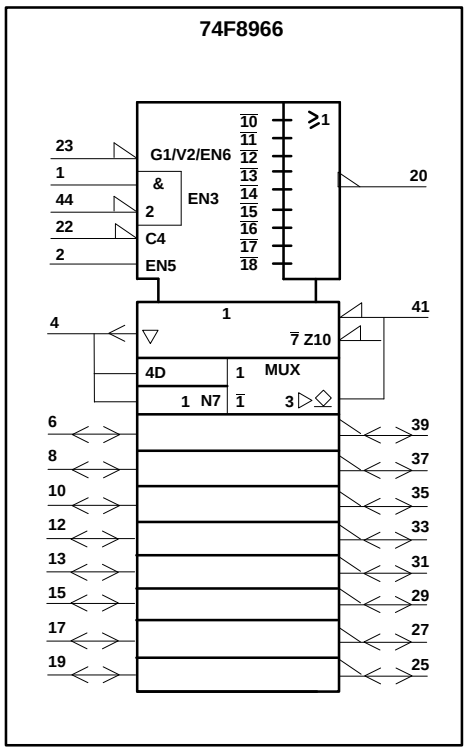
IEC/IEEE SYMBOL



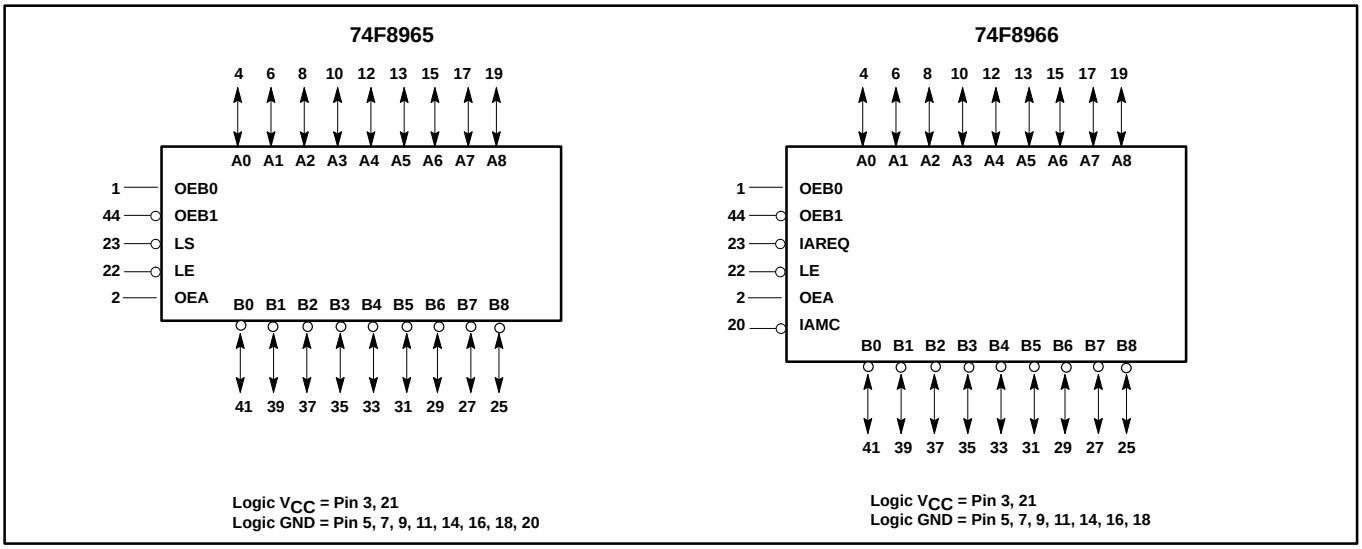
PIN CONFIGURATION PLCC



IEC/IEEE SYMBOL



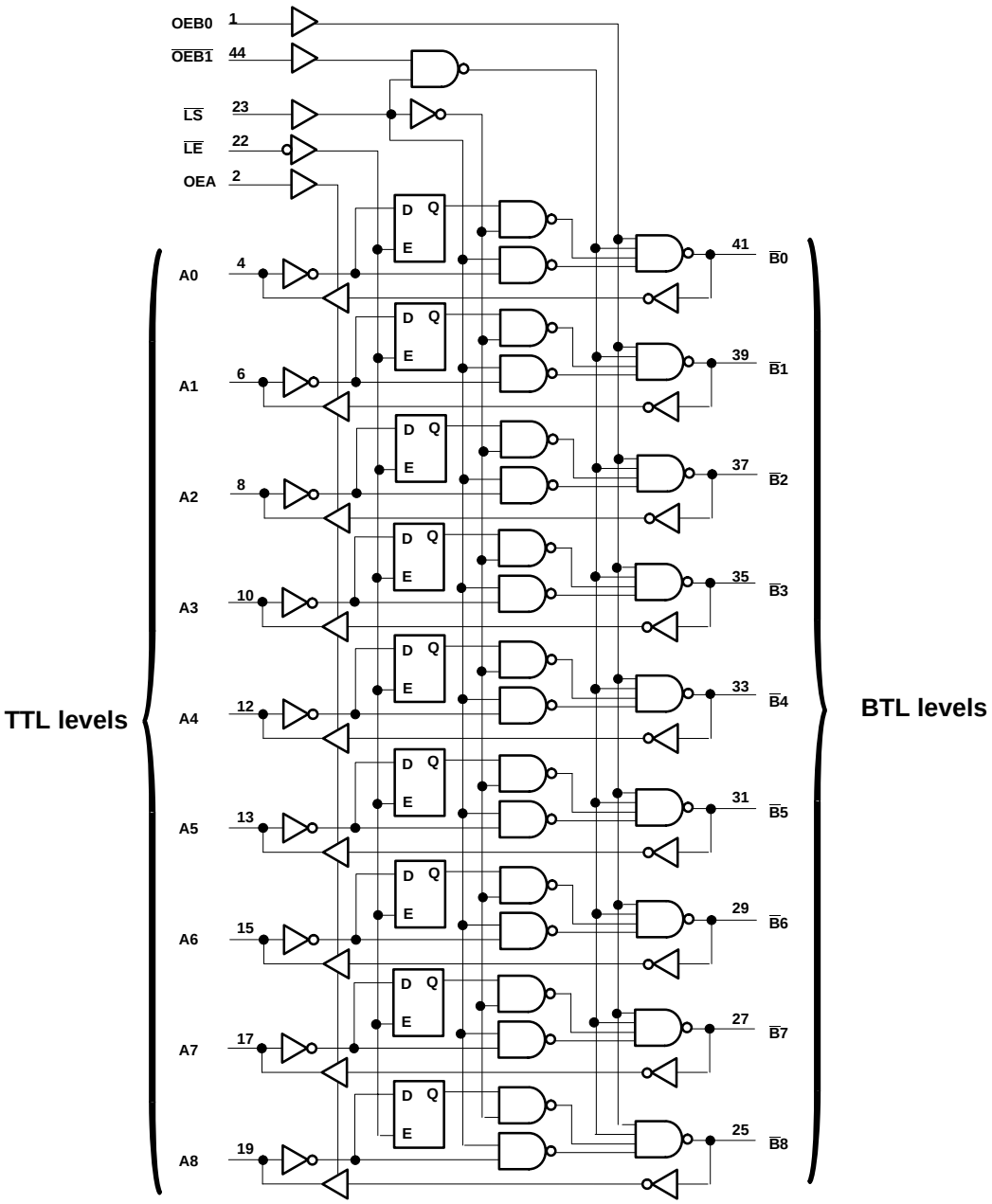
LOGIC SYMBOL



PIN DESCRIPTION

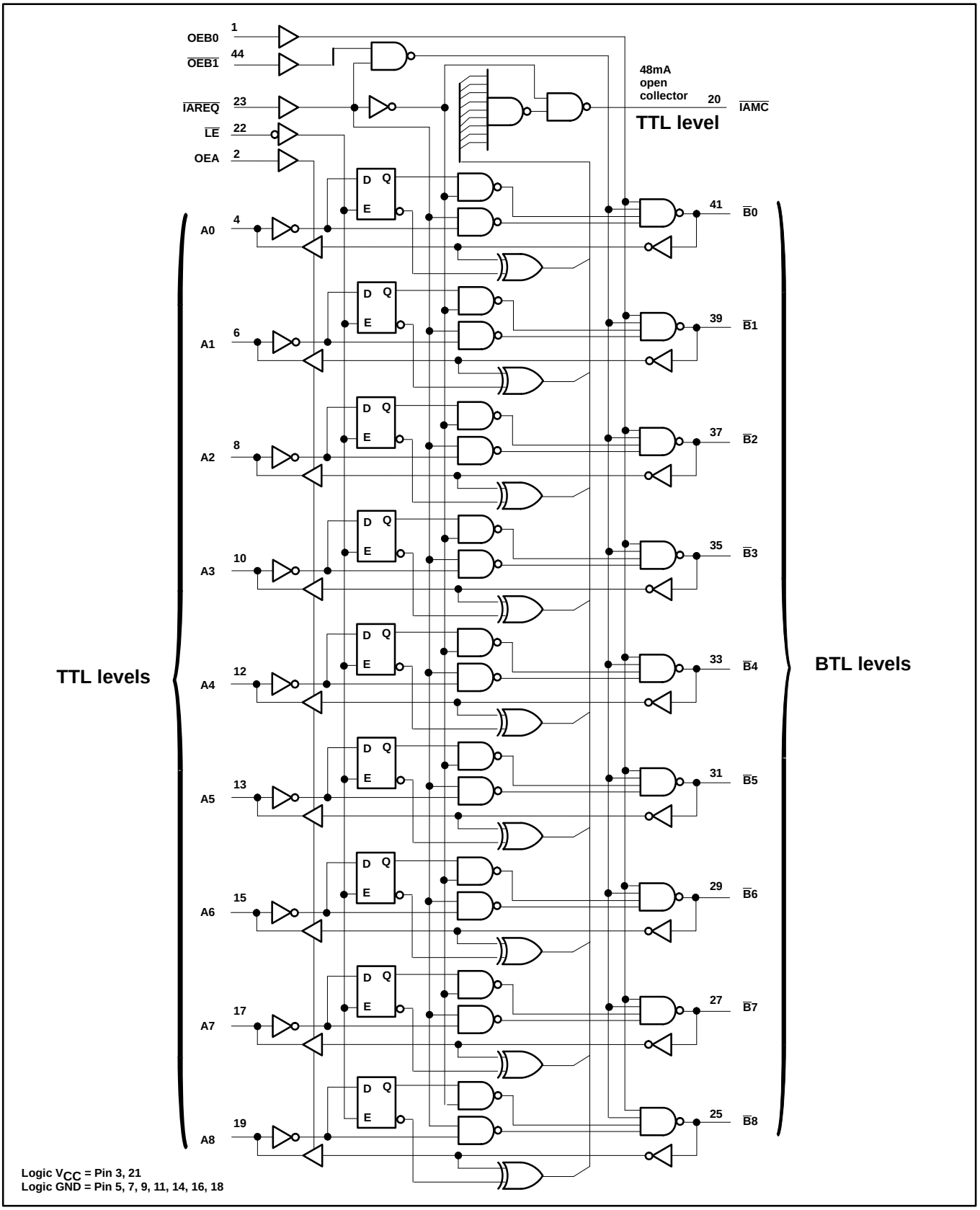
SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A8	4, 6, 8, 10, 12, 13, 15, 17, 19	I/O	Data inputs/TTL 3–state outputs
$\overline{B}0$ – $\overline{B}8$	41, 39, 37, 35, 33, 31, 29, 27, 25	I/O	Data inputs / open collector outputs, high current drives.
OEB0	1	Input	Output enable input. Enables the B outputs when high.
$\overline{OEB}1$	44	Input	Output enable input. Enables the B outputs when low.
OEA	2	Input	Output enable input. Enables the A outputs when high.
$\overline{LE}$	22	Input	Latch enable input. Enables latch when low.
$\overline{LS}$	23	Input	Latch select input. Selects latch when low (74F8965).
$\overline{IAREQ}$	23	Input	Idle arbitration request input (74F8966).
$\overline{IAMC}$	20	Output	Idle arbitration/multiple competitors output (open collector output) (74F8966).
Bus GND	26, 28, 30, 32, 34, 36, 38, 40, 42	Ground	Bus ground (0V)
Logic GND	5, 7, 9, 11, 14, 16, 18, 20 (74F8965)	Ground	Logic ground (0V)
Bus V_{CC}	24, 43	Power	Positive supply voltages
Logic V_{CC}	3, 21	Power	Positive supply voltages

LOGIC DIAGRAM FOR 74F8965



Logic V_{CC} = Pin 3, 21
Logic GND = Pin 5, 7, 9, 11, 14, 16, 18, 20

LOGIC DIAGRAM FOR 74F8966



FUNCTION TABLE FOR 74F8965

INPUTS							LATCH	OUTPUTS		OPERATING MODE
AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{LS}$	OEA	$\overline{LE}$	STATE	An	$\overline{Bn}$	
L	–	H	L	H	L	X	X	input	H**	An to $\overline{Bn}$ bypass latch
H	–	H	L	H	L	X	X	input	L	
L	–	H	L	L	L	L	H	input	H**	An to $\overline{Bn}$ transparent latch
H	–	H	L	L	L	L	L	input	L	
l	–	H	L	L	L	↑	H	input	H**	An to $\overline{Bn}$ latch and read
h	–	H	L	L	L	↑	L	input	L	
–	–	H	L	L	H	H	H	L	H**	An to $\overline{Bn}$ outputs latched and read
–	–	H	L	L	H	H	L	H	L	(preconditioned latch)
X	–	H	L	L	L	H	NC	input	L	An to $\overline{Bn}$ hold
X	X	L	X	X	X	X	X	X	H**	Disable $\overline{Bn}$ outputs
X	X	X	H	H	X	X	X	X	H**	
–	L	L	H	H	H	X	X	H	input	$\overline{Bn}$ to An
–	H	L	H	H	H	X	X	L	input	
–	X	X	X	X	L	X	X	Z	X	Disable An outputs

Notes to function table for 74F8965

1. H = High voltage level
2. h = High voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off' state
8. – = Input not externally driven
9. ↑ = Low–to–high transition
10. H**= Goes to level of pullup voltage.
11. B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

FUNCTION TABLE FOR 74F8966

INPUTS								LATCH	OUTPUTS			OPERATING MODE
AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{IAREQ}$	$\overline{LS}$	OEA	$\overline{LE}$	STATE	An	$\overline{Bn}$	$\overline{IAMC}$	
L	–	H	L	L	H	L	X	X	input	H**	H**	An to $\overline{Bn}$ bypass latch
H	–	H	L	L	H	L	X	X	input	L	H**	
L	–	H	L	L	L	L	L	H	input	H**	H**	An to $\overline{Bn}$ transparent latch
H	–	H	L	L	L	L	L	L	input	L	H**	
l	–	H	L	L	L	L	↑	H	input	H**	H**	An to $\overline{Bn}$ latch and read
h	–	H	L	L	L	L	↑	L	input	L	H**	
–	–	H	L	L	L	H	H	H	L	H**	H**	An to $\overline{Bn}$ outputs latched and read
–	–	H	L	L	L	H	H	L	H	L	H**	(preconditioned latch)
X	–	H	L	L	L	L	H	NC	input	NC	H**	An to $\overline{Bn}$ hold
X	X	L	X	X	X	X	X	X	X	H**	H**	Disable $\overline{Bn}$ outputs
X	X	X	H	H	H	X	X	X	X	H**	H**	
–	L	L	H	H	H	H	X	X	H	input	H**	$\overline{Bn}$ to An
–	H	L	H	H	H	H	X	X	L	input	H**	
–	Bn	L	H	H	↓*	H	H	$\overline{Bn}$	Z	Bn	L	Latch $\overline{Bn}$ data idle arbitration request
–	Bn	L	H	H	↓*	H	H	$\overline{Bn}$	Z	Bn	H**	(preconditioned latch)
–	X	X	X	X	X	L	X	X	Z	X	X	Disable An outputs

Notes to function table for 74F8966
1. H = High voltage level
2. h = High voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off' state
8. – = Input not externally driven
9. ↑ = Low–to–high transition
10. ↓* = High–to–low transition, latch must be preconditioned before $\overline{IAREQ}$
11. H**= Goes to level of pullup voltage.
12. B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage	OEB0, $\overline{OEB}$1, LEA, $\overline{LE}$	–0.5 to +7.0	V
		A0 – A8, $\overline{B}$0 – $\overline{B}$8	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A8	48	mA
		$\overline{IAMC}$ (74F8966 only)	96	mA
		$\overline{B}$0 – $\overline{B}$8	200	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except $\overline{B}$0 – $\overline{B}$8	2.0			V
		$\overline{B}$0 – $\overline{B}$8	1.625	1.55		V
V_{IL}	Low–level input voltage	Except $\overline{B}$0 – $\overline{B}$8			0.8	V
		$\overline{B}$0 – $\overline{B}$8			1.475	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	A0 – A8			–3	mA
V_{OH}	High–level output voltage	$\overline{IAMC}$ (74F8966 only)	4.5			V
I_{OL}	Low–level output current	A0 – A8			24	mA
		$\overline{IAMC}$ (74F8966 only)			48	mA
		$\overline{B}$0 – $\overline{B}$8			100	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High–level output current	$\overline{B}0 – \overline{B}8$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
		$\overline{IAMC}$ (74F8966)	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V				100	µA
I_{OFF}	Power–off output current	$\overline{B}0 – \overline{B}8$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
		$\overline{IAMC}$ (74F8966)	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V				100	µA
V_{OH}	High-level output voltage	A0 – A8[4]	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –3mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	A0 – A8[4]	V_{CC} = MIN,	I_{OL} = 24mA			0.50	V
		$\overline{IAMC}$ (74F8966)	V_{IL} = MAX	I_{OL} = 48mA			0.50	V
		$\overline{B}0 – \overline{B}8$	V_{IH} = MIN	I_{OL} = 100mA	0.75	1.0	1.10	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	OEB0, $\overline{OEB}1$, OEA, $\overline{LE}$, $\overline{LS}$, $\overline{IAREQ}$	V_{CC} = MAX, V_I = 7.0V				100	µA
		A0 – A8, $\overline{B}0 – \overline{B}8$	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	OEB0, $\overline{OEB}1$, OEA, $\overline{LE}$, $\overline{LS}$, $\overline{IAREQ}$	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{B}0 – \overline{B}8$	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	OEB0, $\overline{OEB}1$, OEA, $\overline{LE}$, $\overline{LS}$, $\overline{IAREQ}$	V_{CC} = MAX, V_I = 0.5V				–100	µA
		$\overline{B}0 – \overline{B}8$	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{IH} + I_{OZH}	Off–state output current, high–level voltage applied	A0 – A8	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{IL} + I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short circuit output current[3]	A0 – A8 only AO8	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			80	140	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			85	145	mA
		I_{CCZ}				75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8V and V_{IL} = 1.3V.

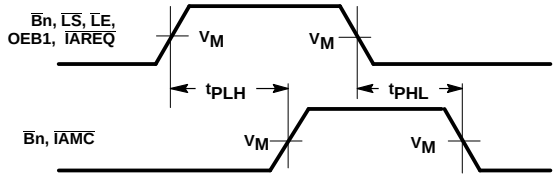
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{B}$n to An	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 5, 6	7.5 9.0	9.0 11.0	12.0 13.5	6.0 7.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output disable from high or low, OEA to An	Waveform 5, 6	3.0 4.0	5.0 6.0	8.0 9.0	2.5 4.0	9.0 10.0	ns
$t_{sk(o)}$	Skew between receivers in same package	Waveform 4		0.5	1.0		1.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{B}$n (transparent latch)	Waveform 2	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{B}$n (bypass latch)	Waveform 2	1.0 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to $\overline{B}$n	Waveform 1, 2	3.0 4.0	5.0 5.5	8.0 8.5	3.0 3.5	8.5 9.5	ns
t_{PLH} t_{PHL}	Output enable/disable time, OEB0 to $\overline{B}$n	Waveform 2	4.0 5.0	6.0 6.5	8.5 9.5	3.5 3.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Output enable/disable time, $\overline{OEB}$1 to $\overline{B}$n	Waveform 1	5.5 3.0	7.5 5.0	10.0 8.0	5.0 2.5	11.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{IAREQ}$ or $\overline{LS}$ to $\overline{B}$n	Waveform 1, 2	4.5 2.0	7.5 6.5	10.0 9.5	4.0 2.0	11.0 11.0	ns
t_{TLH} t_{THL}	Transition time, $\overline{B}$n port 10% to 90%, 90% to 10%	Test circuit and waveforms		2.0 2.0		1.0 1.0	3.0 3.0	ns
$t_{sk(o)}$	Skew between drivers in same package	Waveform 4		1.0	2.0		2.0	ns
SYMBOL	PARAMETER	TEST CONDITION	$\overline{IAMC}$ PORT LIMITS (74F8966 only)					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{IAMC}$ (latches preset)	Waveform 2	10.5 7.0	14.5 12.0	18.0 15.0	9.5 6.0	20.0 17.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{IAREQ}$ to $\overline{IAMC}$	Waveform 2	6.5 2.5	8.0 4.5	11.0 7.0	6.0 2.0	11.5 8.0	ns

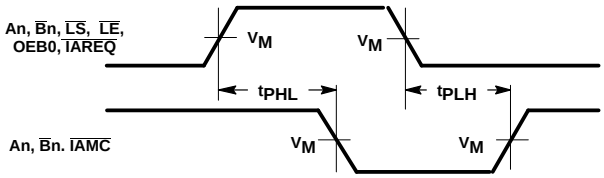
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{LE}$	Waveform 3	2.5 0.0			3.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{LE}$	Waveform 3	4.0 2.5			5.0 3.0		ns
$t_w(L)$	$\overline{LE}$ pulse width, low	Waveform 3	4.0			4.5		ns

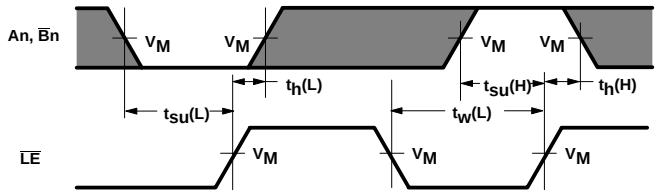
AC WAVEFORMS



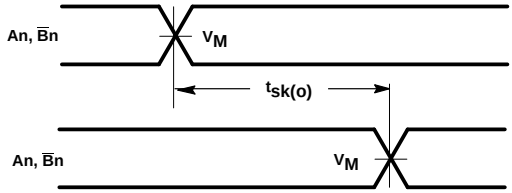
Waveform 1. Propagation delay for data or output enable to output



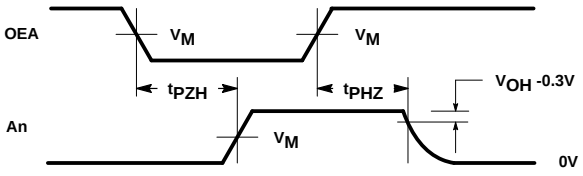
Waveform 2. Propagation delay for data or output enable to output



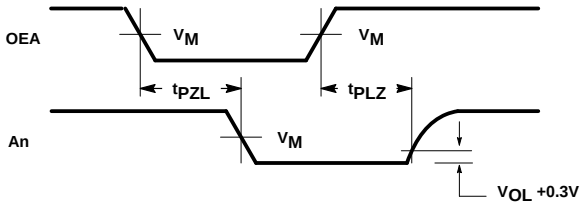
Waveform 3. Data setup and hold times and $\overline{LE}$ pulse width



Waveform 4. Output skew



Waveform 5. 3–state output enable time to high level and output disable time from high level



Waveform 6. 3-state output enable time to low level and output disable time from low level

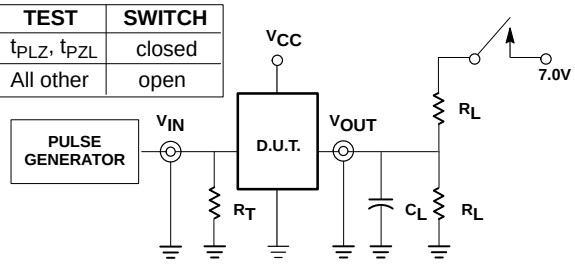
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

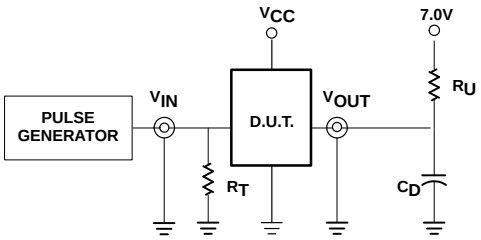
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

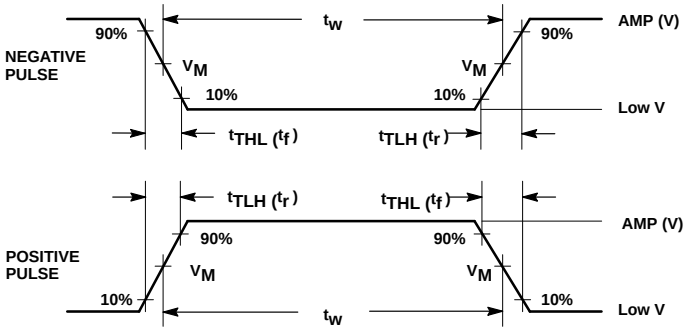
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family 74F	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	3.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.