

DATA SHEET

74AHC2G125; 74AHCT2G125 Bus buffer/line driver; 3-state

Product specification

2004 Jan 13

Bus buffer/line driver; 3-state**74AHC2G125; 74AHCT2G125****FEATURES**

- Symmetrical output impedance
- High noise immunity
- ESD protection:
 - HBM EIA/JESD22-A114-A exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
 - CDM EIA/JESD22-C101 exceeds 1000 V.
- Low power dissipation
- Balanced propagation delays
- SOT505-2 and SOT765-1 package
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74AHC2G/AHCT2G125 is a high-speed Si-gate CMOS device.

The 74AHC2G/AHCT2G125 provides a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ($\overline{\text{nOE}}$). A HIGH at pin $\overline{\text{nOE}}$ causes the output to assume a high-impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; $T_{\text{amb}} = 25\text{ °C}$; $t_r = t_f \leq 3.0\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC2G	AHCT2G	
$t_{\text{PHL}}/t_{\text{PLH}}$	propagation delay nA to nY	$C_L = 15\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	3.4	3.4	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}$; $f = 1\text{ MHz}$; notes 1 and 2	9	11	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \sum (C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\sum (C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_I = \text{GND to } V_{\text{CC}}$.

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
$\overline{\text{nOE}}$	nA	nY
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

ORDERING INFORMATION

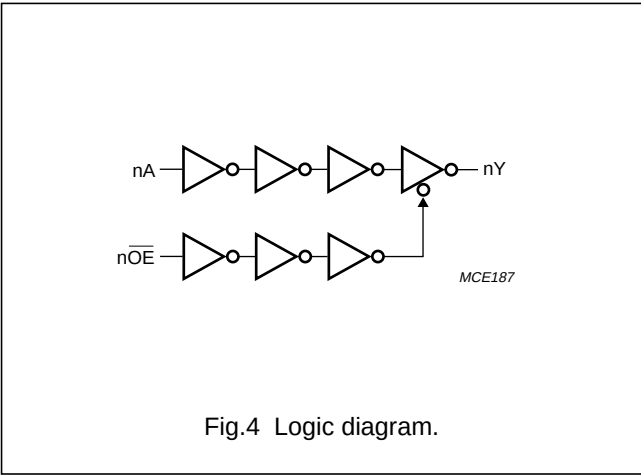
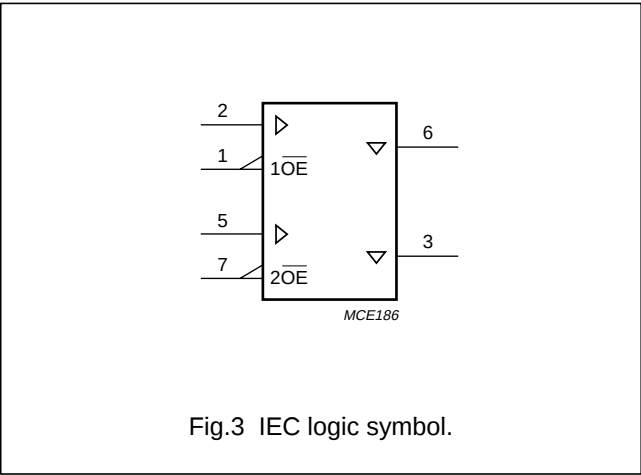
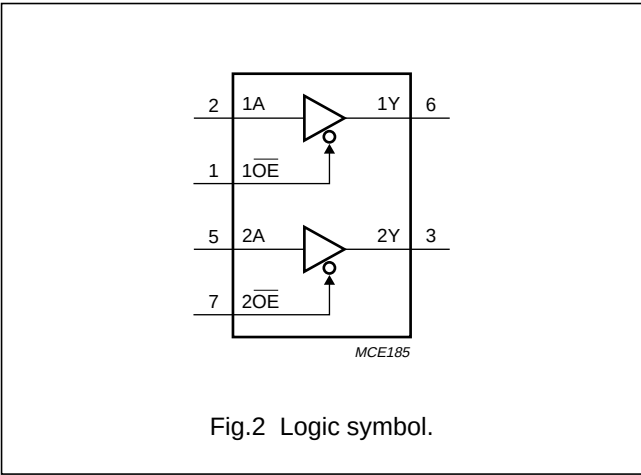
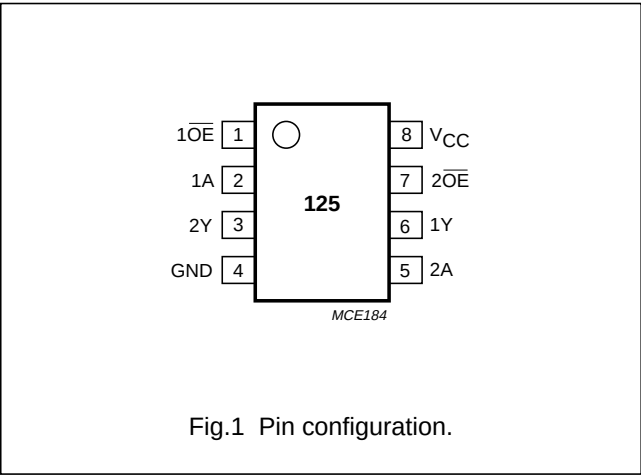
TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC2G125DP	−40 to +125 °C	8	TSSOP8	plastic	SOT505-2	A25
74AHCT2G125DP	−40 to +125 °C	8	TSSOP8	plastic	SOT505-2	C25
74AHC2G125DC	−40 to +125 °C	8	VSSOP8	plastic	SOT765-1	A25
74AHCT2G125DC	−40 to +125 °C	8	VSSOP8	plastic	SOT765-1	C25

PINNING

PIN	SYMBOL	DESCRIPTION
1	1OE	output enable input (active LOW)
2	1A	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	1Y	data output
7	2OE	output enable input (active LOW)
8	V _{CC}	supply voltage

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125



Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC2G125			74AHCT2G125			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 3.3 \pm 0.3$ V	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 \pm 0.5$ V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V	–	–20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	± 20	mA
I_O	output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V	–	± 25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	± 75	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40$ to $+125$ °C	–	250	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

DC CHARACTERISTICS

Type 74AHC2G125

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –50 μA	2.0	1.9	2.0	–	V
		I _O = –50 μA	3.0	2.9	3.0	–	V
		I _O = –50 μA	4.5	4.4	4.5	–	V
		I _O = –4.0 mA	3.0	2.58	–	–	V
		I _O = –8.0 mA	4.5	3.94	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	2.0	–	0	0.1	V
		I _O = 50 μA	3.0	–	0	0.1	V
		I _O = 50 μA	4.5	–	0	0.1	V
		I _O = 4.0 mA	3.0	–	–	0.36	V
		I _O = 8.0 mA	4.5	–	–	0.36	V
I _{OZ}	3-state output OFF-state current	V _I = V _{CC} or GND	5.5	–	–	0.25	μA
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	1.0	μA
C _I	input capacitance		–	–	1.5	10	pF

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = −50 μA	2.0	1.9	–	–	V
		I _O = −50 μA	3.0	2.9	–	–	V
		I _O = −50 μA	4.5	4.4	–	–	V
		I _O = −4.0 mA	3.0	2.48	–	–	V
		I _O = −8.0 mA	4.5	3.8	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	2.0	–	–	0.1	V
		I _O = 50 μA	3.0	–	–	0.1	V
		I _O = 50 μA	4.5	–	–	0.1	V
		I _O = 4.0 mA	3.0	–	–	0.44	V
		I _O = 8.0 mA	4.5	–	–	0.44	V
I _{OZ}	3-state output OFF-state current	V _I = V _{CC} or GND	5.5	–	–	2.5	μA
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	10	μA
C _I	input capacitance		–	–	–	10	pF

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = −50 μA	2.0	1.9	–	–	V
		I _O = −50 μA	3.0	2.9	–	–	V
		I _O = −50 μA	4.5	4.4	–	–	V
		I _O = −4.0 mA	3.0	2.40	–	–	V
		I _O = −8.0 mA	4.5	3.70	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	2.0	–	–	0.1	V
		I _O = 50 μA	3.0	–	–	0.1	V
		I _O = 50 μA	4.5	–	–	0.1	V
		I _O = 4.0 mA	3.0	–	–	0.55	V
		I _O = 8.0 mA	4.5	–	–	0.55	V
I _{OZ}	3-state output OFF-state current	V _I = V _{CC} or GND	5.5	–	–	10	μA
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	2.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	μA
C _I	input capacitance		–	–	–	10	pF

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

Type 74AHCT2G125

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –50 μA	4.5	4.4	4.5	–	V
		I _O = –8.0 mA	4.5	3.94	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	4.5	–	0	0.1	V
		I _O = 8.0 mA	4.5	–	–	0.36	V
I _{OZ}	3-state output OFF-state current	V _I = V _{CC} or GND	5.5	–	–	0.25	μA
I _{LI}	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	1.0	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	1.35	mA
C _I	input capacitance			–	1.5	10	pF
T _{amb} = –40 to +85 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –50 μA	4.5	4.4	–	–	V
		I _O = –8.0 mA	4.5	3.8	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	4.5	–	–	0.1	V
		I _O = 8.0 mA	4.5	–	–	0.44	V
I _{OZ}	3-state output OFF-state current	V _I = V _{CC} or GND	5.5	–	–	2.5	μA
I _{LI}	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	10	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	1.5	mA
C _I	input capacitance		–	–	–	10	pF

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	—	—	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	—	—	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = −50 μA	4.5	4.4	—	—	V
		I _O = −8.0 mA	4.5	3.70	—	—	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	4.5	—	—	0.1	V
		I _O = 8.0 mA	4.5	—	—	0.55	V
I _{OZ}	3-state output OFF-state current	V _I = V _{CC} or GND	5.5	—	—	10	μA
I _{LI}	input leakage current	V _I = V _{IH} or V _{IL}	5.5	—	—	2.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	—	—	40	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0	5.5	—	—	1.5	mA
C _I	input capacitance		—	—	—	10	pF

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

AC CHARACTERISTICS

Type 74AHC2G125

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
T _{amb} = 25 °C							
V _{CC} = 3.0 to 3.6 V; note 1							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	–	4.7	8.0	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	–	5.0	8.0	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	–	6.0	9.7	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	–	6.6	11.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	–	6.9	11.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	–	8.3	13.2	ns
V _{CC} = 4.5 to 5.5 V; note 2							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	–	3.4	5.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	–	3.6	5.1	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	–	4.1	6.8	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	–	4.8	7.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	–	4.9	7.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	–	5.7	8.8	ns
T _{amb} = –40 to +85 °C							
V _{CC} = 3.0 to 3.6 V; note 1							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	9.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	9.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	11.5	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	13.0	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	13.0	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	15.0	ns
V _{CC} = 4.5 to 5.5 V; note 2							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	6.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	6.0	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	8.0	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	8.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	8.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	10.0	ns

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
T _{amb} = −40 to +125 °C							
V _{CC} = 3.0 to 3.6 V; note 1							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	11.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	11.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	12.5	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	14.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	14.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	16.5	ns
V _{CC} = 4.5 to 5.5 V; note 2							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	7.0	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	6.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	8.5	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	9.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	9.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	11.0	ns

Notes

1. All typical values are measured at V_{CC} = 3.3 V.
2. All typical values are measured at V_{CC} = 5.0 V.

Type 74AHCT2G125

GND = 0 V; t_r = t_f ≤ 3.0 ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
T _{amb} = 25 °C							
V _{CC} = 4.5 to 5.5 V; note 1							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	–	3.4	5.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	–	3.9	5.1	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	–	4.5	6.8	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	–	4.8	7.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	–	5.1	7.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	–	6.1	8.8	ns
T _{amb} = –40 to +85 °C							
V _{CC} = 4.5 to 5.5 V							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	6.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	6.0	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	8.0	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	8.5	ns

Bus buffer/line driver; 3-state

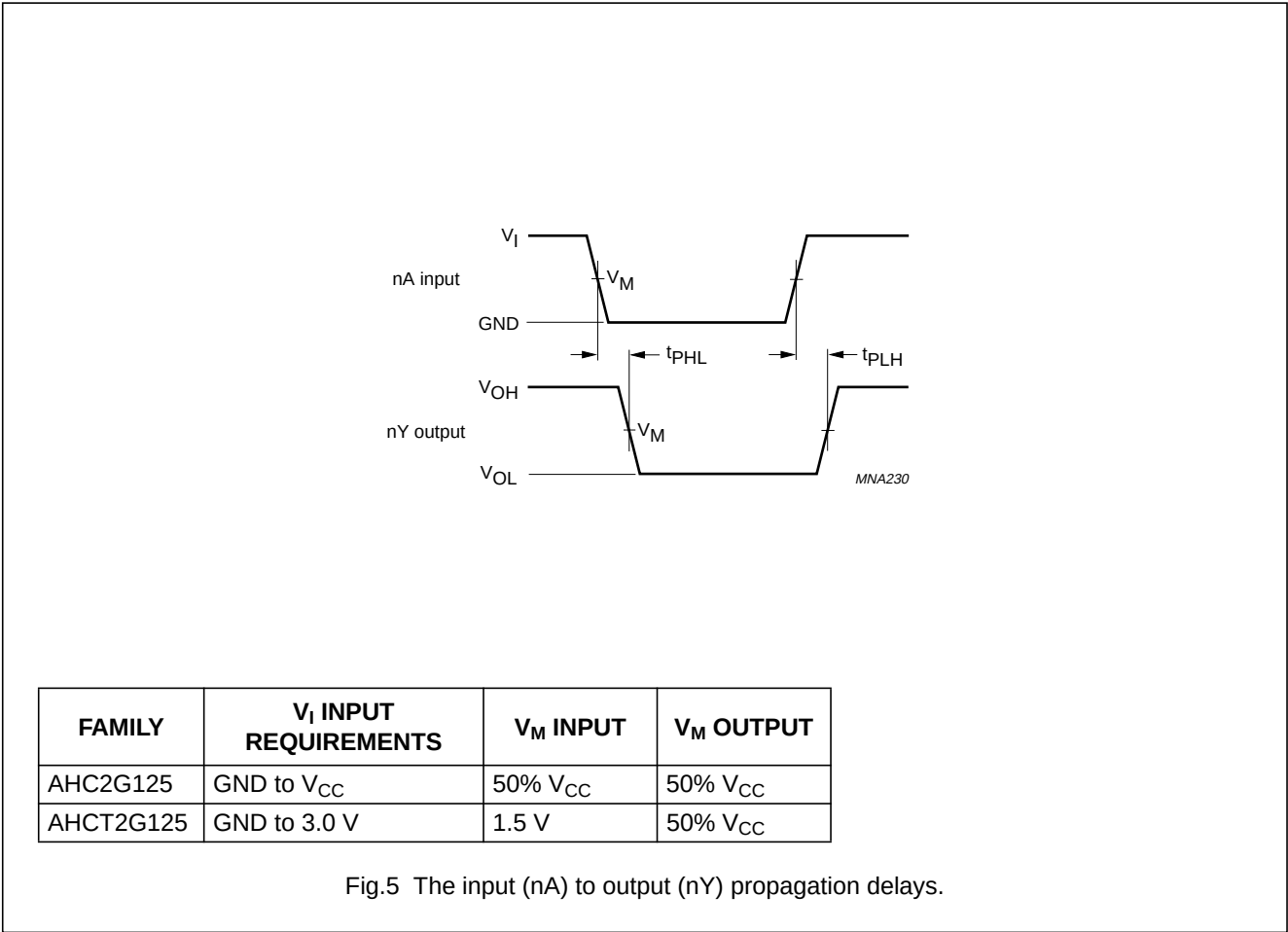
74AHC2G125; 74AHCT2G125

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	8.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	10.0	ns
T _{amb} = –40 to +125 °C							
V _{CC} = 4.5 to 5.5 V							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	6.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	6.0	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	15	1.0	–	8.0	ns
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	8.5	ns
t _{PZH} /t _{PZL}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	8.5	ns
t _{PHZ} /t _{PLZ}	propagation delay n $\overline{\text{OE}}$ to nY	see Figs 6 and 7	50	1.0	–	10.0	ns

Note

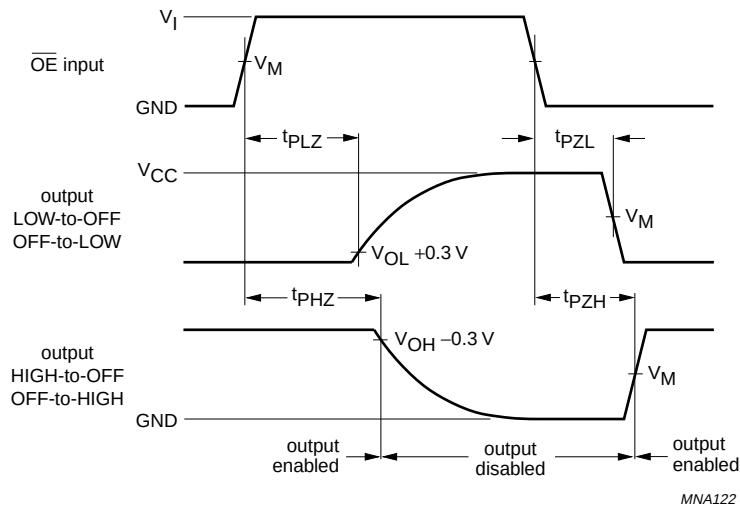
1. All typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS



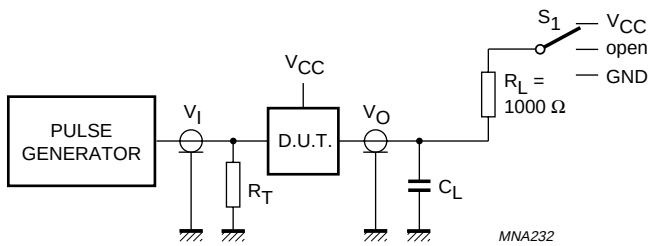
Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125



FAMILY	V _I INPUT REQUIREMENTS	V _M INPUT	V _M OUTPUT
AHC2G125	GND to V _{CC}	50% V _{CC}	50% V _{CC}
AHCT2G125	GND to 3.0 V	1.5 V	50% V _{CC}

Fig.6 The 3-state enable and disable times.



TEST	S ₁
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND

Definitions for test circuit:
R_L = load resistance.
C_L = load capacitance including jig and probe capacitance (see Chapter “AC characteristics” for the value).
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

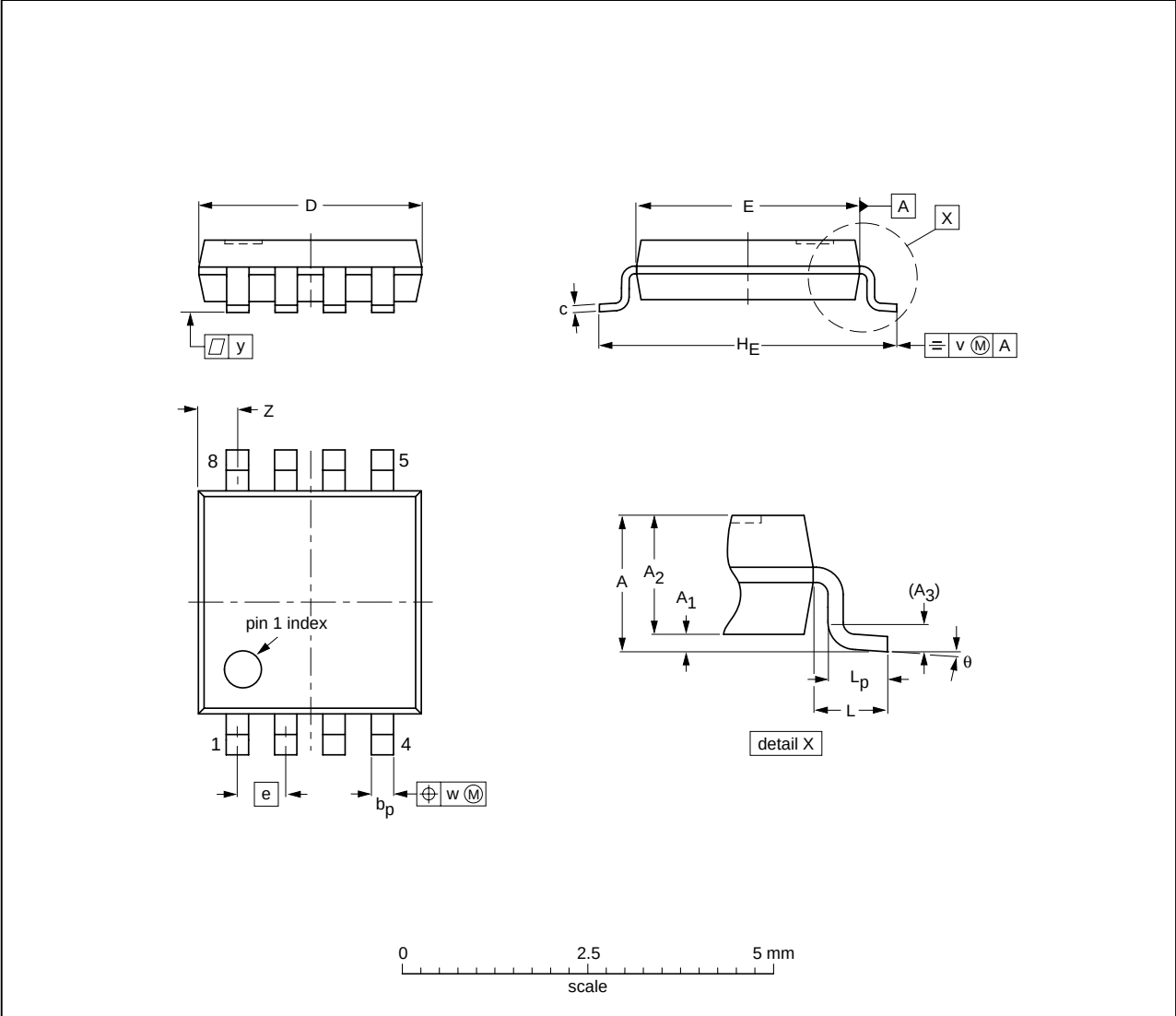
Fig.7 Load circuitry for switching times.

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

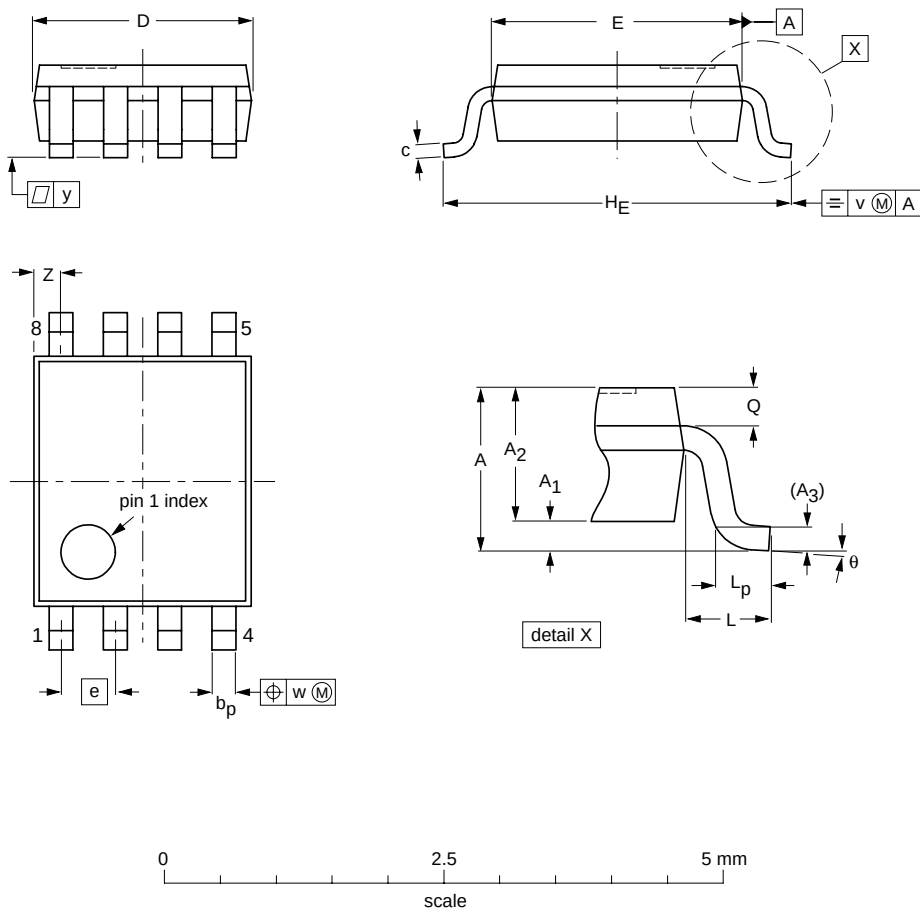
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Bus buffer/line driver; 3-state

74AHC2G125; 74AHCT2G125

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2004

SCA76

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R44/01/pp18

Date of release: 2004 Jan 13

Document order number: 9397 750 12426

Let's make things better.

**Philips
Semiconductors**



PHILIPS