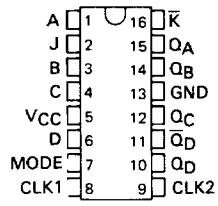
DECEMBER 1972—REVISED DECEMBER 1983

- N-Bit Serial-to-Parallel Converter
- N-Bit Parallel-to-Serial Converter
- N-Bit Storage Register
- J-$\overline{K}$ Serial Input

SN54L99 . . . J PACKAGE
(TOP VIEW)



description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flop and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on a high-to-low transition of clock 1 when the mode control is low. Serial data for the right-shift mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, a D-type, or T-type flip-flop as shown in the function table. Shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.). Serial data for this mode is entered at the D input. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

FUNCTION TABLE

INPUTS									OUTPUTS				
MODE	CLOCKS		SERIAL		PARALLEL								
CONTROL	2 (L)	1 (R)	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
H	H	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	↓	X	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	↓	X	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d	$\overline{d}$
L	L	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
L	X	↓	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	X	↓	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	X	↓	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	X	↓	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
↑	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↓	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↓	L	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↑	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↑	H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$

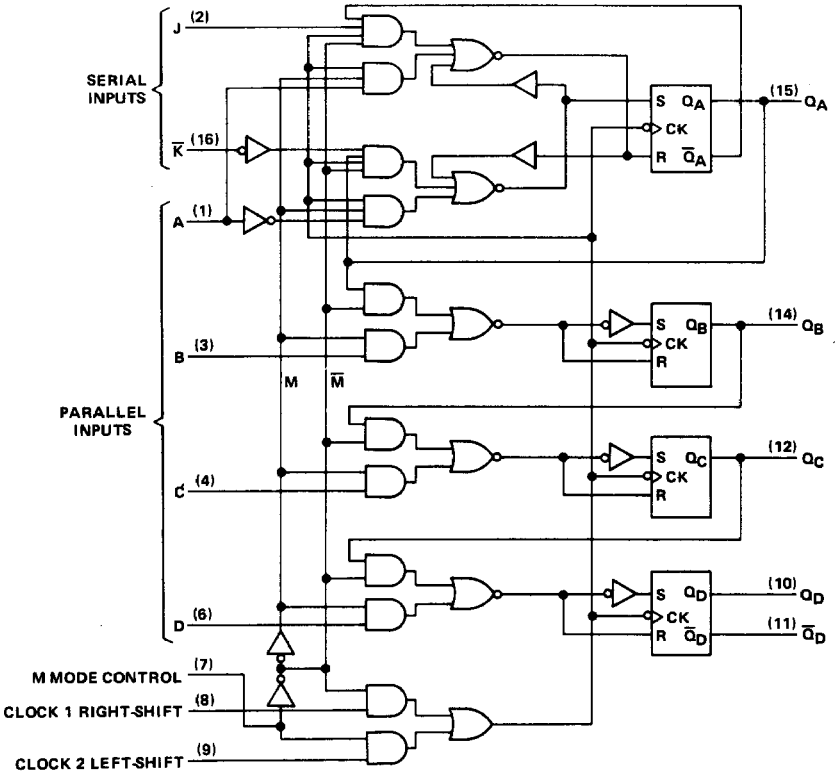
†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level.
a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

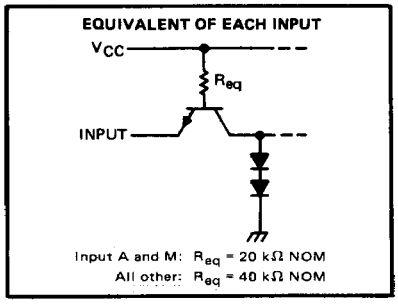
PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

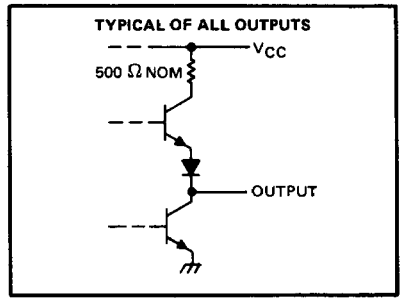
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logic diagram



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . − 55°C to 125°C
Storage temperature range . . . . . − 65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L99			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.7	V
I_{OH}	High-level output current			− 0.1	mA
I_{OL}	Low-level output current			2	mA
$t_{w(clock)}$	Width of clock pulse	200			ns
$t_{su(H)}$	Setup time for high-level data at J, $\overline{K}$, A, B, C, or D inputs	100			ns
$t_{su(L)}$	Setup time for low-level data at J, $\overline{K}$, A, B, C, or D inputs	120			ns
t_h	Hold time at J, $\overline{K}$, A, B, C, or D inputs	0			ns
$t_{enable\ 1}$	Time to enable clock 1 (See Figure 1)	225			ns
$t_{enable\ 2}$	Time to enable clock 2 (See Figure 1)	200			ns
$t_{inhibit\ 1}$	Time to inhibit clock 1 (See Figure 1)	100			ns
$t_{inhibit\ 2}$	Time to inhibit clock 2 (See Figure 1)	0			ns
T_A	Operating free-air temperature	− 55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54L99			UNIT
			MIN	TYP‡	MAX	
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = − 0.1 mA	2.4	3.3		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = 2 mA		0.15	0.3	V
I_I	J, $\overline{K}$, B, C, or D	V_{CC} = MAX, V_I = 5.5 V			0.1	mA
	M or A				0.2	
I_{IH}	J, $\overline{K}$, B, C, or D	V_{CC} = MAX, V_I = 2.4 V			10	μA
	M or A				20	
I_{IL}	J, $\overline{K}$, B, C, or D	V_{CC} = MAX, V_I = 0.3 V			− 0.18	mA
	M or A				− 0.36	
I_{OS} §		V_{CC} = MAX	− 3		− 15	mA
I_{CC}		V_{CC} = MAX, See Note 3		3.8	9	mA

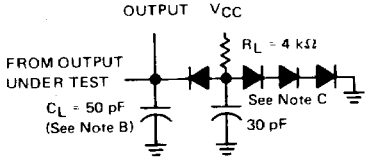
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: With all outputs and J and $\overline{K}$ inputs open, mode control at 4.5 V, inputs A through D grounded, I_{CC} is measured after a momentary 3 V, then ground is applied to both clock inputs.

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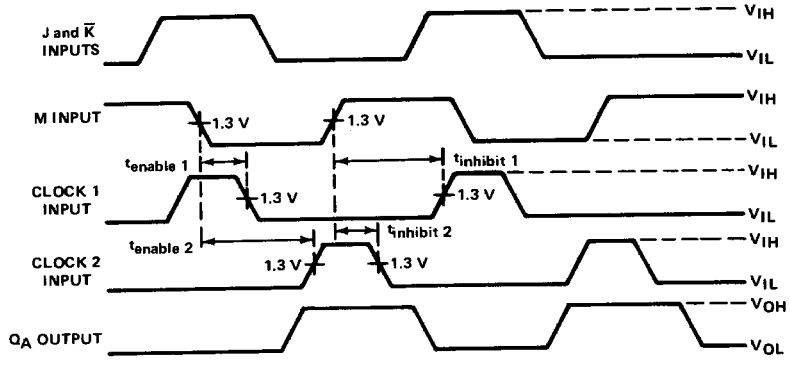
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Any	Any	R_L = 4 kΩ, C_L = 50 pF See Figures 1 and 2	3	5		MHz
t_{PLH}					115	200	ns
t_{PHL}					125	200	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

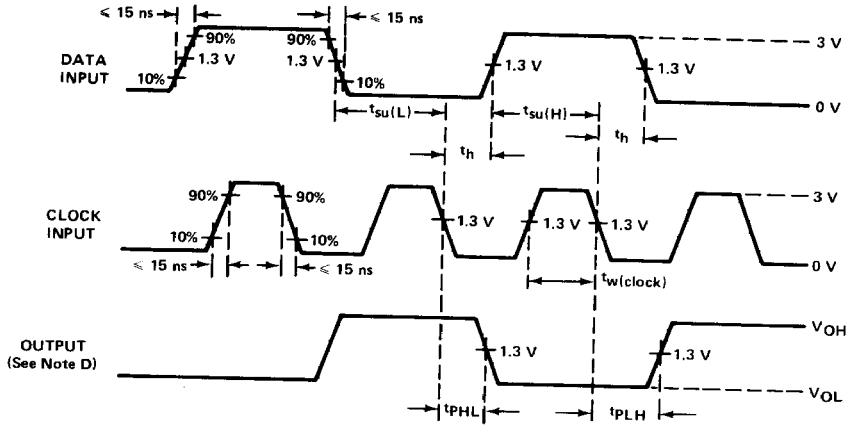


NOTE: A input is at the low level.

VOLTAGE WAVEFORMS
FIGURE 1–CLOCK ENABLE/INHIBIT TIMES

NOTES: A. The input waveforms are supplied by pulse generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)}$ = 120 ns, and $t_{setup(H)}$ = 100 ns. For clock pulse generator: $t_w \geq 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. When data input is applied to J and K inputs, the output waveform applies only to output Q_A.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 2–SWITCHING TIMES

NOTES: A. The input waveforms are supplied by pulse generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)} = 120$ ns, and $t_{setup(H)} = 100$ ns. For clock pulse generator: $t_w = 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

D. When data input is applied to J and $\overline{K}$ inputs, the output waveform applies only to output Q_A.

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