DS26C32AMQML

DS26C32AMQML Quad Differential Line Receiver



Literature Number: SNOSAS3

National Semiconductor

October 26, 2010

DS26C32AMQML

Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE ® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

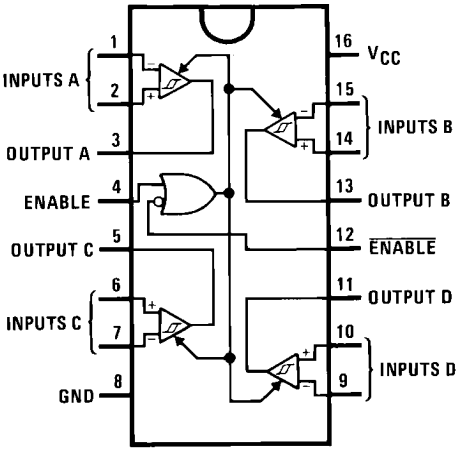
- CMOS design for low power
- ±0.2V sensitivity over input common mode voltage range
- Input fail-safe circuitry.
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS26C32AME/883	5962–9164001M2A	E20A	20LD Leadless Chip Carrier
DS26C32AMJ/883	5962–9164001MEA	J16A	16LD Ceramic Dip
DS26C32AMW/883	5962–9164001MFA	W16A	16LD Ceramic Flatpack
DS26C32AMWG/883	5962–9164001MXA	WG16A	16LD Ceramic SOIC

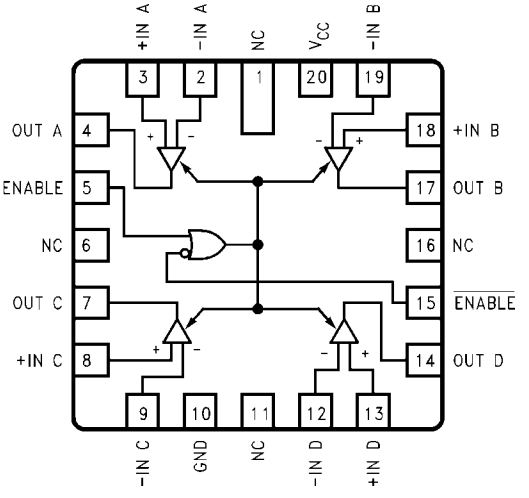
Connection Diagrams

Dual-In-Line Package



Top View
See NS Package J16A, WG16A, or W16A

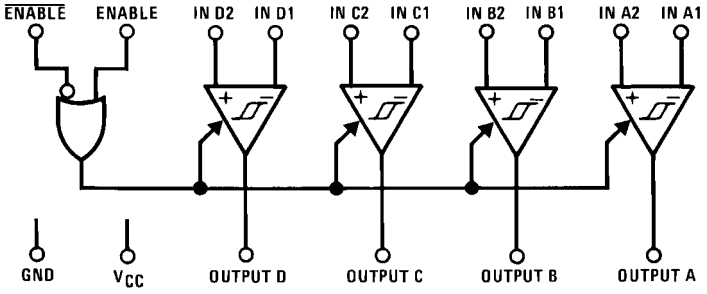
20-Lead Ceramic Leadless Chip Carrier



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Logic Diagram



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{Th}$ (Max)	H
		$V_{ID} \leq V_{Th}$ (Min)	L
		Open	H

Z = TRI-STATE

Absolute Maximum Ratings (*Note 2*, *Note 1*)

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{Diff})	±14V
Enable Input Voltage (V_I)	7V
Storage Temperature Range (T_{Stg})	−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)	−55	+125	°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS26C32AM Electrical Characteristics

DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{TH}	Minimum Differential Input Voltage	V_{CC} = 5V, V_O = V_{OH} or V_{OL}, -7 < V_{CM} < +7		-200	+200	mV	1, 2, 3
R_I	Input Resistance	V_{CC} = 5V, -7 < V_{CM} < +7, One input AC Gnd		4.5	11	KΩ	1, 2, 3
I_I	Input Current	V_{CC} = 5V, V_I = +10V, Other Input = Gnd			+1.8	mA	1, 2, 3
		V_{CC} = 5V, V_I = -10V, Other Input = Gnd			-2.7	mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, V_{Diff} = +1V, I_O = -6.0mA		3.8		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 5.5V, V_{CC} = Max, V_{Diff} = -1V, I_O = 6.0mA			0.3	V	1, 2, 3
V_{IH}	Minimum Enable High Level Voltage		(*Note 3*)	2.0		V	1, 2, 3
V_{IL}	Maximum Enable Low Level Voltage		(*Note 3*)		0.8	V	1, 2, 3
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_O = V_{CC} or Gnd, Enable = V_{IL}, $\overline{\text{Enable}}$ = V_{IH}			±5.0	µA	1, 2, 3
I_I	Maximum Enable Input Current	V_I = V_{CC} or Gnd			±1.0	µA	1, 2, 3
I_{CC}	Quiescent Power Supply Current	V_{Diff} = +1V, V_{CC} = 5.5V			25	mA	1, 2, 3

AC Parameters - Propagation Delay Time

The following conditions apply, unless otherwise specified. V_{CC} = 5V ±10%, C_{CL} = 50pF, V_{Diff} = 2.5V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PLH}	Input to Output Prop Delay	V_{CM} = 0V			35	ns	9, 10, 11
t_{PHL}	Input to Output Prop Delay	V_{CM} = 0V			35	ns	9, 10, 11
t_{Rise}	Output Rise Time	V_{CM} = 0V			9	ns	9, 10, 11
t_{Fall}	Output Fall Time	V_{CM} = 0V			9	ns	9, 10, 11
t_{PLZ}	Output Disable Time	R_L = 1000Ω			29	ns	9, 10, 11
t_{PZL}	Output Enable Time	R_L = 1000Ω			29	ns	9, 10, 11
t_{PHZ}	Output Disable Time	R_L = 1000Ω			29	ns	9, 10, 11
t_{PZH}	Output Enable Time	R_L = 1000Ω			29	ns	9, 10, 11

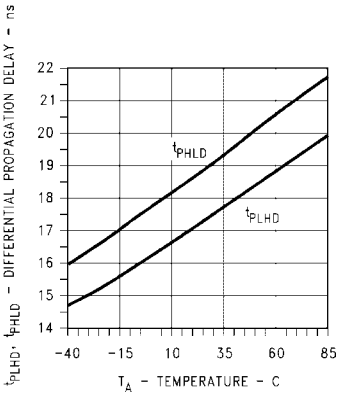
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Parameter tested Go-No-Go only.

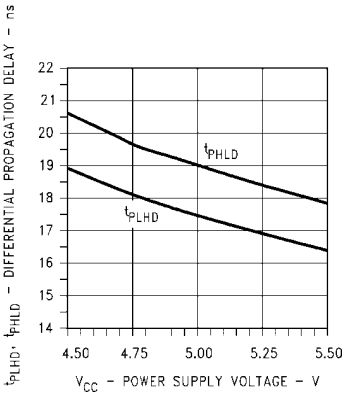
Typical Performance Characteristics

Differential Propagation Delay vs Temperature



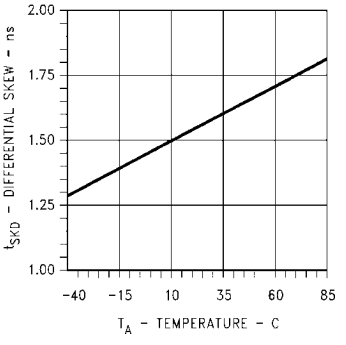
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Differential Propagation Delay vs Power Supply Voltage



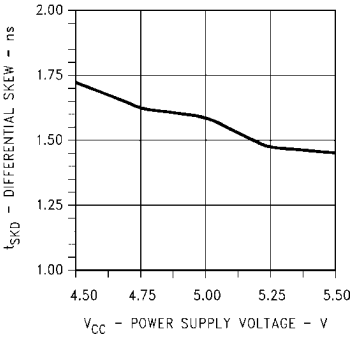
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Differential Skew vs Temperature



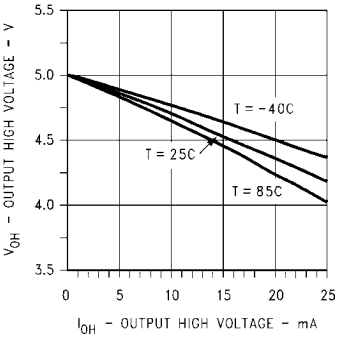
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Differential Skew vs Power Supply Voltage



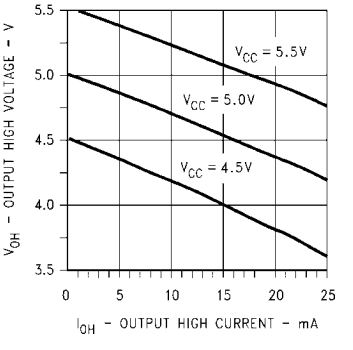
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Output High Voltage vs Output High Current



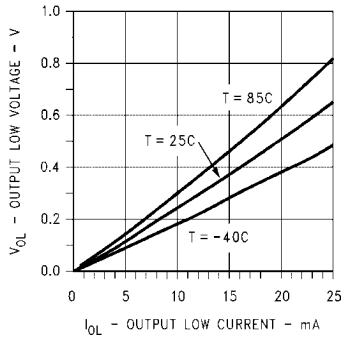
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Output High Voltage vs Output High Current



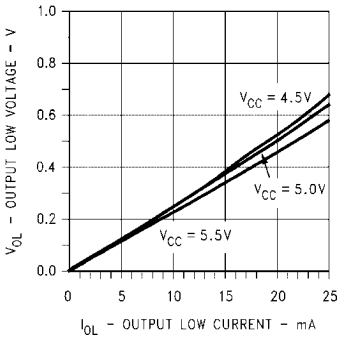
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Output Low Voltage vs Output Low Current



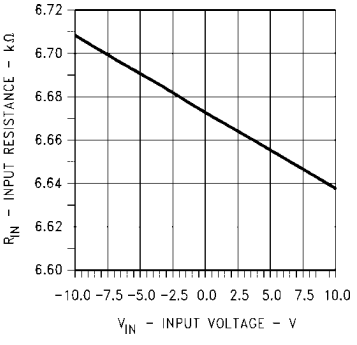
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Output Low Voltage vs Output Low Current



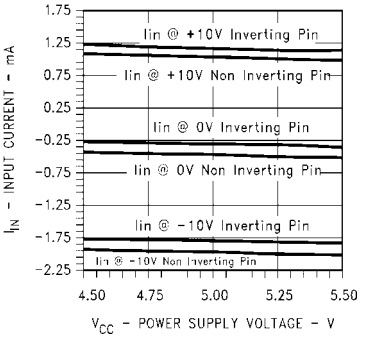
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Input Resistance vs Input Voltage



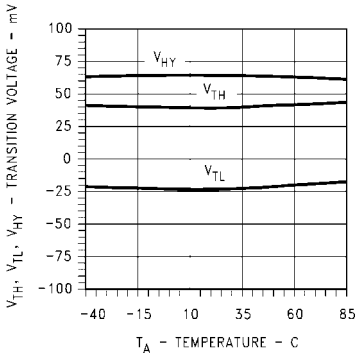
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Input Current vs Power Supply Voltage



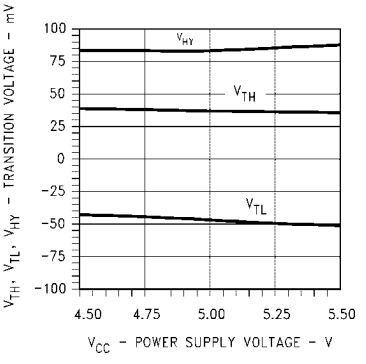
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Hysteresis & Differential Transition Voltage vs Temperature



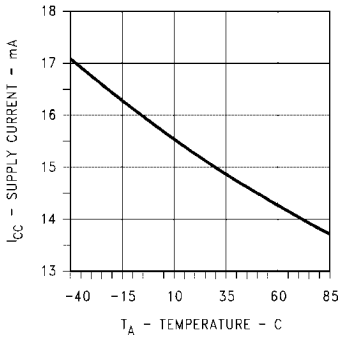
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Hysteresis & Differential Transition Voltage vs Power Supply Voltage



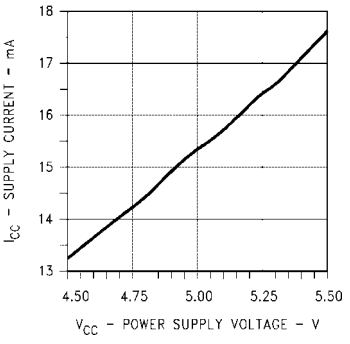
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Supply Current vs Temperature



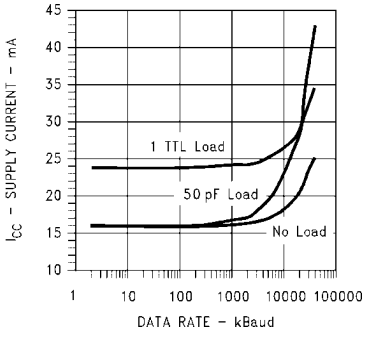
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Disabled Supply Current vs Power Supply Voltage



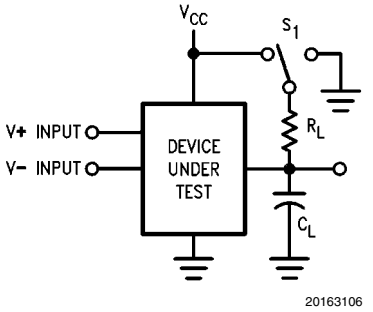
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Supply Current vs Data Rate



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AC Test Circuit and Switching Time Waveforms



C_L includes load and test jig capacitance.
$S_1 = V_{CC}$ for t_{PZL}, and t_{PLZ} measurements.
S_1 = Gnd for t_{PZH}, and t_{PHZ} measurements.

FIGURE 1. Test Circuit for TRI-STATE Output Tests

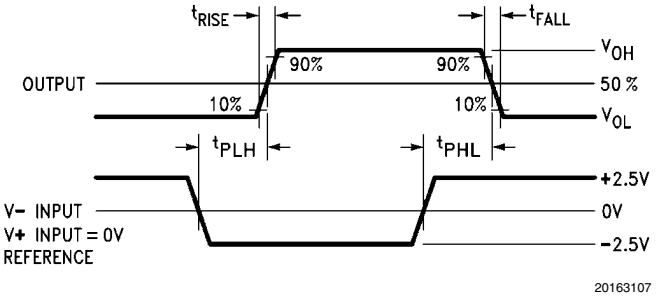


FIGURE 2. Propagation Delay

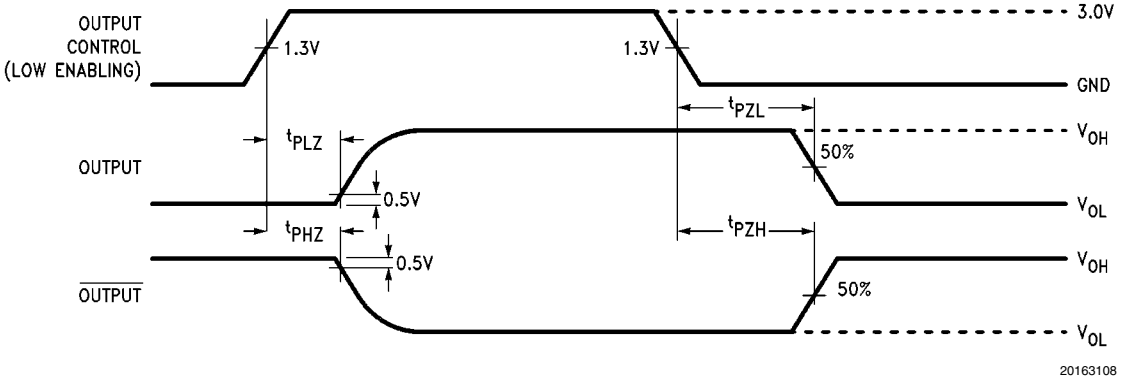
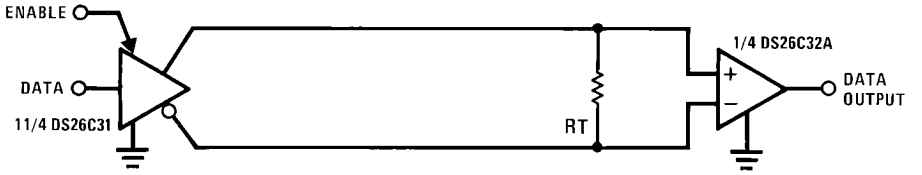


FIGURE 3. TRI-STATE®Output Enable and Disable Waveforms

Typical Applications

Two-Wire Balanced Systems, RS-422

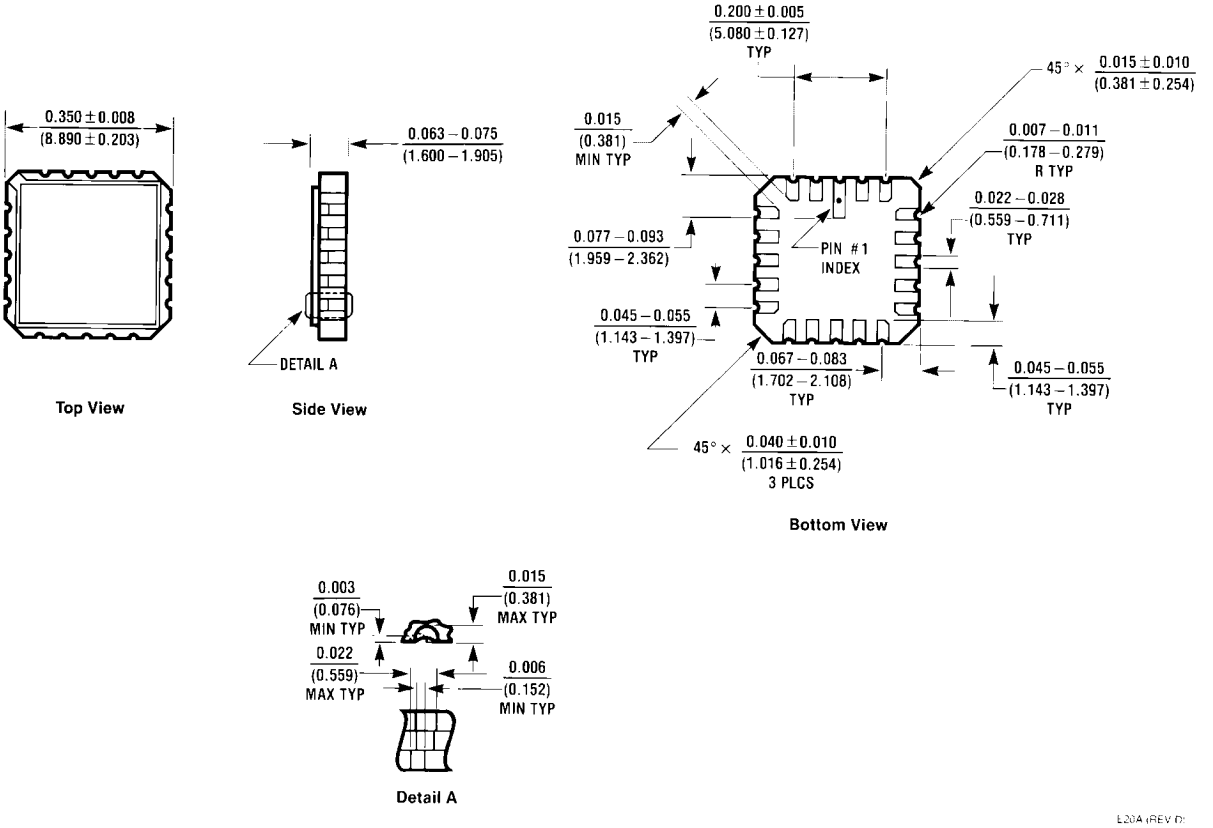


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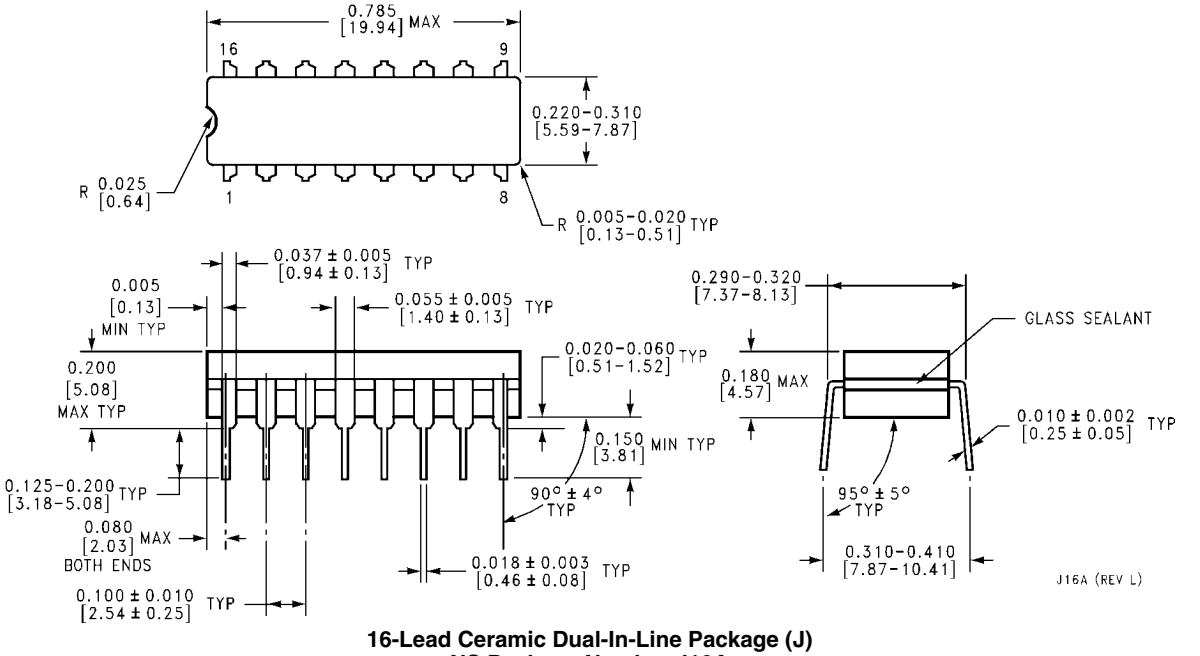
Revision History Section

Released	Revision	Section	Changes
10/26/2010	A	New Release, Corporate format	MDS data sheets converted into one Corp. data sheet format. MNDS26C32AM-X Rev 0B0 will be archived.

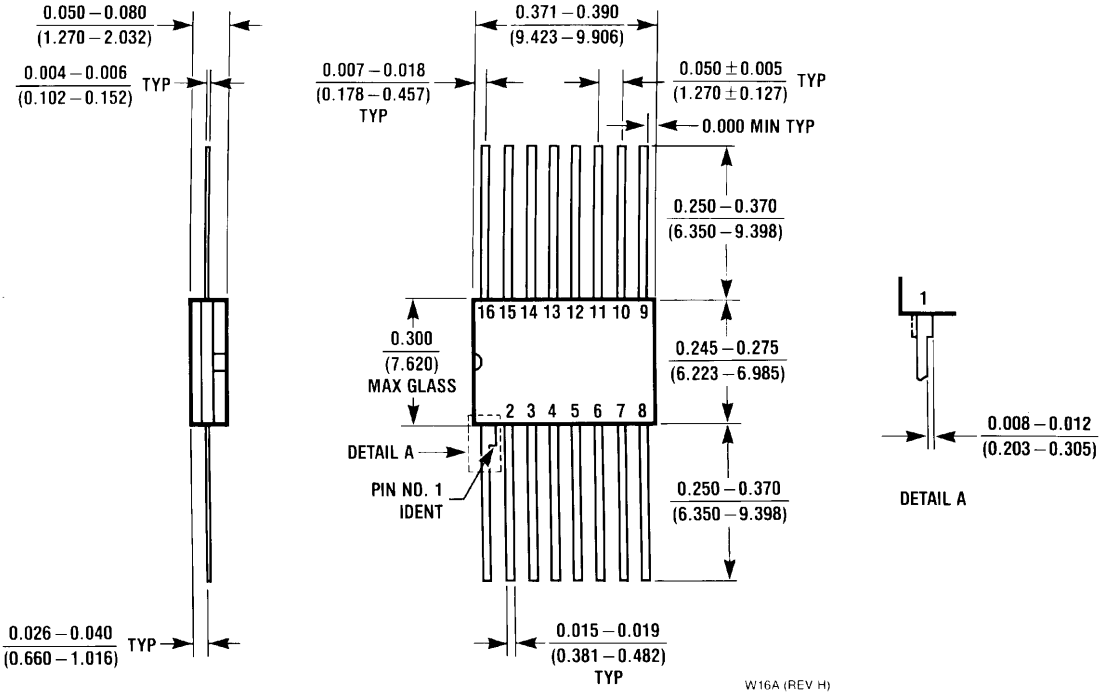
Physical Dimensions inches (millimeters) unless otherwise noted



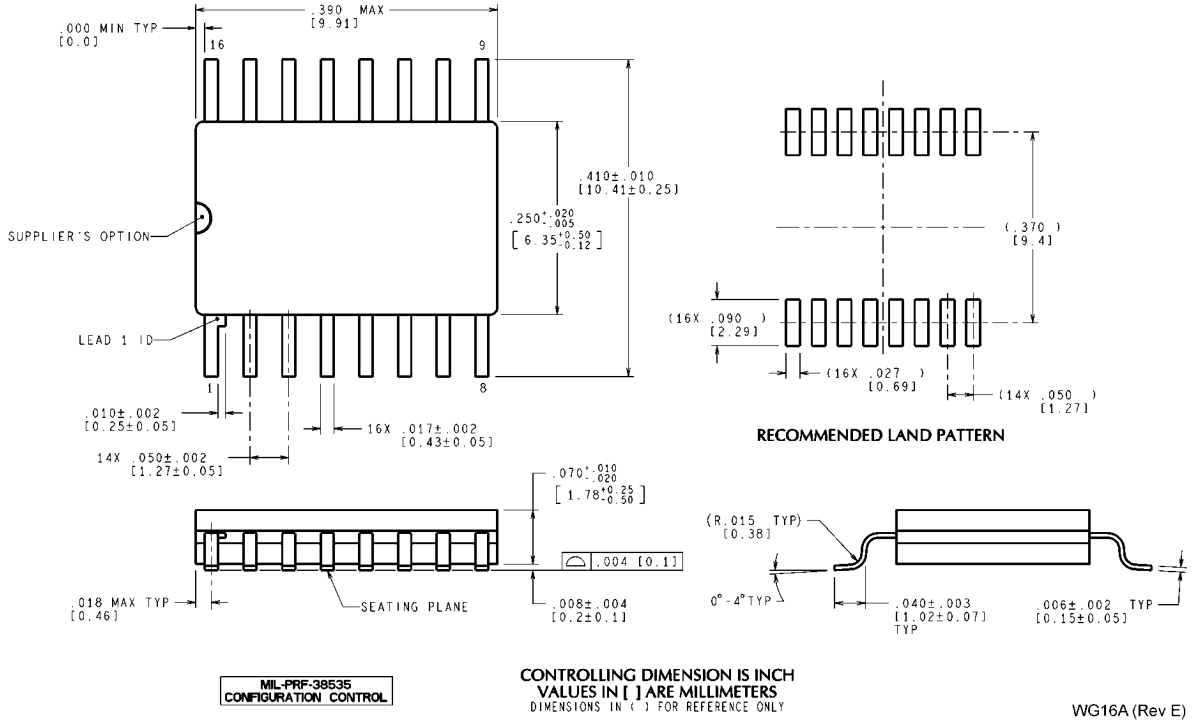
20-Lead Ceramic Leadless Chip Carrier (E)
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



16-Lead Ceramic FlatPak (W)
NS Package Number W16A



16-Lead Ceramic FlatPak (W)
NS Package Number WG16A

Notes

Notes

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