DESCRIPTION

The PT4501 is a highly integrated wideband FSK multi-channel half-duplex transceiver operating in sub-1 GHz license-free ISM bands. The PT4501 is supplied in a small 4 mm x 4 mm QFN-24 package, offers low power consumption, and is specified to operate in the consumer –40°C to +85°C temperature range. The receive part utilizes a fully integrated low-IF architecture. Direct PLL modulation with the fractional-N synthesizer is used for FSK transmission.

The device supports data rates up to 50 Kb/s in Manchester, bi-phase and other coding formats in transparent mode and provides a typical output power of +10 dBm into a 50 Ω load at 433.92 MHz, and +9 dBm at 915 MHz and achieves typical sensitivities of –113 dBm at 433.92 MHz and –110 dBm at 915 MHz for FSK data.

The PT4501 is suitable for wireless applications in unlicensed (ISM) bands and requires few external components due to its high level of integration.

APPLICATIONS

- Remote Control / Remote Sensing
- Remote Metering
- 2-Way Remote Keyless Entry
- Home Automation
- Local Telemetry Systems
- Wireless Modem

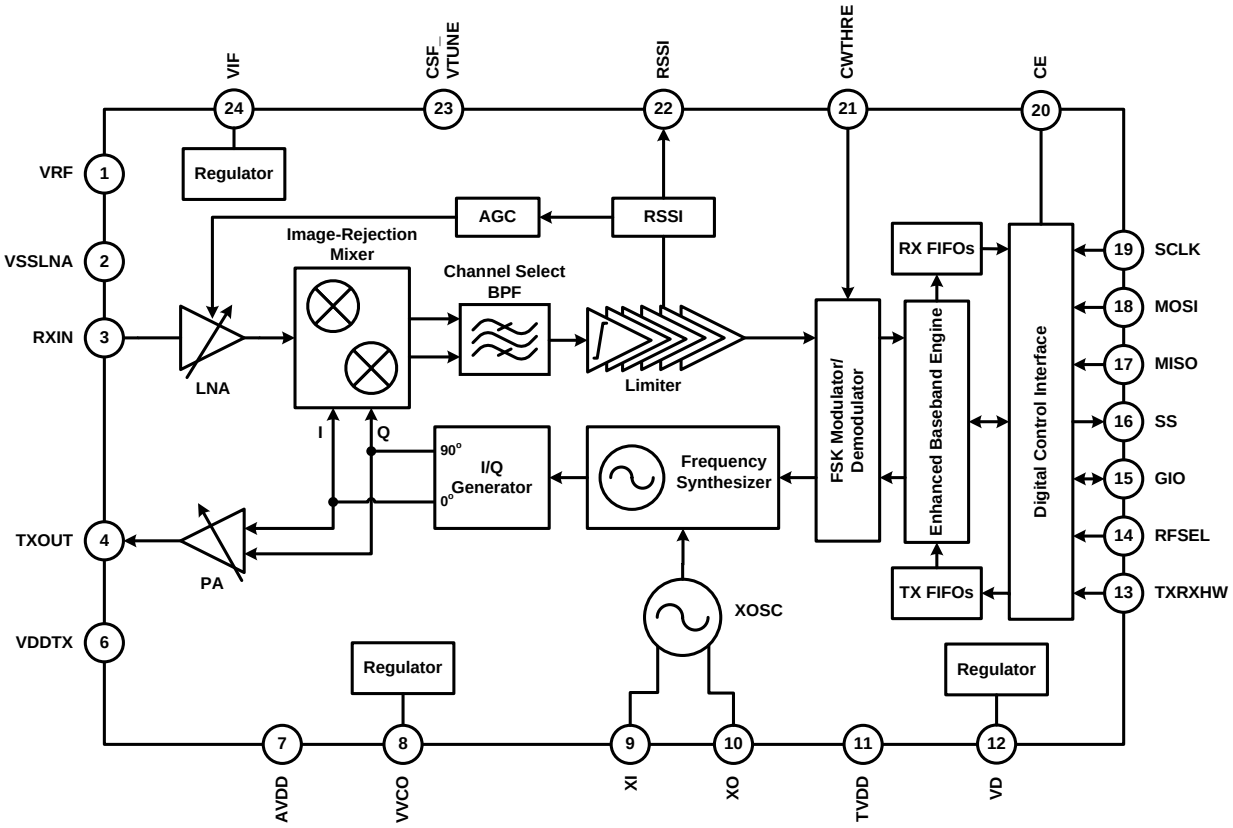
FEATURES

- Carrier frequency range: 300 MHz to 960 MHz
- Supply voltage range: 1.9 V to 3.6 V
- Low current consumption: frequency band: 14.5 mA for receive-mode and 30 mA for transmit-mode (+9 dBm at 915 MHz and +10 dBm at 433.92 MHz)
- Programmable RF output power with 20 dB power control range
- Programmable channel-select filter bandwidth of 200 KHz / 300 KHz / 400 KHz
- Excellent FSK sensitivity: –113 dBm (300 KHz channel bandwidth and 0.1% BER) at 433.92 MHz and –110 dBm 915 MHz
- > 25 dB image-rejection
- Few external components
- 50 dB RSSI range
- Power down function (< 1 µA current consumption in power-down mode)
- 4-wire SPI interface
- 2 separate TX and RX FIFOs (32 bytes each)
- QFN-24 package (4 mm × 4 mm)

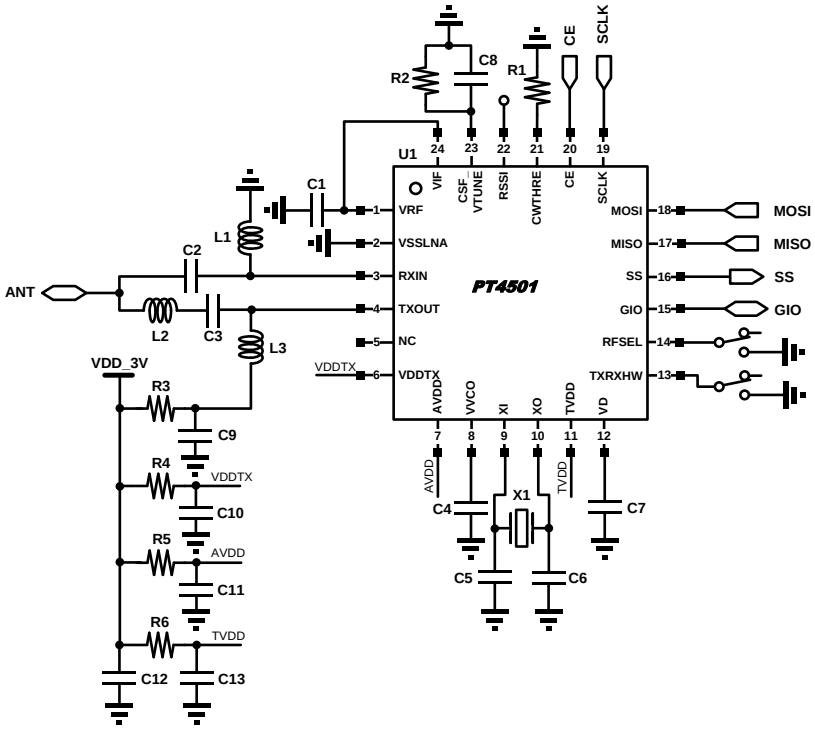
BENEFITS

- Low system cost due to high system integration level
- Extended battery life because of the low power consumption and the minimum supply voltage down to 1.9 V
- Merged RF input/output matching to save the external T/R switch
- Single-ended RF interface with high isolation of PLL/VCO from PA and the power supply allows for easy incorporation of dipole or loop antenna

BLOCK DIAGRAM



APPLICATION CIRCUIT



BILL OF MATERIALS

Part	Value					Unit
	315 MHz	434 MHz	470 MHz	868 MHz	915 MHz	
C1/C4/C7/C10/C13	10n	10n	10n	10n	10n	F
C2	2.7p	1.5p	1.5p	1.2p	1.5p	F
C3	220p	220p	220p	680p	680p	F
C5/C6	33p/33p	33p/33p	33p/33p	33p/33p	33p/33p	F
C8	680p	680p	680p	680p	680p	F
C9	10μ	10μ	10μ	10μ	10μ	F
C11/C12	NC	NC	NC	NC	NC	F
L1	47n	39n	33n	10n	8.2n	H
L2	6.8n	6.8n	6.8n	5.6n	5.6n	H
L3	18n	22n	22n	33n	39n	H
R1	68K	68K	68K	68K	68K	Ω
R2	150K	150K	150K	150K	150K	Ω
R3	0	0	0	0	0	Ω
R4/R5/R6	10	10	10	10	10	Ω
X1 (crystal)	20					MHz
U1	PT4501 IC					-

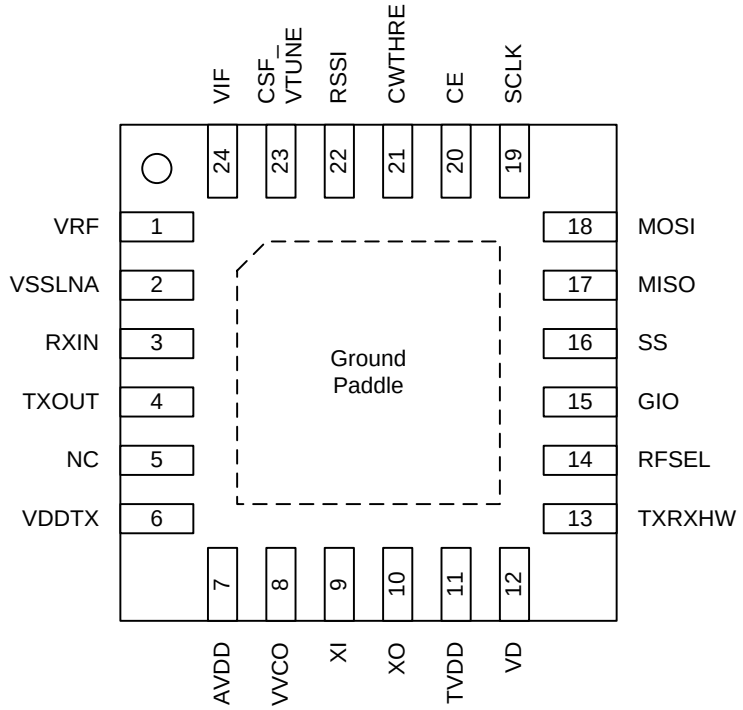
Notes:

1. L1/L2/L3 and C2/C3 are the components for input matching network. They may need to be adjusted for different PCB layout and antenna requirements.
2. R1 is used for adjusting the threshold voltage of carrier sense window.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4501	24 Pins, QFN	PT4501

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	VRF	P	Regulated 1.8V voltage for RF domain of receive chain
2	VSSLNA	G	Ground for low noise amplifier (LNA)
3	RXIN	I	Receiver RF input, connected to antenna through matching circuit
4	TXOUT	O	Transmitter RF output, connected to antenna through matching circuit
5	NC	—	No connection
6	VDDTX	P	External supply voltage for transmit and LO chains, 3 V input
7	AVDD	P	External supply voltage for analog domain, 3 V input
8	VVCO	P	Regulated 1.8V supply voltage for VCO
9	XI	I	Crystal oscillator input
10	XO	O	Crystal oscillator output
11	TVDD	P	External supply voltage for digital domain, 3 V input
12	VD	P	Regulated 1.8V supply voltage for digital domain
13	TXRXHW	I	TX/RX hardware control pin
14	RFSEL	I	RF frequency band (433.92/915 MHz) select pin
15	GIO	I/O	General purpose input/output, 3 V logic
16	SS	I	4-wire SPI interface low active slave select, 3 V logic
17	MISO	O	4-wire SPI interface serial data output, 3 V logic
18	MOSI	I	4-wire SPI interface serial data input, 3 V logic
19	SCLK	I	4-wire SPI interface serial clock, 3 V logic
20	CE	I	Chip-enable control pin, 3 V logic (CE = H = chip enable; CE = L = chip disable)
21	CWTHRE	I/O	Threshold voltage for carrier sense window
22	RSSI	O	Received signal strength indicator voltage
23	CSF_VTUNE	I/O	Tuning voltage for channel select filter
24	VIF	P	Regulated 1.8V voltage for analog domain of receive chain

IMPORTANT NOTICE

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