

Document Title

128K x 32 Pipelined SyncBurst SRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	September 17,2001	

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128K x 32, 128K x 36 SYNCHRONOUS PIPELINED STATIC RAM

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- 100-Pin TQFP (JEDEC LQFP) and 119-pin PBGA package
- Single +3.3V, +10%, -5% power supply
- Power-down snooze mode

DESCRIPTION

The *ICSI* IC61SP12832, IC61SP12836 are high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, secondary cache for the Pentium™, 680X0™, and PowerPC™ microprocessors. It is organized as 131,072 words by 32 bits, fabricated with *ICSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. BW1 controls DQa, BW2 controls DQb, BW3 controls DQc, BW4 controls DQd, conditioned by BWE being LOW. A LOW on GW input would cause all bytes to be written.

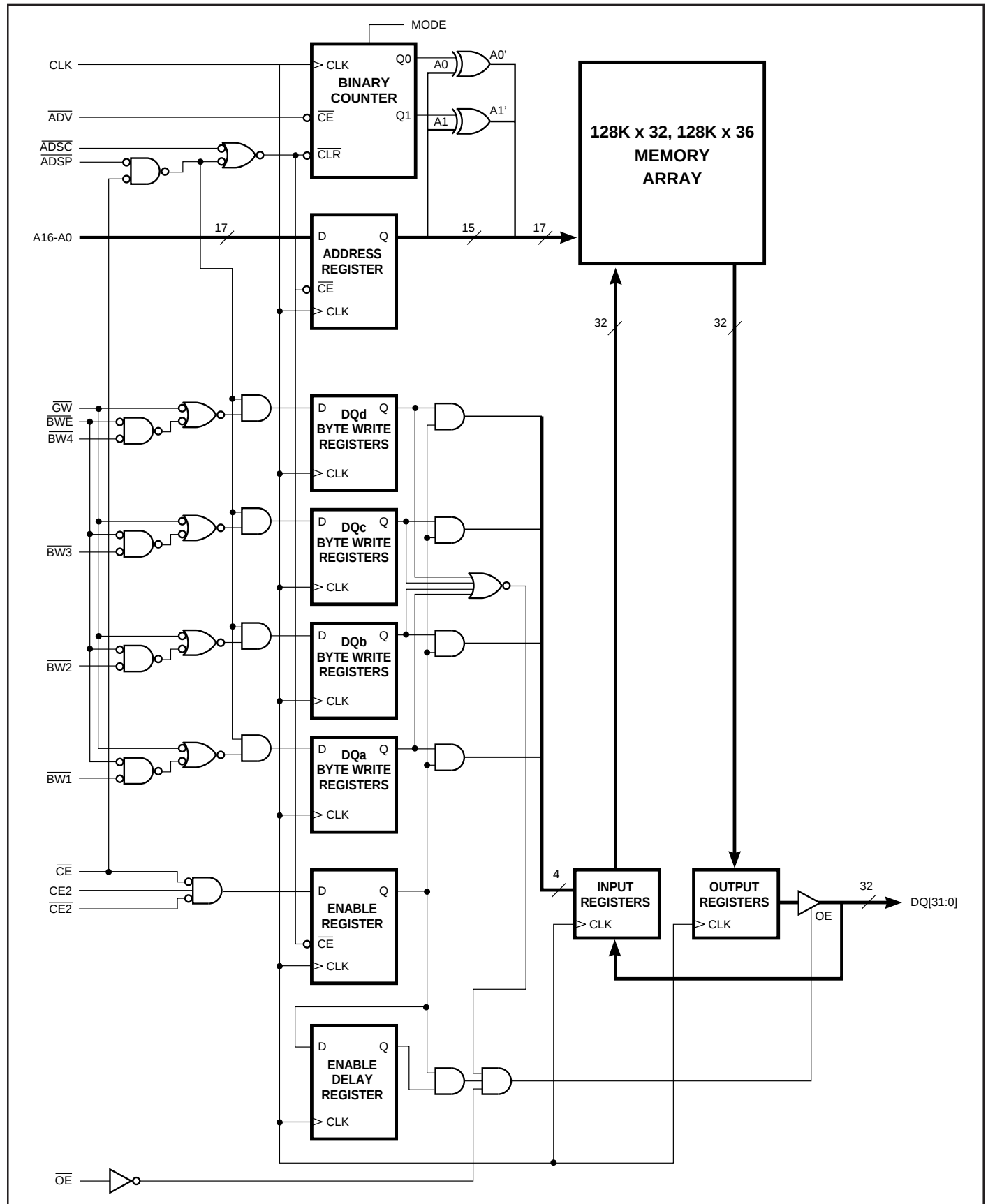
Bursts can be initiated with either ADSP (Address Status Processor) or ADSC (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IC61SP12832, IC61SP12836 and controlled by the ADV (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

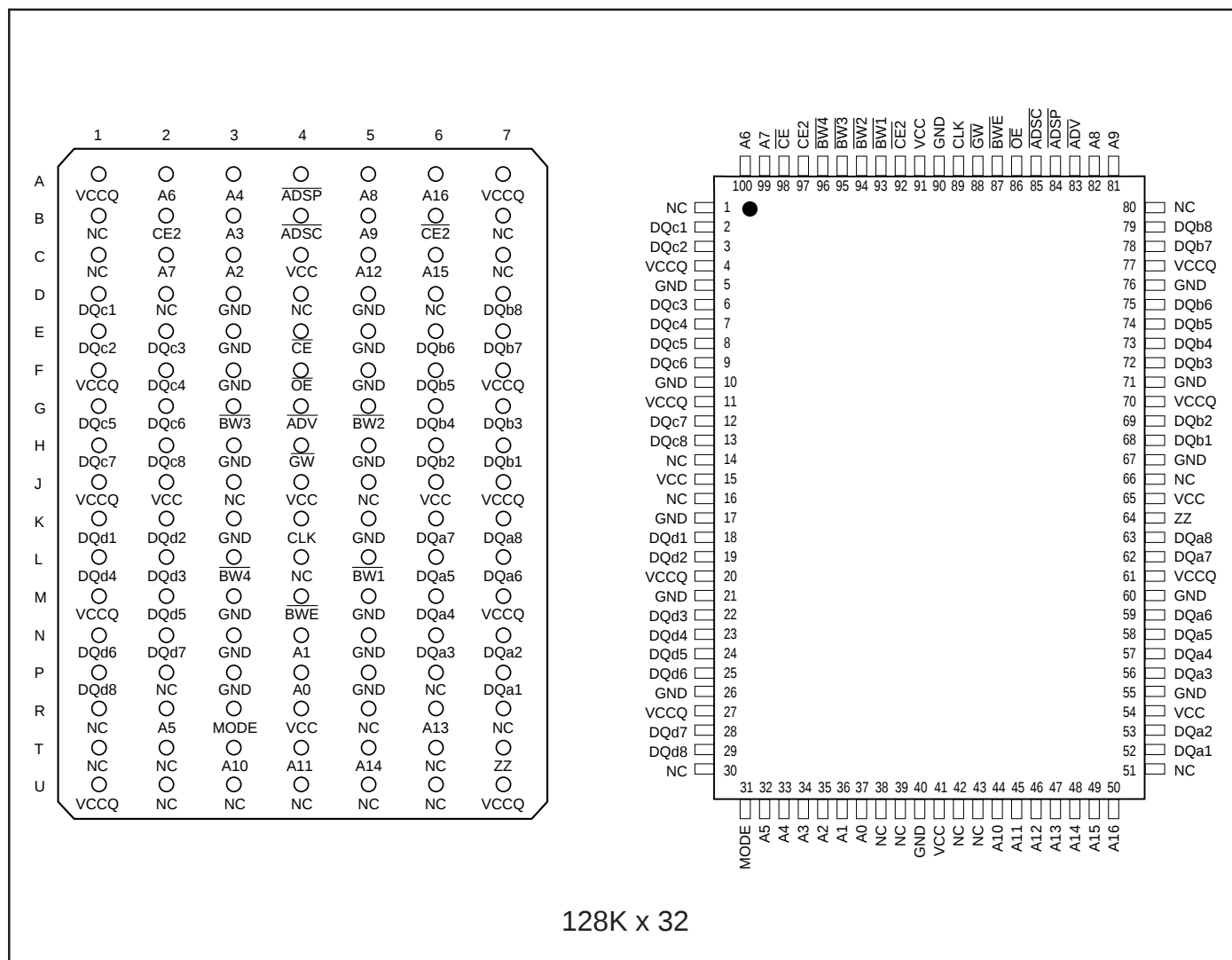
Symbol	Parameter	-166	-150	-133	-117	-5	Units
tkQ	Clock Access Time	3.5	3.8	4	4	5	ns
tkC	Cycle Time	6	6.7	7.5	8.5	10	ns
	Frequency	166	150	133	117	100	MHz

BLOCK DIAGRAM



PIN CONFIGURATION

119-pin PBGA (Top View) and 100-Pin LQFP



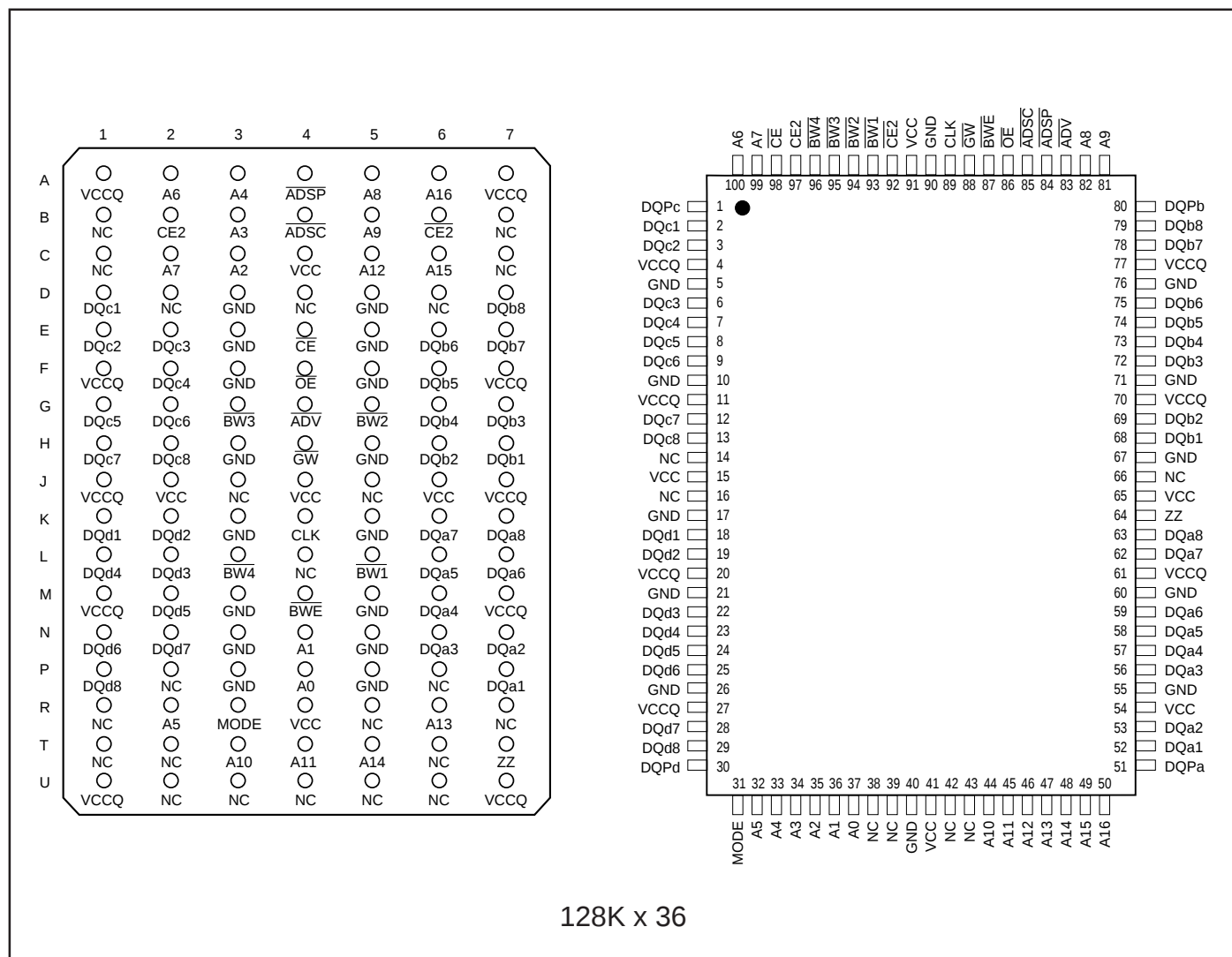
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BW1-BW4	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable

GW	Synchronous Global Write Enable
CE, CE2, CE2	Synchronous Chip Enable
OE	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable
GNDq	Isolated Output Buffer Ground

PIN CONFIGURATION

119-pin PBGA (Top View) and 100-Pin LQFP



PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.	GW	Synchronous Global Write Enable
A2-A16	Synchronous Address Inputs	CE, CE2, CE2	Synchronous Chip Enable
CLK	Synchronous Clock	OE	Output Enable
ADSP	Synchronous Processor Address Status	DQa-DQd	Synchronous Data Input/Output
ADSC	Synchronous Controller Address Status	MODE	Burst Sequence Mode Selection
ADV	Synchronous Burst Address Advance	Vcc	+3.3V Power Supply
BW1-BW4	Synchronous Byte Write Enable	GND	Ground
BWE	Synchronous Byte Write Enable	Vccq	Isolated Output Buffer Supply: +3.3V
		ZZ	Snooze Enable
		GNDq	Isolated Output Buffer Ground
		DQPa-DQPd	Parity Data I/O

TRUTH TABLE

Operation	Address Used	$\overline{\text{CE}}$	CE2	$\overline{\text{CE2}}$	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	0	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	H	0	X	Read	X	High-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	High-Z
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	High-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	High-Z
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	High-Z

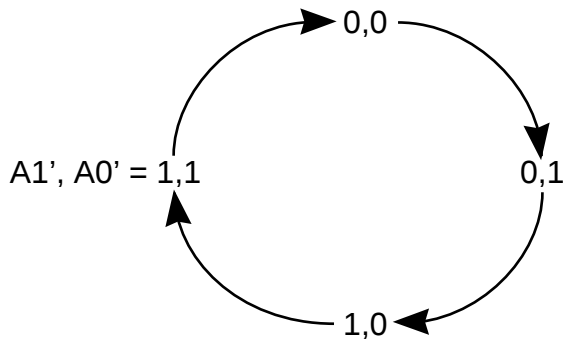
PARTIAL TRUTH TABLE

Function	$\overline{\text{GW}}$	$\overline{\text{BWE}}$	BW1	BW2	BW3	BW4
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	−40 to +85	°C
T _{STG}	Storage Temperature	−55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	−0.5 to V _{CCQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	−0.5 to V _{CC} + 0.5	V
V _{CC}	Voltage on V _{CC} Supply Relative to GND	−0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V, +10%, -5%
Industrial	-40°C to +85°C	3.3V, +10%, -5%

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CCQ} ⁽²⁾	Com. Ind.	-2 5	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_{IH}$	Com. Ind.	-2 5	μA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-166 Typ.	-166 Max.	-150 Typ.	-150 Max.	-133 Typ.	-133 Max.	-117 Typ.	-117 Max.	-5 Typ.	-5 Max.	Unit
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} $\overline{OE} = V_{IH}$, V _{CC} = Max. Cycle Time ≥ t _{kc} min.	Com.	200	230	190	220	180	210	175	205	170	200	mA
			Ind.	—	—	200	230	190	220	185	215	180	210	mA
I _{SB}	Standby Current	Device Deselected, V _{CC} = Max., All Inputs = V _{IH} or V _{IL} CLK Cycle Time ≥ t _{kc} min.	Com.	45	70	45	70	45	70	45	65	45	65	mA
			Ind.	—	—	50	80	50	80	50	75	50	75	mA
I _{ZZ}	Power-down Mode Current	ZZ = V _{CCQ} Clock Running All Inputs ≤ GND + 0.2V or ≥ V _{CC} - 0.2V	Com.	—	5	—	5	—	5	—	5	—	5	mA
			Ind.	—	15	—	15	—	15	—	15	—	15	mA

Notes:

1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{CCQ}.
2. The MODE pin should be tied to V_{CC} or GND. It exhibits ±10 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{CC} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

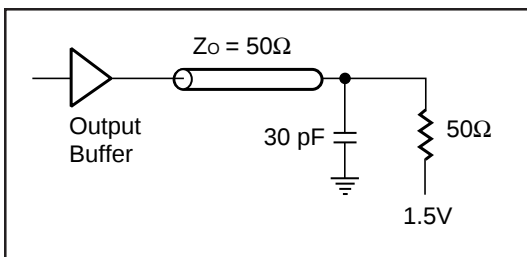


Figure 1

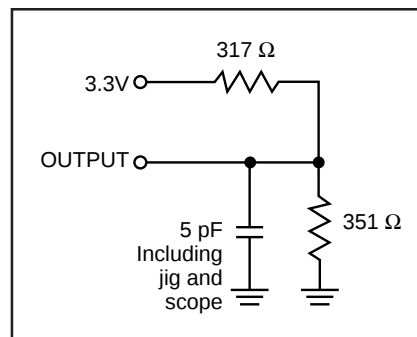


Figure 2

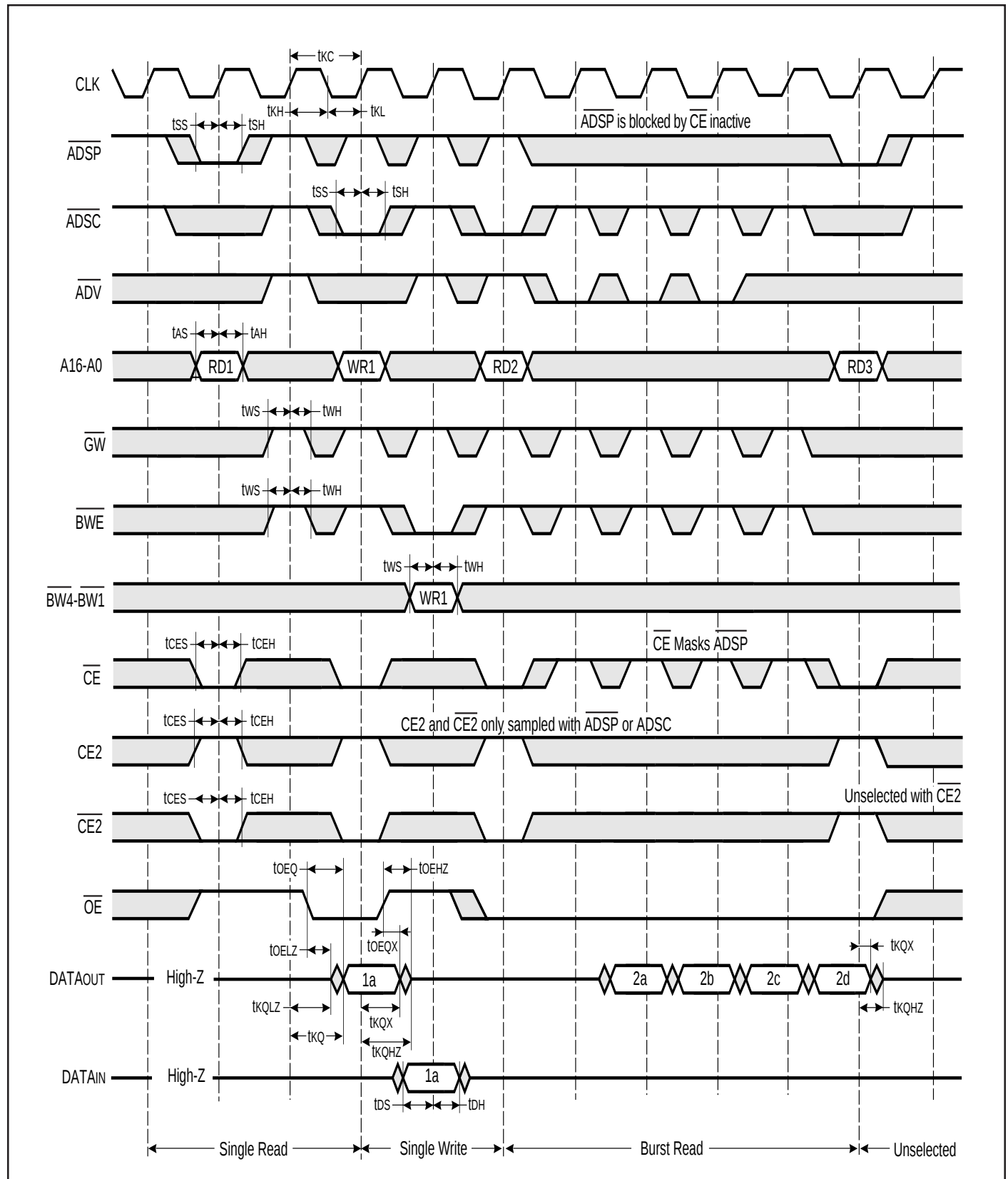
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166		-150		-133		-117		-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Clock Frequency	—	166	—	150	—	133	—	117	—	100	MHz
t _{KC}	Cycle Time	6	—	6.7	—	7.5	—	8.5	—	10	—	ns
t _{KH}	Clock High Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t _{KL}	Clock Low Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t _{KQ}	Clock Access Time	—	3.5	—	3.8	—	4	—	4	—	5	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	2.5	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	1.5	6	1.5	6.7	1.5	7.5	1.5	8.5	1.5	10	ns
t _{OEQ}	Output Enable to Output Valid	—	3.5	—	3.5	—	3.8	—	4	—	5	ns
t _{OEQX} ⁽¹⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	0	—	ns
t _{OEZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t _{OEZH} ^(1,2)	Output Disable to Output High-Z	2	3.5	2	3.5	2	3.8	2	4	2	5	ns
t _{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns

Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166		-150		-133		-117		-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CC}	Cycle Time	6	—	6.7	—	7.5	—	8.5	—	10	—	ns
t _{KH}	Clock High Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t _{KL}	Clock Low Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t _{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{DS}	Data In Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{DH}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns

Timing diagram for ADSP, ADSC, ADV, A16-A0, GW, BWE, BW4-BW1, CE, CE2, CE2, OE, DATAOUT, and DATAIN signals. The diagram illustrates the sequence of operations: Single Write, Burst Write, Write, and Unselected. Key timing parameters are labeled: t_{SS} , t_{SH} , t_{KH} , t_{KL} , t_{AVS} , t_{AVH} , t_{AS} , t_{AH} , t_{WS} , t_{WH} , t_{CES} , t_{CEH} , t_{DS} , and t_{DH} . Annotations include: "ADSP is blocked by CE inactive", "ADV must be inactive for ADSP Write", "CE Masks ADSP", "CE2 and CE2 only sampled with ADSP or ADSC", "Unselected with CE2", and "BW4-BW1 only are applied to first cycle of WR2".

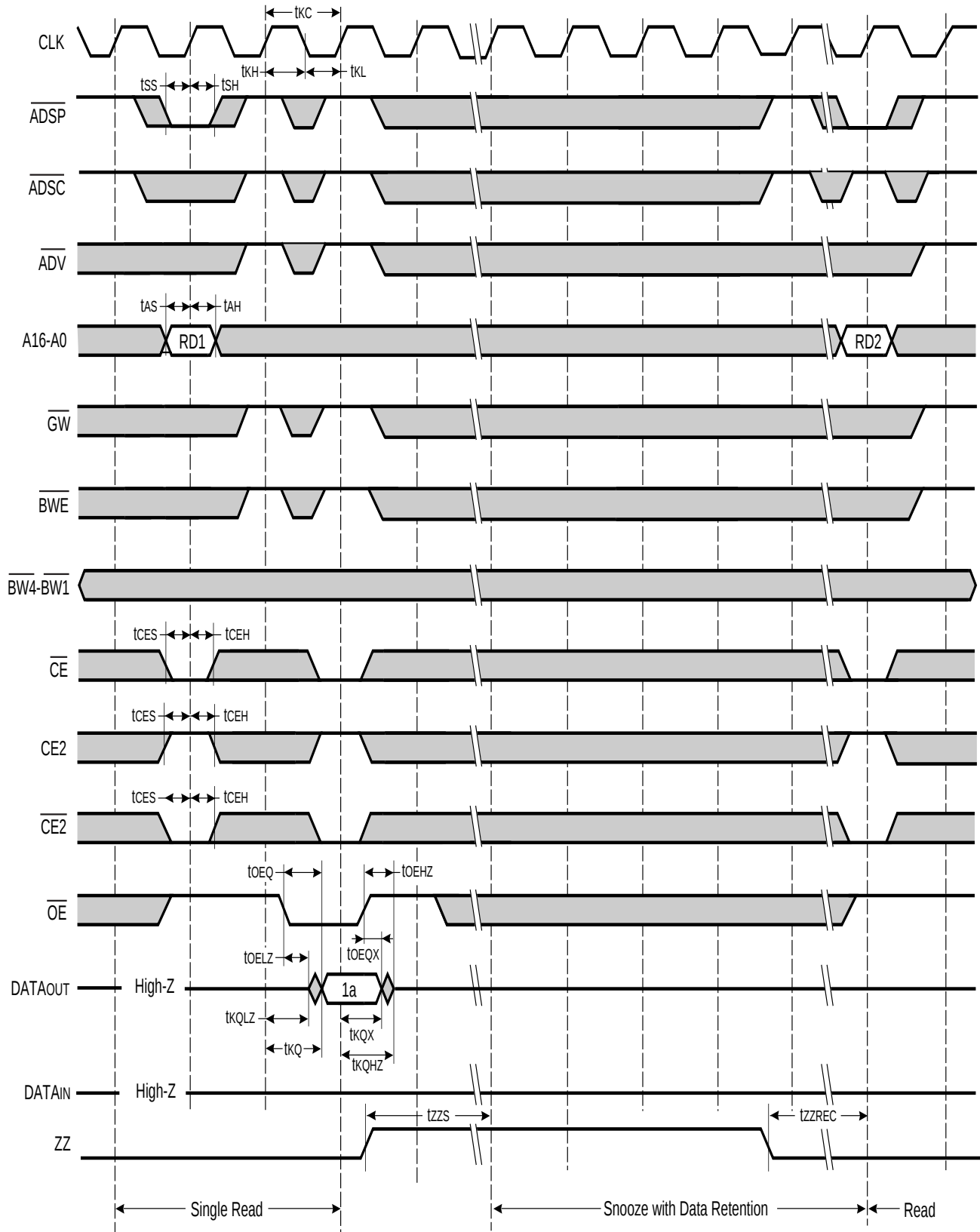
SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166		-150		-133		-117		-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	6	—	6.7	—	7.5	—	8.5	—	10	—	ns
t _{KH}	Clock High Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t _{KL}	Clock Low Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t _{KQ}	Clock Access Time	—	3.5	—	3.8	—	4	—	4	—	5	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	2	—	2.5	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	1.5	3.6	1.5	6.7	1.5	7.5	1.5	8.5	1.5	10	ns
t _{OEQ}	Output Enable to Output Valid	—	3.5	—	3.5	—	3.9	—	4	—	5	ns
t _{OEQX} ⁽¹⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	0	—	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t _{OEHZ} ^(1,2)	Output Disable to Output High-Z	2	3.5	2	3.5	2	3.8	2	4	2	5	ns
t _{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{ZZS}	ZZ Standby	2	—	2	—	2	—	2	—	2	—	cyc
t _{ZZREC}	ZZ Recovery	2	—	2	—	2	—	2	—	2	—	cyc

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166 MHz	IC61SP12832-166TQ	14x20x1.4mm LQFP
	IC61SP12832-166B	14*22mm PBGA
150 MHz	IC61SP12832-150TQ	14*20*1.4mm LQFP
	IC61SP12832-150B	14*22mm PBGA
133 MHz	IC61SP12832-133TQ	14*20*1.4mm LQFP
	IC61SP12832-133B	14*22mm PBGA
117 MHz	IC61SP12832-117TQ	14*20*1.4mm LQFP
	IC61SP12832-117B	14*22mm PBGA
100 MHz	IC61SP12832-5TQ	14*20*1.4mm LQFP
	IC61SP12832-5B	14*22mm PBGA

Speed	Order Part Number	Package
166 MHz	IC61SP12836-166TQ	14x20x1.4mm LQFP
	IC61SP12836-166B	14*22mm PBGA
150 MHz	IC61SP12836-150TQ	14*20*1.4mm LQFP
	IC61SP12836-150B	14*22mm PBGA
133 MHz	IC61SP12836-133TQ	14*20*1.4mm LQFP
	IC61SP12836-133B	14*22mm PBGA
117 MHz	IC61SP12836-117TQ	14*20*1.4mm LQFP
	IC61SP12836-117B	14*22mm PBGA
100 MHz	IC61SP12836-5TQ	14*20*1.4mm LQFP
	IC61SP12836-5B	14*22mm PBGA



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