

TRIACs, 40A Snubberless

FEATURES

- High current triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated TO-3P package
- High commutation capability
- 41T series are **UL** certified (File ref: E320098)
- Packages are RoHS compliant

APPLICATIONS

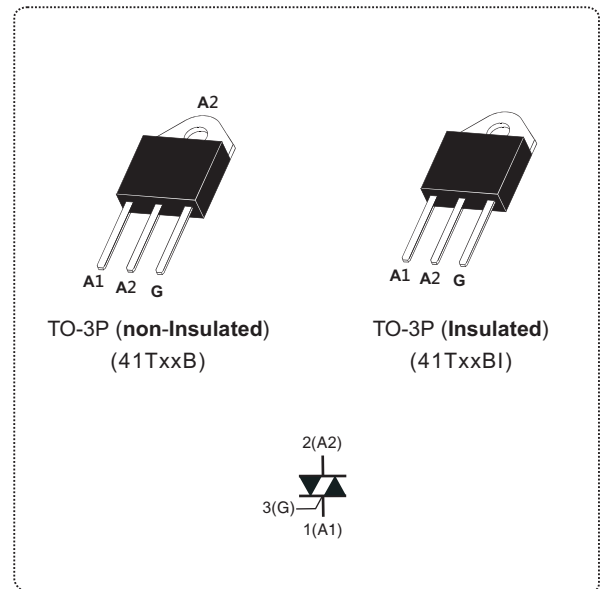
The snubberless concept offer suppression of RC network and it is suitable for applications such as on/off function in static relays, heating regulation, induction motor starting circuits, phase control operation in light dimmers, motor speed controllers, and similar.

Due to their clip assembly technique, they provide a superior performance in surge current handling capabilities.

By using an internal ceramic pad, the 41T series provides voltage insulated tab (rated at 2500VRMS) complying with UL standards.

MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	40	A
V_{DRM}/V_{RRM}	600 to 1600	V
$I_{GT(Q1)}$	35 to 50	mA



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$	TO-3P	$T_c = 95^\circ\text{C}$	40	A
		TO-3P insulated	$T_c = 80^\circ\text{C}$		
Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	I_{TSM}	F = 50 Hz	t = 20 ms	400	A
		F = 60 Hz	t = 16.7 ms	420	
I^2t Value for fusing	I^2t	$t_p = 10$ ms		800	A^2s
Critical rate of rise of on-state current $I_G = 2xI_{GT}$, $t_r \leq 100\text{ns}$	dI/dt	F = 100 Hz	$T_j = 125^\circ\text{C}$	50	A/ μs
Peak gate current	I_{GM}	$T_p = 20 \mu\text{s}$	$T_j = 125^\circ\text{C}$	4	A
Peak gate power dissipation ($t_p = 20\mu\text{s}$)	P_{GM}	$T_j = 125^\circ\text{C}$		10	W
Average gate power dissipation	$P_{G(AV)}$	$T_j = 125^\circ\text{C}$		1	
Storage temperature range	T_{stg}			- 40 to + 150	$^\circ\text{C}$
Operating junction temperature range	T_j			- 40 to + 125	

© ELECTRICAL CHARACTERISTICS (T_j = 25 °C unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)					
SYMBOL	TEST CONDITIONS	QUADRANT		41Txxxx	Unit
				BW	
I _{GT} ⁽¹⁾	V _D = 12 V, R _L = 30Ω	I - II - III	MAX.	50	mA
V _{GT}		I - II - III		1.3	V
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ T _j = 125°C	I - II - III	MIN.	0.2	V
I _H ⁽²⁾	I _T = 500 mA		MAX.	60	mA
I _L	I _G = 1.2 I _{GT}	I - III	MAX.	80	mA
		II		100	
dV/dt ⁽²⁾	V _D = 67% V _{DRM} , gate open, T _j = 125°C		MIN.	1000	V/μs
(dI/dt) _c ⁽²⁾	Without snubber, T _j = 125°C			20	A/ms

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
V _{TM} ⁽²⁾	I _{TM} = 60 A, t _p = 380 μs	T _j = 25°C	MAX.	1.55	V
V _{T0} ⁽²⁾	Threshold voltage	T _j = 125°C	MAX.	0.85	V
R _d ⁽²⁾	Dynamic resistance	T _j = 125°C	MAX.	10	mΩ
I _{DRM} I _{RRM}	V _D = V _{DRM} V _R = V _{RRM}	T _j = 25°C	MAX.	10	μA
		T _j = 125°C		5	mA

Note 1: Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE					
SYMBOL				VALUE	UNIT
R _{th(j-c)}	Junction to case (AC)	TO-3P		0.6	°C/W
		TO-3P Insulated		0.9	
R _{th(j-a)}	Junction to ambient	TO-3P, TO-3P Insulated		50	

S = Copper surface under tab.

PRODUCT SELECTOR								
PART NUMBER	VOLTAGE (xx)					SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V	1200 V	1600 V			
41TxxB-BW/41TxxBI-BW	V	V	V	V	V	50 mA	Snubberless	TO-3P

BI: Insulated TO-3P package

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
41TxxB-yy	41TxxB-yy	TO-3P	4.3g	30	Tube
41TxxBI-yy	41TxxBI-yy	TO-3P insulated	4.8g	30	Tube

Note: xx = voltage, yy = sensitivity

ORDERING INFORMATION SCHEME	
	41 T 06 B - BW
Current	41 = 40A
Triac series	T
Voltage	06 = 600V 08 = 800V 10 = 1000V 12 = 1200V 16 = 1600V
Package type	B = TO-3P (non-insulated) BI = TO-3P (insulated)
I_{GT} Sensitivity	BW = 50mA Snubberless

Fig.1 Maximum power dissipation versus on-state rms current (full cycle)

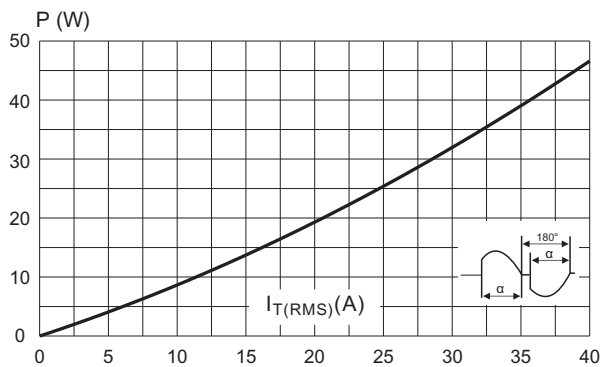


Fig.2 On-state rms current versus case temperature (full cycle)

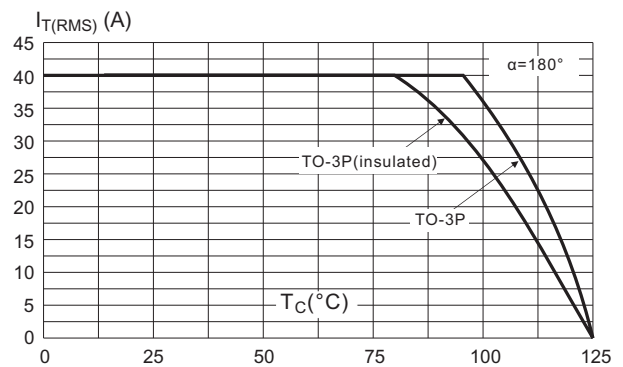


Fig.3 Relative variation of thermal impedance versus pulse duration.

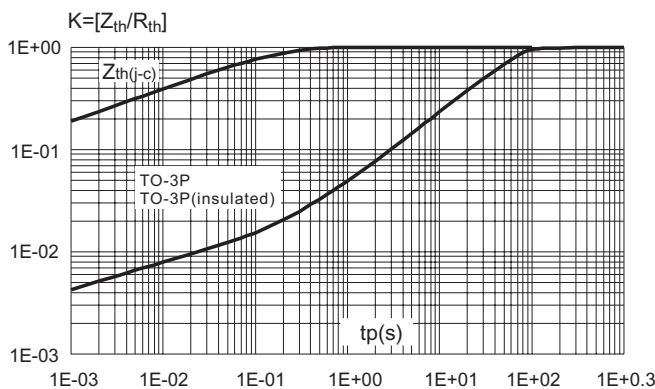


Fig.4 On-state characteristics (maximum values).

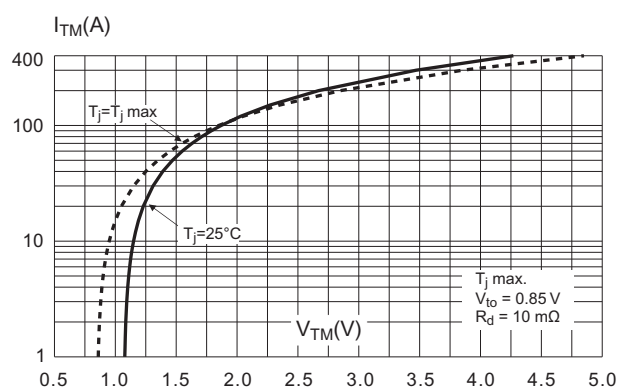


Fig.5 Surge peak on-state current versus number of cycles.

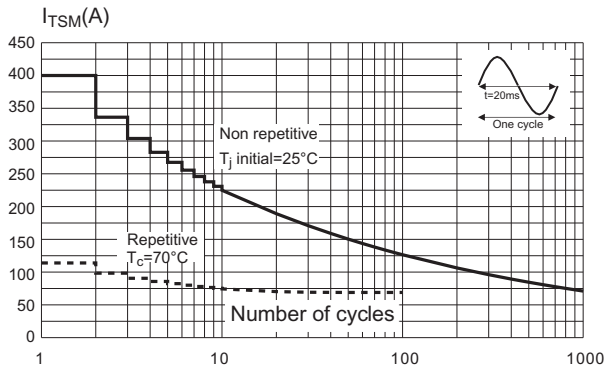


Fig.6 Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding value of I^2t .

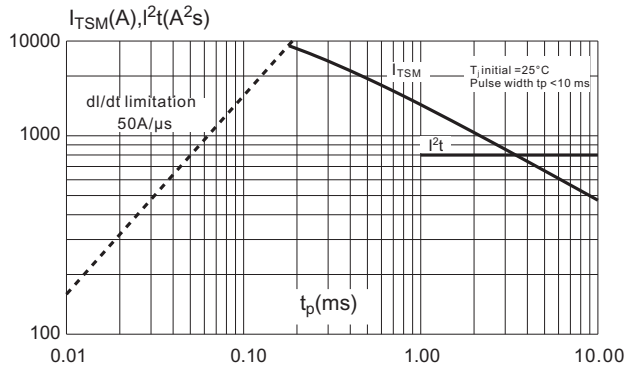


Fig.7 Relative variation of gate trigger, holding and latching current versus junction temperature.

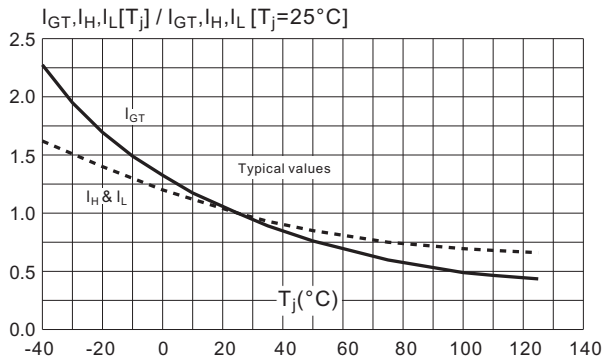


Fig.8 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values).

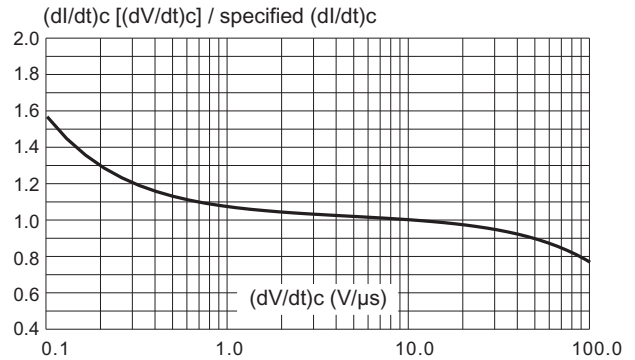
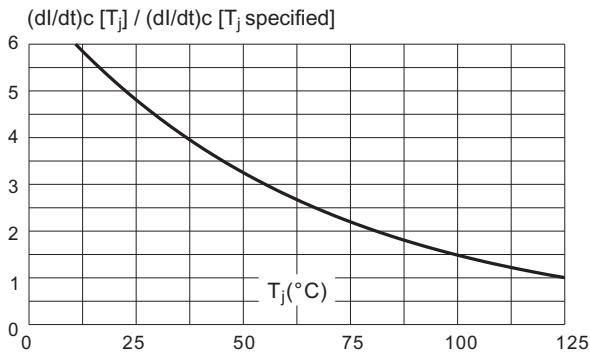


Fig.9 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$.



Case Style

