

ML9040A-Axx/-Bxx

DOT MATRIX LCD CONTROLLER WITH 16-DOT COMMON DRIVER AND 40-DOT SEGMENT DRIVER

GENERAL DESCRIPTION

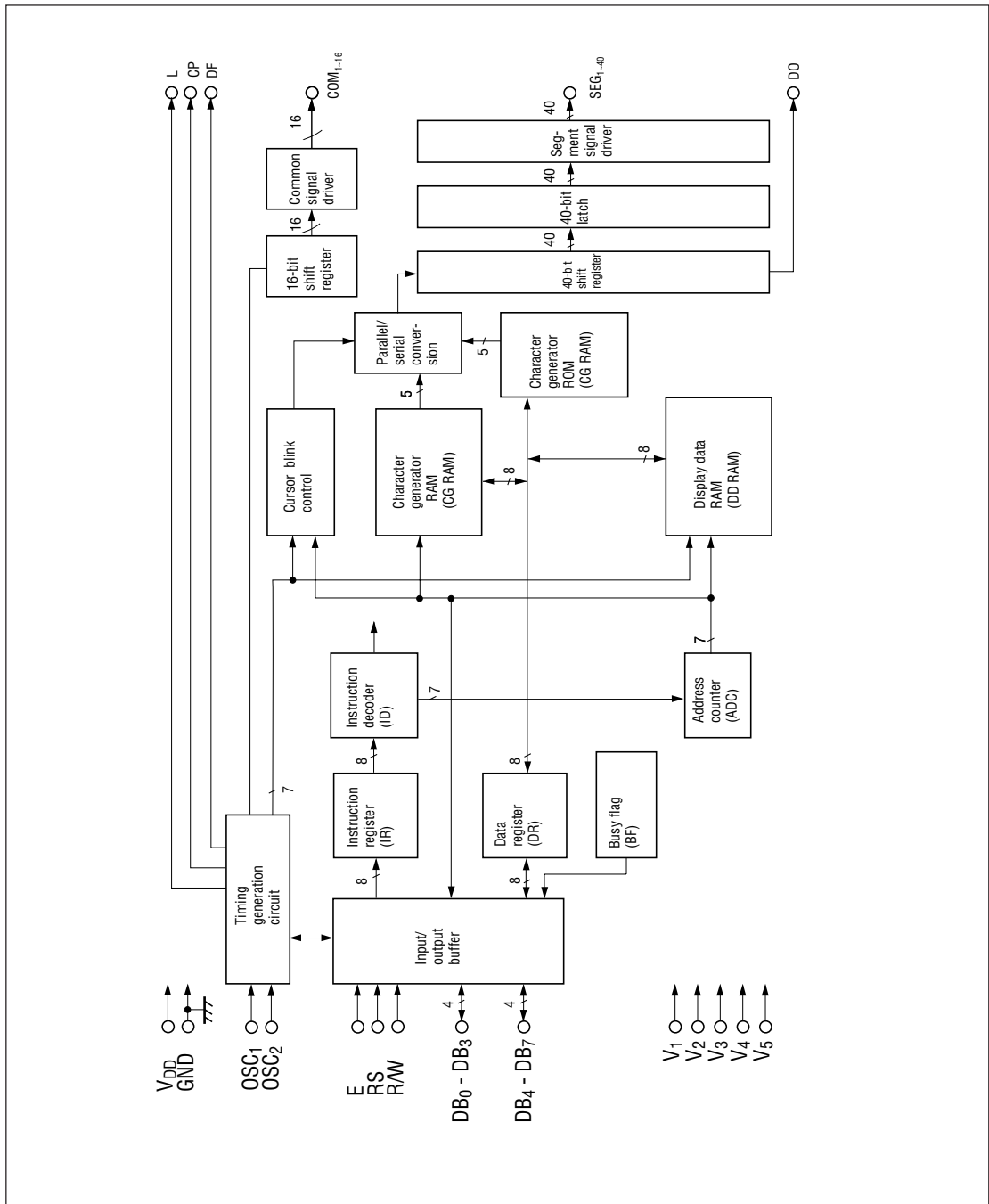
The ML9040A-Axx/-Bxx is a dot matrix LCD controller which is fabricated in low power CMOS silicon gate technology. Character display on the dot matrix character type LCD can be controlled in combination with a 4-bit or 8-bit microcontroller. This LSI consists of 16-dot COMMON driver, 40-dot SEGMENT driver, display data RAM, character generator RAM, character generator ROM and control circuit.

The ML9040A-Axx/-Bxx has the character generator ROM that can be programmed by custom mask. The ML9040A-A01/-B01 is a standard version having 160 characters with lowercase (5 x 7 dots), and 32 characters with uppercase (5 x 10 dots) in this ROM.

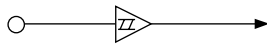
FEATURES

- Easy interface with an 8-bit or 4-bit microcontroller.
 - Dot matrix LCD controller/driver for lowercase (5 x 7 dots) or uppercase (5 x 10 dots).
 - Automatic power ON reset.
 - COMMON signal drivers (16) and SEGMENT signal drivers (40).
 - Can control up to 80 characters when used in combination with MSM5259.
 - Character generator ROM for 160 characters with lowercase (5 x 7 dots) and 32 characters with uppercase (5 x 10 dots).
 - Character patterns are programmable by character generator RAM. (Lowercase: 5 x 8 dots, 8 patterns, uppercase: 5 x 11 dots, 4 patterns).
 - Built-in oscillation circuit to connect with external resistor or ceramlock.
 - 1/8 duty (1 line; 5 x 7 dots + cursor), 1/11 duty (1 line; 5 x 10 dots + cursor), or 1/16 duty (2 lines; 5 x 7 dots + cursor), selectable.
 - Clear display even at 1/5 bias, 3.0V LCD driving voltage.
 - LCD driving waveform
 - ML9040A-Axx: A mode
 - ML9040A-Bxx: B mode
 - Package options:
 - 80-pin plastic QFP(QFP80-P-1420-0.80-BK)(Product name: ML9040A-Axx/-BxxGA)
 - Al pad chip (Product name: ML9040A-Axx/-BxxWA)
- xx indicates code number.
01 indicates standard code number.

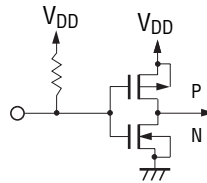
BLOCK DIAGRAM



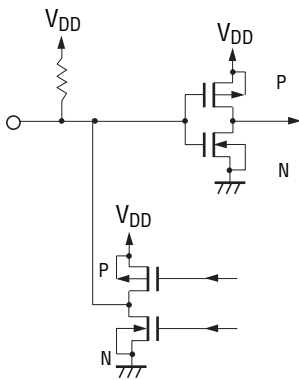
INPUT AND OUTPUT CONFIGURATION



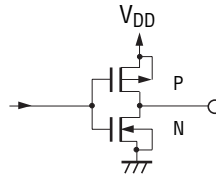
Applicable to pin E.



Applicable to pins R/W and RS.



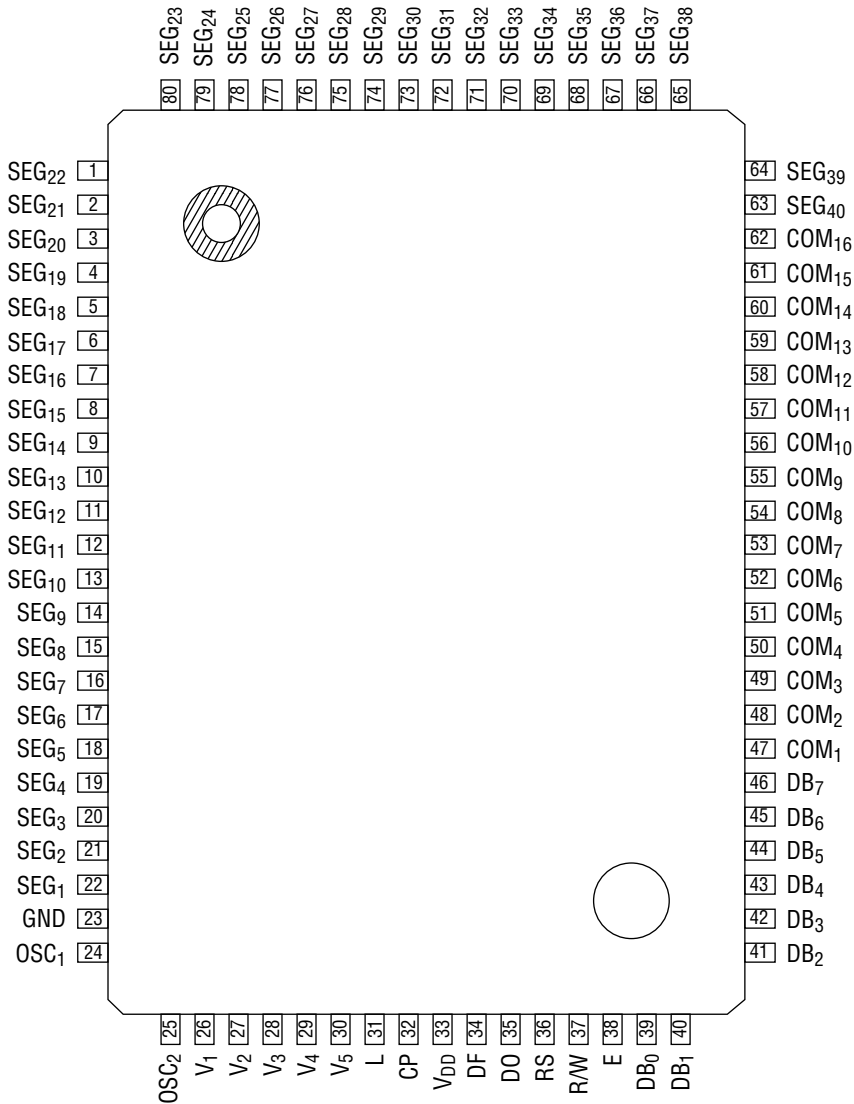
Applicable to pins DB₀ - DB₇.



Applicable to pins DO, CP, L, and DF.

PIN CONFIGURATION (TOP VIEW)

ML9040A-Axx/-Bxx GA



80-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Description
R/W	Read/write selection input pin. "H" : Read, and "L" : Write
RS	Register selection input pin. "H" : Data register, and "L" : Instruction register
E	Input pin for data input/output with CPU and for instruction register activation.
DB ₀ - DB ₇	Input/output pins for data send/receive with CPU
OSC ₁ , OSC ₂	Clock oscillating pins required for internal operation upon receipt of the LCD drive signal and CPU instruction.
COM ₁ - COM ₁₆	LCD COMMON signal output pins.
SEG ₁ - SEG ₄₀	LCD SEGMENT signal output pins.
DO	Output pin to be connected to MSM5259 to expand the number of characters to be displayed.
CP	Clock output pin used when DO pin data output shifts inside of MSM5259.
L	Clock output pin for the serially transferred data to be latched to MSM5259.
DF	The alternating current signal (Display Frequency) output pin.
V _{DD}	Power supply pin.
GND	Ground pin.
V ₁ , V ₂ , V ₃ , V ₄ , V ₅	Bias voltage input pins to drive the LCD.
TEST	This is the pin for testing the IC chip. Leave this pin open during normal use. *This pin is available only for AI pad chip.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable pin
Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to + 7.0	V	V_{DD} , GND
LCD Driving Voltage	V_1, V_2, V_3 V_4, V_5	$T_a = 25^\circ\text{C}$	$V_{DD} - 8.0$ to $V_{DD} + 0.3$	V	V_1, V_2, V_3 V_4, V_5
Input Voltage	V_I	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD} + 0.3$	V	R/W, RS, E, DB ₀ - DB ₇ OSC ₁
Power Dissipation	P_D	—	500	mW	—
Storage Temperature	T_{STG}	—	-55 to + 150	°C	—

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable pin
Supply Voltage	V_{DD}	—	4.5 to 5.5	V	V_{DD} , GND
Data Holding Voltage* ¹	V_{HOLD}	—	3.0 to 5.5	V	V_{DD} , GND
LCD Driving Voltage* ²	V_{LCD}	1/4 bias, $V_{DD} - V_5$ * ³	3.0 to 6.0	V	V_{DD} , V_5
		1/5 bias, $V_{DD} - V_5$ * ⁴	3.0 to 6.0	V	
Operating Temperature	T_{op}	—	-20 to + 75	°C	—

*1 Voltage to assure R_f oscillation and register data retention.

*2 Voltage between V_{DD} and V_5 .

*3 Voltages applicable to V_1 , V_2 , V_3 and V_4 are as follows.

$$V_1 = V_{DD} - 1/4 (V_{DD} - V_5)$$

$$V_2 = V_3 = V_{DD} - 1/2 (V_{DD} - V_5)$$

$$V_4 = V_{DD} - 3/4 (V_{DD} - V_5)$$

*4 $V_1 = V_{DD} - 1/5 (V_{DD} - V_5)$

$$V_2 = V_{DD} - 2/5 (V_{DD} - V_5)$$

$$V_3 = V_{DD} - 3/5 (V_{DD} - V_5)$$

$$V_4 = V_{DD} - 4/5 (V_{DD} - V_5)$$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5V, T_a = -20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin	
"H" Input Voltage	V _{IH1}	—	2.2	—	V _{DD}	V	RS, E, DB ₀ - DB ₇	
"L" Input Voltage	V _{IL1}	—	-0.3	—	0.6	V	DB ₀ - DB ₇ , RS, E, RW	
"H" Input Voltage	V _{IH2}	—	V _{DD} -1.0	—	V _{DD}	V	OSC ₁ , R/W	
"L" Input Voltage	V _{IL2}	—	-0.3	—	1.0	V	OSC ₁	
"H" Output Voltage	V _{OH1}	I _O = -0.205mA	2.4	—	—	V	DB ₀ - DB ₇	
"L" Output Voltage	V _{OL1}	I _O = 1.2mA	—	—	0.4	V		
"H" Output Voltage	V _{OH2}	I _O = -40μA	0.9V _{DD}	—	—	V	DO, CP, L, DF, OSC ₂	
"L" Output Voltage	V _{OL2}	I _O = 40μA	—	—	0.1V _{DD}	V		
Driver ON Resistor (COM pins)	R _{COM}	I _O = ±50μA, V _{LCD} = 4V	—	—	20	kΩ	COM ₁ - COM ₁₆	
Driver ON Resistor (SEG pins)	R _{SEG}	I _O = ±50μA, V _{LCD} = 4V	—	—	30	kΩ	SEG ₁ - SEG ₄₀	
Input Leakage Current	I _{IL}	V _I = V _{SS}	—	—	-1	μA	E	
		V _I = V _{DD}	—	—	1	μA		
Input Current	I _{IL2}	V _{DD} = 5.0V V _I = V _{SS}	-50	-125	-250	μA	R/W, RS DB ₀ - DB ₇	
		V _I = V _{DD} , excluding current flowing over pullup resistor and output drive MOS	—	—	2	μA		
Supply Current (1)	I _{DD1}	V _{DD} = 5.0V, resistor oscillation or external clock input via OSC ₁ . f _{OSC} = 270kHz. E is in "L" level. Other inputs are open. Output pins are all no load. *1	—	0.35	0.6	mA	V _{DD}	
Supply Current (2)	I _{DD2}	V _{DD} = 5.0V, ceramic oscillation, f _{OSC} = 250kHz. E is in "L" level. Other pins are open. Output pins are all no load. *1	—	0.55	0.8	mA	V _{DD}	
LCD Driving Bias Input Voltage	V _{LCD1}	V _{DD} -V ₅ *6	1/5 bias	3.0	—	6.0	V	V _{DD} , V ₁ , V ₂ , V ₃ , V ₄ , V ₅
	V _{LCD2}		1/4 bias	3.0	—	6.0		
Schmitt voltage width	V _{SUM}	—	0.6	0.7	0.8	V	E	
Built-in reset detection voltage	V _{RES}	—	—	—	3.0	V	V _{DD}	

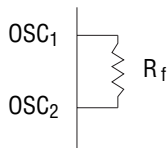
AC Characteristics

($V_{DD} = 4.5$ to $5.5V$, $T_a = -20$ to $+75^{\circ}C$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
R _f Clock Oscillation Frequency	f _{OSC1}	R _f = 91kΩ ± 2% *2	190	270	350	kHz	OSC ₁ OSC ₂
Clock Input Frequency	f _{IN}	OSC ₂ is open. Input from OSC ₁	125	250	350	kHz	OSC ₁
Input Clock Duty	f _{DUTY}	*3	45	50	55	%	OSC ₁
Input Clock Rise Time	t _r	*4	—	—	0.2	μs	OSC ₁
Input Clock Fall Time	t _f	*4	—	—	0.2	μs	OSC ₁
Ceramic Unit Oscillation Frequency	f _{OSC}	R _f = 510kΩ, C ₁ = C ₂ = 200 pF, R _d = 30kΩ, and Ceralock CSB250A. *5	245	250	255	kHz	OSC ₁ OSC ₂

*1 Applicable to the current that flows in pin V_{DD} when power is input as follows:
V_{DD} = 5V, GND = 0V, V₁ = 3.8V, V₂ = 2.6V, V₃ = 1.4V, V₄ = 0.2V, and V₅ = -1V.

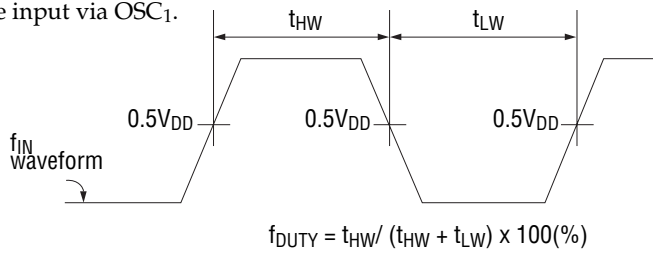
*2



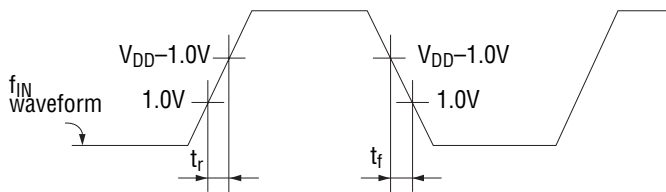
R_f = 91 kΩ ± 2%

Minimum wiring is required between OSC₁ and R_f and between OSC₂ and R_f.

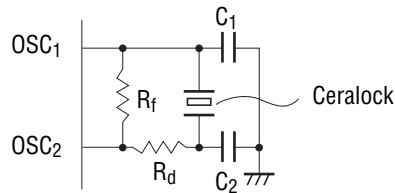
*3 Applied to pulse input via OSC₁.



*4 Applied to pulse input via OSC₁.



*5



Ceralock : CSB250A (mfd. by MURATA MFG.Co.)

R_f : 510kΩ ±5%

R_d : 30kΩ ±5%

C₁ : 200pF ±10%

C₂ : 200pF ±10%

Please contact us when using this circuit.

*6 Input the voltage listed in the table below to V₁ - V₅:

Pin	N (LCD lines)	
	1-line mode	2-line mode
V ₁	$V_{DD} - \frac{V_{LCD}}{4}$	$V_{DD} - \frac{V_{LCD}}{5}$
V ₂	$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{2V_{LCD}}{5}$
V ₃	$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{3V_{LCD}}{5}$
V ₄	$V_{DD} - \frac{3V_{LCD}}{4}$	$V_{DD} - \frac{4V_{LCD}}{5}$
V ₅	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

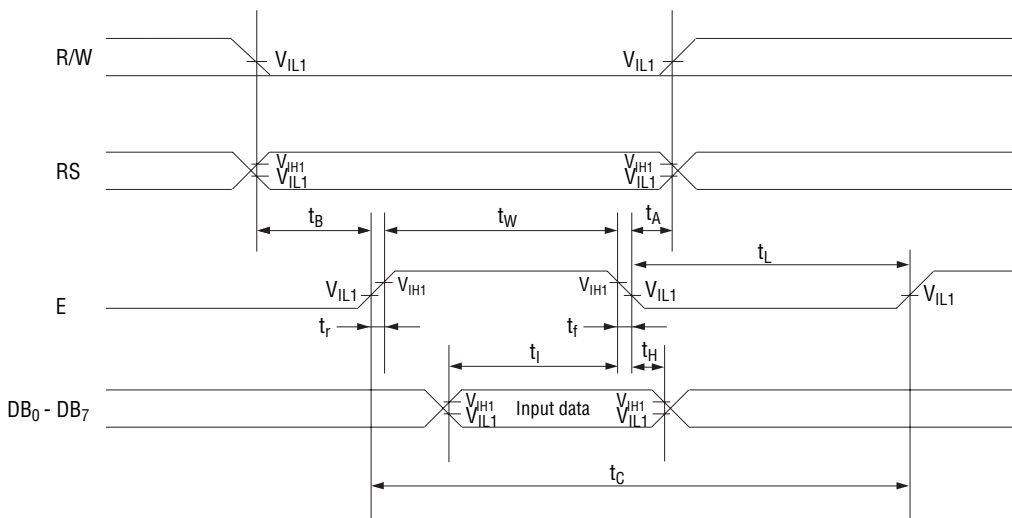
V_{LCD} is an LCD driving voltage. (For "N" (number of LCD lines), refer to the initial set of the instruction code.)

Switching Characteristics

- Timing for input from the CPU

($V_{DD} = 4.5$ to $5.5V$, $T_a = -20$ to $+75^{\circ}C$)

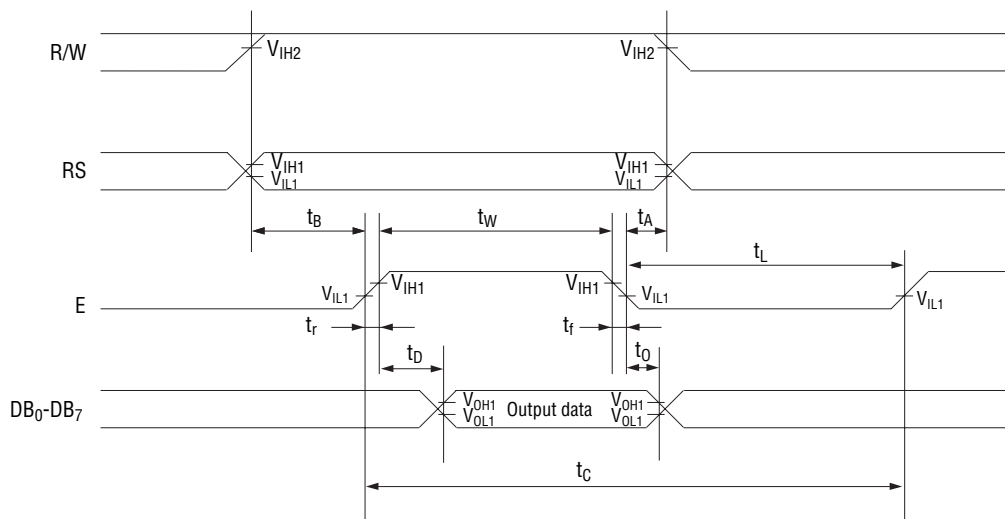
Parameter	Symbol	Min.	Typ.	Max.	Unit
R/W and RS setup time	t_B	140	—	—	ns
E "H" pulse width	t_W	280	—	—	ns
R/W and RS hold time	t_A	10	—	—	ns
E rise time	t_r	—	—	100	ns
E fall time	t_f	—	—	100	ns
E "L" pulse width	t_L	280	—	—	ns
E cycle time	t_C	667	—	—	ns
DB ₀ to DB ₇ input data setup time	t_I	180	—	—	ns
DB ₀ to DB ₇ input data hold time	t_H	10	—	—	ns



• Timing for output to the CPU

($V_{DD} = 4.5$ to $5.5V$, $T_a = -20$ to $+75^{\circ}C$)

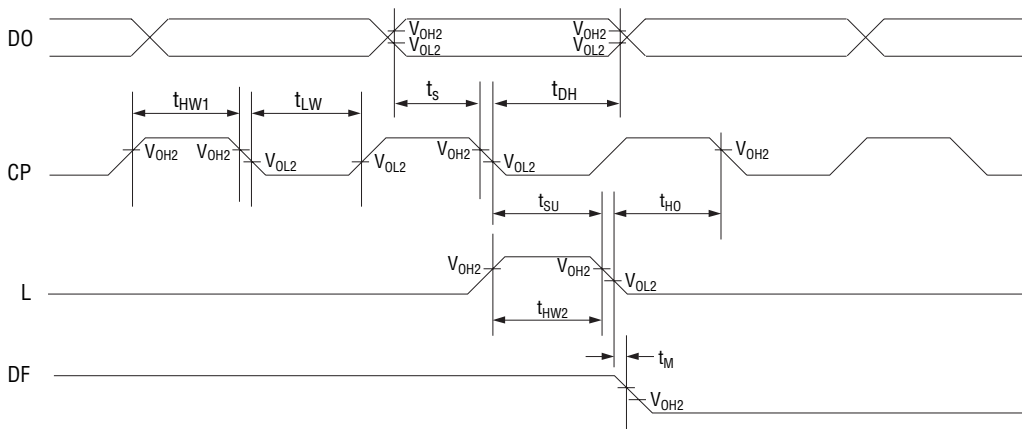
Parameter	Symbol	Min.	Typ.	Max.	Unit
R/W and RS setup time	t_B	140	—	—	ns
E "H" pulse width	t_W	280	—	—	ns
R/W and RS hold time	t_A	10	—	—	ns
E rise time	t_r	—	—	100	ns
E fall time	t_f	—	—	100	ns
E "L" pulse width	t_L	280	—	—	ns
E cycle time	t_C	667	—	—	ns
DB ₀ to DB ₇ data output delay time	t_D	—	—	220	ns
DB ₀ to DB ₇ data output hold time	t_O	20	—	—	ns



• Timing for output to MSM5259

($V_{DD} = 4.5$ to $5.5V$, $T_a = -20$ to $+75^{\circ}C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CP "H" pulse width	t_{HW1}	800	—	—	ns
CP "L" pulse width	t_{LW}	800	—	—	ns
DO setup time	t_s	300	—	—	ns
DO holding time	t_{DH}	300	—	—	ns
"L" clock set-up time	t_{SU}	500	—	—	ns
"L" clock hold time	t_{HO}	100	—	—	ns
"L" "H" pulse width	t_{HW2}	800	—	—	ns
DF delay time	t_M	-1000	—	1000	ns



FUNCTIONAL DESCRIPTION

Instruction Register (IR) and Data Register (DR)

These two registers are selected by the REGISTER SELECTION (RS) pin.

The DR is selected when the "H" level is input to the RS pin and IR is selected when the "L" level is input.

The IR is used to store the address of the display data RAM (DD RAM) or character generator RAM (CG RAM) and instruction code.

The IR can be written, but not be read by the microcomputer (CPU).

The DR is used to write and read the data to and from the DD RAM or CG RAM.

The data written to DR by the CPU is automatically written to the DD RAM or CG RAM as an internal operation.

When an address code is written to IR, the data (of the specified address) is automatically transferred from the DD RAM or CG RAM to the DR. Next, when the CPU reads the DR, it is possible to verify DD RAM or CG RAM data from the DR data.

After the writing of DR by the CPU, the next address in the DD RAM or CG RAM is selected to be ready for the next CPU writing.

Likewise, after the reading out of DR by the CPU, DD RAM or CG RAM data is read out by the DR to be ready for the next CPU reading.

Write/read to and from both registers is carried out by the READ/WRITE (R/W) pin.

Table 1 RS and R/W pins functions

R/W	RS	Function
L	L	IR write
H	L	Read of busy flag (BF) and address counter (ADC)
L	H	DR write
H	H	DR read

Busy Flag (BF)

When the busy flag is at "H", it indicates that the ML9040A-Axx/-Bxx is engaged in internal operation.

When the busy flag is at "H", any new instruction is ignored.

When R/W = "H" and RS = "L", the busy flag is output from DB₇.

New instruction should be input when busy flag is "L" level.

When the busy flag is at "H", the output code of the address counter (ADC) is undefined.

Address Counter (ADC)

The address counter (ADC) allocates the address for the DD RAM and CG RAM write/read and also for the cursor display.

When the instruction code for a DD RAM address or CG RAM address setting is input to IR, after deciding whether it is DD RAM or CG RAM, the address code is transferred from IR to ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC is incremented (decremented) by 1 internally.

The data of the ADC is output to DB₀ - DB₆ on the conditions that R/W = "H", RS = "L", and BF = "L".

Timing Generator Circuit

This circuit is used to generate timing signals to activate internal operations upon receipt of CPU instruction and also from such internal circuits as the DD RAM, CG RAM, and CG ROM.

It is designed so that the internal operation caused by accessing from the CPU will not interfere with the internal operation caused by LCD driving. Consequently, when data is written from the CPU to DD RAM, flickering does not occur in a display area other than the display area where the data is written.

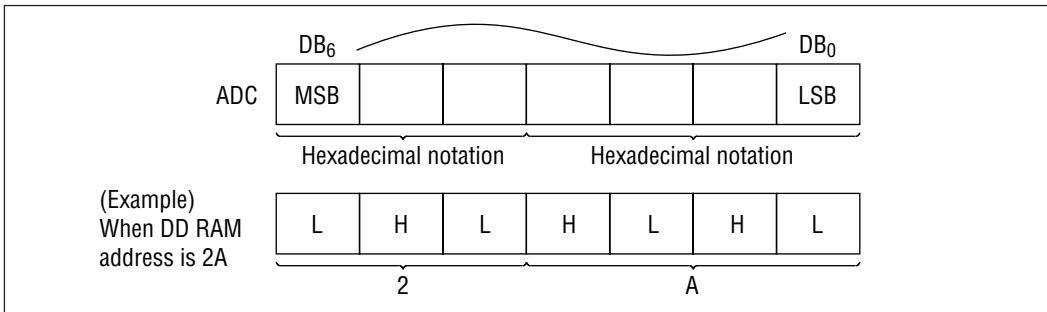
In addition, this circuit generates the transfer signal to MSM5259 for display character expansion.

Display Data RAM (DD RAM)

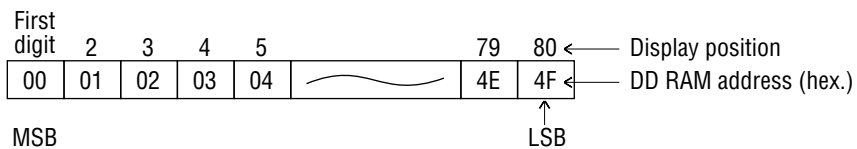
This RAM is used to store display data of 8-bit character codes (see Table 2).

DD RAM address corresponds to the display position of the LCD. The correspondence between the two is described in the following.

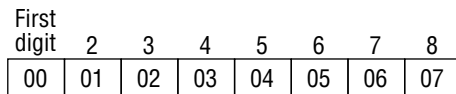
DD RAM address (set to ADC) is expressed in hexadecimal notation as shown below:



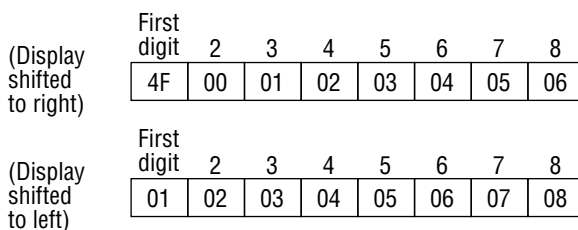
(1) Correspondence between address and display position in the 1-line display mode



(2) When the ML9040A-Axx/-Bxx alone is used, up to 8 characters can be displayed from the first to eighth digit.



When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:



- (3) When the ML9040A-Axx/-Bxx is used with one MSM5259, up to 16 characters can be displayed from the first to sixteenth digit as shown below:

First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

ML9040A-Axx/-Bxx display
 MSM5259 display

When the display is shifted by instruction, the correspondence between the LCD display and the DD RAM address changes as shown below:

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(Display shifted to right)	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

ML9040A-Axx/-Bxx display
 MSM5259 display

(Display shifted to left)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
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- (4) Since the ML9040A-Axx/-Bxx has a DD RAM capacity of up to 80 characters, up to 9 MSM5259 devices can be connected to ML9040A-Axx/-Bxx so that 80 characters can be displayed.

First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		73	74	75	76	77	78	79	80
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	----	48	49	4A	4B	4C	4D	4E	4F

ML9040A-Axx/-Bxx display
MSM5259 (1) display
MSM5259 (2) - (8) display
 MSM5259 (9) display

(5) Correspondence between address and display position in the 2-line display mode

	First digit	2	3	4	5		39	40	← Display position
First line	00	01	02	03	04		26	27	← DD RAM address (hex.)
Second line	40	41	42	43	44		66	67	←

(Note) The last address of the first line is not consecutive to the head address of the second line.

(6) When ML9040A-Axx/-Bxx alone is used, up to 16 characters (8 characters x 2 lines) can be displayed from the first to eighth digit.

	First digit	2	3	4	5	6	7	8
First line	00	01	02	03	04	05	06	07
Second line	40	41	42	43	44	45	46	47

When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:

		First digit	2	3	4	5	6	7	8
(Display shifted to right)	First line	27	00	01	02	03	04	05	06
	Second line	67	40	41	42	43	44	45	46
(Display shifted to left)	First line	01	02	03	04	05	06	07	08
	Second line	41	42	43	44	45	46	47	48

(7) When the ML9040A-Axx/-Bxx is used with one MSM5259, up to 32 characters (16 characters x 2 lines) can be displayed from the first to the sixteenth digit.

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

ML9040A-Axx/-Bxx display
 MSM5259 display

Table 2 Relationship Between Character Codes and Characters (Character Patterns) of ML9040A-A01/-B01

Lower 4 bits \ Upper 4 bits	MSB 0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000 LSB	CG RAM (1)		0	0	@	Q	P	\	'	p	P		
0001	(2)	!	1	1	A	Q	Q	a	a	q	q	。	。
0010	(3)	"	2	2	B	R	R	b	b	r	r	「	「
0011	(4)	#	3	3	C	S	S	c	c	s	s	」	」
0100	(5)	\$	4	4	D	T	T	d	d	t	t	、	、
0101	(6)	%	5	5	E	U	U	e	e	u	u	・	・
0110	(7)	&	6	6	F	V	U	f	f	v	v	ヲ	ヲ
0111	(8)	'	7	7	G	W	U	g	g	w	w	ア	ア
1000	(1)	(8	8	H	X	X	h	h	x	x	イ	イ
1001	(2))	9	9	I	Y	Y	i	i	y	y	ウ	ウ
1010	(3)	*	:	:	J	Z	Z	j	j	z	z	エ	エ
1011	(4)	+	;	;	K	[[k	k	{	{	オ	オ
1100	(5)	,	<	<	L	¥	¥	l	l	l	l	ヤ	ヤ
1101	(6)	-	=	=	M]]	m	m	}	}	ユ	ユ
1110	(7)	.	>	>	N	^	^	n	n	→	→	ヨ	ヨ
1111	(8)	/	?	?	O	_	_	o	o	←	←	ッ	ッ

Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character patterns other than character patterns in the CG ROM.

The CG RAM has a capacity (64 bytes = 512 bits) of writing 8 kinds of characters for 5 x 7 dots and 4 kinds of characters for 5 x 10 dots.

When displaying character patterns stored in the CG RAM, write 8-bit character codes (00 to 07 or 08 to 0F; hex.) on the left side as shown in Table 2. Then it is possible to output the character pattern to the LCD display position corresponding to the DD RAM address.

The following explains how to write and read character patterns to and from the CG RAM.

(1) When the character pattern is 5 x 7 dots (see Table 3-1).

- A method of writing character pattern to the CG RAM by CPU:

Three bits of CG RAM addresses 0-2 correspond to the line position of the character pattern.

First, set increment or decrement by the CPU, and then input the CG RAM address. After this, write character patterns to the CG RAM through DB₀ - DB₇ line by line. DB₀ to DB₇ correspond to CG RAM data 0-7 in Table 3-1.

It is displayed when "H" is set as input data and is not displayed when "L" is set as input data.

Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.

The line, in which the CG RAM addresses 0-2 are all "H" ("7" in hexadecimal notation), is the cursor position. It is ORed with the cursor at the cursor position and displayed to LCD.

For this reason, it is necessary to set all input data that become cursor positions to "L". Although CG RAM data 0-4 bits are output to the LCD as display data, CG RAM data bits 5-7 are not output. The latter can be written and read to and from the RAM, it is therefore allowed to be used as data RAM.
- A method of displaying the CG RAM character pattern to the LCD:

The CG RAM is selected when upper 4 bits of the character codes are all "L".

As character code bit 3 is invalid, the display of "0" in Table 3-1, is selected by character code "00" (hex.) or "08" (hex.).

When the 8-bit character code of the CG RAM is written to the DD RAM, the character pattern of the CG RAM is displayed on the LCD display position corresponding to the DD RAM address. (DD RAM data, bits 0-2 correspond to CG RAM address, bits 3-5.)

(2) When character pattern is 5 x 10 dots (see Table 3-2).

- A method of writing character pattern into the CG RAM by the CPU:

Four bits of CG RAM address, bits 0-3, correspond to the line position of the character pattern.

First, set increment or decrement with the CPU, and then input the address of the CG RAM.

After this, write the character pattern code into the CG RAM, line by line from DB₀-DB₇.

DB₀ to DB₇ correspond to CG RAM data, bits 0-7, in Table 3-2.

It is displayed when "H" is set as input data, while it is not displayed when "L" is set as input data.

As the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.

The line, the CGRAM addresses 0-3 of which are "A" in hexadecimal notation, is the cursor position. The CGRAM data is 0Red with the cursor at the cursor position and displayed to LCD. For this reason, it is necessary to set all input data that become cursor positions to "L".

When the CG RAM data, bits 0-4, and CG RAM addresses, bits 0-3, are "0" to "A", they are displayed on the LCD as the display data. When the CG RAM data, bits of 5-7, and CG RAM, bit data is 0-4 and CG RAM address data is "B" to "F", it is not output to the LCD.

But in this case, CG RAM can be used as RAM and it can be written into/read out. So, it can be used as the data RAM.
- A method of displaying the CG RAM character pattern to the LCD:

The CG RAM is selected when 4-upper order bits of the character code are all "L".

As character code bits 0 and 3 are invalid, the display of "μ" is selected by character codes "00", "01", "08", and "09" (hex.) as in Table 3-2.

When the CG RAM character code is written to the DD RAM, the CG RAM character pattern is displayed on the LCD display position corresponding to the DD RAM address.

(DD RAM data bits 1 and 2 correspond to CG RAM address bits 4 and 5.)

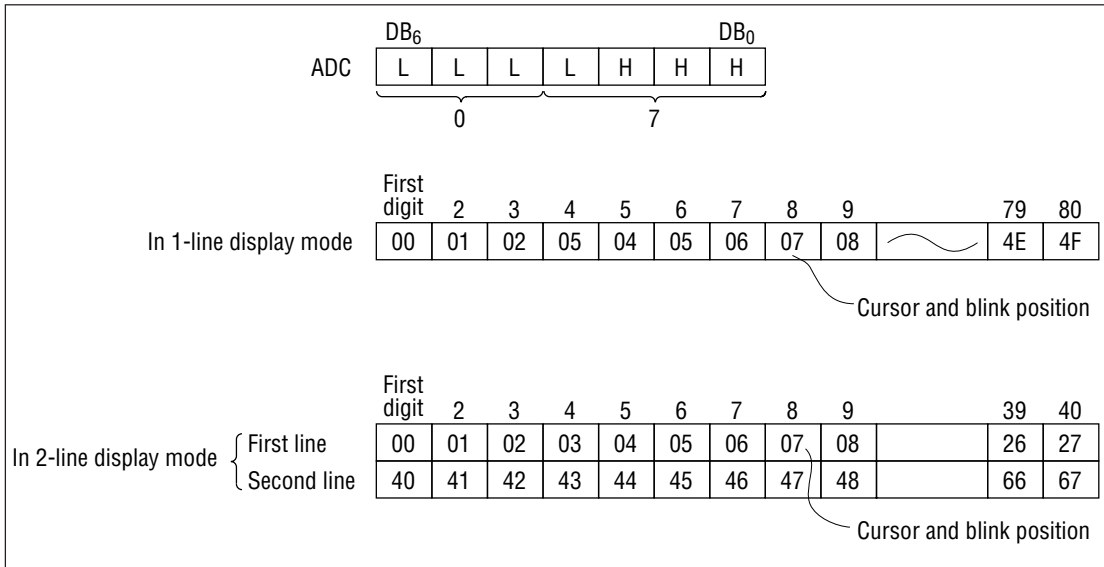
Cursor/Blink Control Circuit

This is a circuit that generates the LCD cursor and blink.

This circuit is under the control of the CPU program.

The display of the cursor and blink on the LCD is made at a position corresponding to the DD RAM address that is set in the ADC.

The figure below shows an example of the cursor/blink position when the value of ADC is set to "07" (hex.).



(Note) The cursor and blink are displayed even when the CG RAM address is set in the ADC. For this reason, it is necessary to inhibit the cursor and blink display while the CG RAM address is set in the ADC.

LCD Display Circuit (COM₁ to COM₁₆, SEG₁ to SEG₄₀, L, CP, DO, and DF)

As the ML9040A-Axx/-Bxx provides the COM signal outputs (16 outputs) and the SEG signal outputs (40 outputs), it can display 8 characters (1-line display) or 16 characters (2-line display) as a unit.

SEG₁ to SEG₄₀ are used to display 8-digit display on the LCD. To expand the display, an MSM5259 is used.

The MSM5259, 40-dot segment driver, is used for expansion of the SEG signal output. Interface with the MSM5259 is made through data output pin (DO), clock output pin (CP), latch output pin (L), and display frequency pin (DF). The character pattern data is serially transferred to MSM5259 through DO and CP. When the data of 72 characters 360-bit (= 5-bit/ch. x 72 ch. = 1-line display) or 32 characters 160-bit (5-bit/ch. x 32 ch. = 2-line display) is output, the latch pulse is also output through pin L. By this latch pulse, the data transferred serially to MSM5259 is latched to be used as display data. The display frequency signal (DF) required when LCD is displayed is also output from DF pin synchronously with this latch pulse.

Built-in Reset Circuit

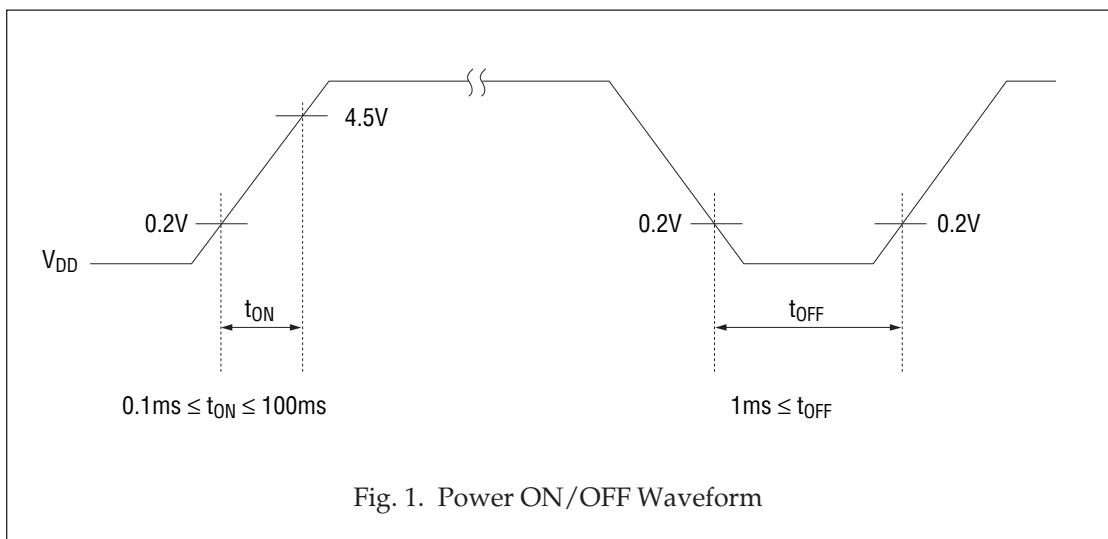
The ML9040A-Axx/-Bxx is automatically initialized when the power is turned on. During initialization, the busy flag (BF) holds "H" and does not accept instructions (other than the busy flag read).

The busy flag holds "H" for 15 ms after V_{DD} reaches 4.5V or more.

During initialization, the ML9040A-Axx/-Bxx executes the following instructions:

- Display clear
- Data length of interface with CPU: 8 bits (8B/4B = "H")
- LCD: 1-line display (N = "L")
- Character font: 5 x 7 dots (F = "L")
- ADC: Increment (I/D = "H")
- No display shift (SH = "L")
- Display: Off (DI = "L")
- Cursor: Off (C = "L")
- No blink (B = "L")

It is required to satisfy the following power supply conditions.



Data Bus Connected with CPU

The data bus connected with CPU is available either once for 8 bits or twice for 4 bits. This allows the ML9040A-Axx/-Bxx to be interfaced with either an 8-bit or 4-bit CPU.

(1) When the interface data bus is 8 bits

Data bus DB₀ to DB₇ (8 lines) are all used and data input/output is carried out in one step.

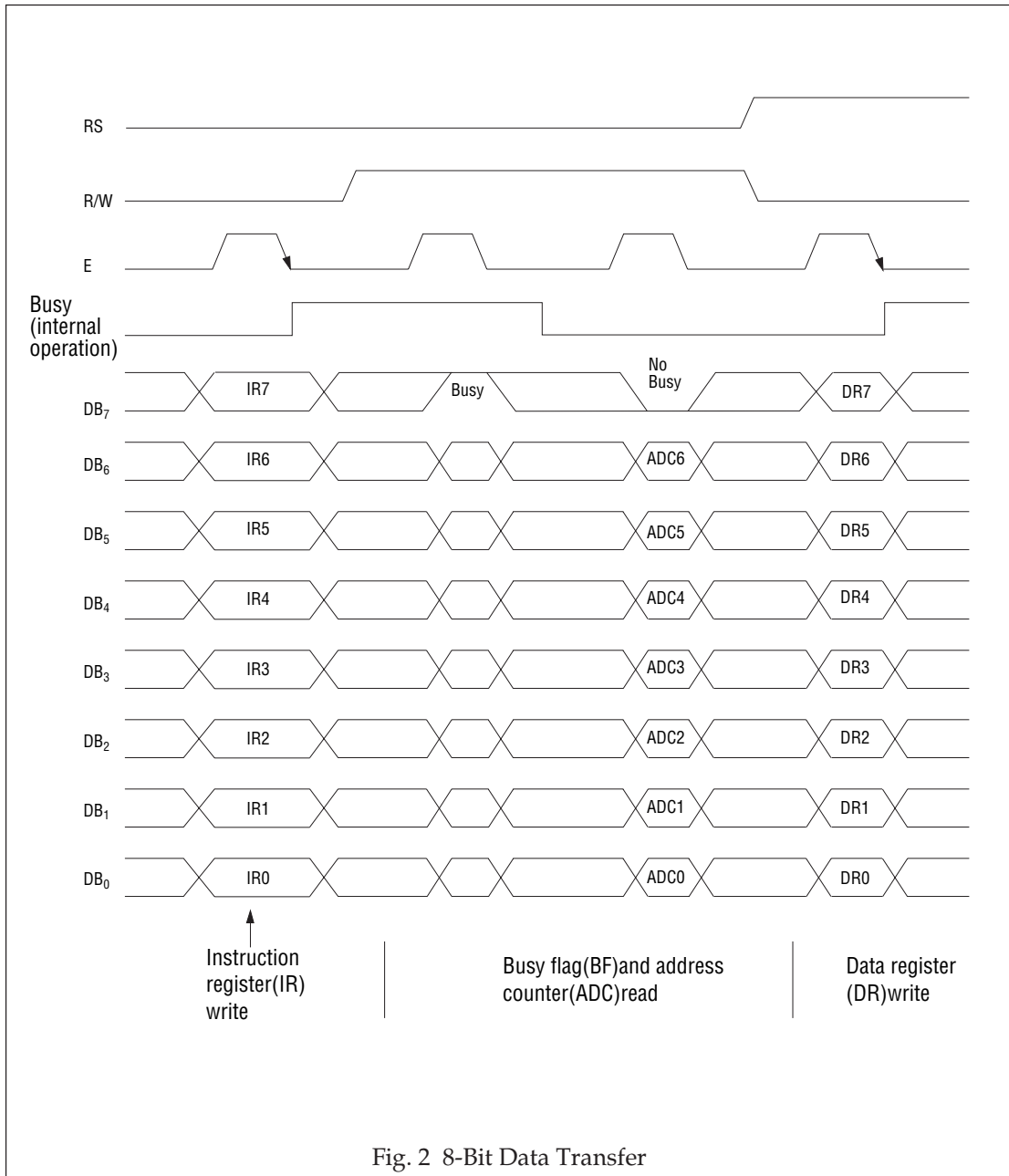
(2) When the interface data bus is 4 bits

The 8-bit data input/output is carried out in two steps by using only high-order 4 bits of data bus DB₄ to DB₇ (4 lines)

The first time data input/output is made for 4-high order bits (DB₄ to DB₇) and the second time data input/output is made for low-order 4 bits (DB₀ to DB₃). Even when the data input/output can be completed through high-order 4 bits, be sure to make another input/output of low-order 4 bits.

(Example: Busy flag Read).

Since the data input/output is carried out in two steps as one execution, no normal data transfer is executed from the next input/output if accessed only once.



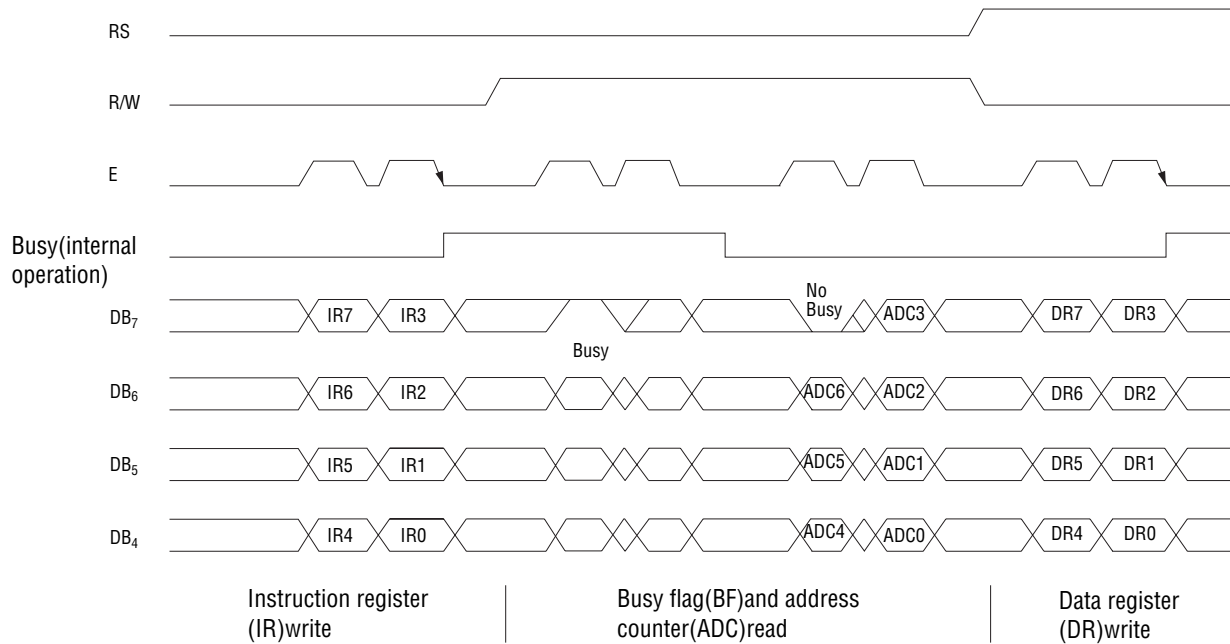


Fig. 3 4-Bit Data Transfer

Instruction Code

The instruction code is defined as the signal through which the ML9040A-Axx/-Bxx is accessed by the CPU.

The ML9040A-Axx/-Bxx begins operation upon receipt of the instruction code input. As the internal processing operation of ML9040A-Axx/-Bxx starts in a timing that does not affect the LCD display, the busy status continues for longer than the CPU cycle time. Under the busy status (when the busy flag is set to "H"), the ML9040A-Axx/-Bxx does not execute any instructions other than the busy flag read.

Therefore, the CPU has to verify that the busy flag is set to "L" prior to the input of the instruction code.

(1) Display clear:

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	L	L	L	L	L	L	H

When this instruction is executed, the LCD display is cleared.

I/D in the entry mode setting is set to "H" (increment). SH does not change.

When the cursor and blink are in display, the blinking position moves to the left end of the LCD (the left end of the first line in the 2-line display mode).

(Note) All DD RAM data goes to "20" (hex.), while the address counter (ADC) goes to "00" (hex.). The execution time is 1.53 ms (max.), when the OSC oscillation frequency is 270 kHz.

(2) Cursor home

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	L	L	L	L	L	H	X

X: Don't Care

When this instruction is executed while the cursor and blink are being displayed, the blinking position moves to the left end of the LCD (to the left end of the first line in the 2-line display mode).

While the display is in shift, the display returns to its original position before shifting.

(Note) The address counter (ADC) goes to "00" (hex.). The execution time is 1.53 ms (max.), when the OSC oscillation frequency is 270 kHz.

(3) Entry mode setting

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	L	L	L	L	H	I/D	SH

- ① When the I/D is set, the 8-bit character code is written or read to and from the DD RAM, the cursor and blink shift to the right by 1 character position (I/D = "H"; increment) or to the left by 1 character position (I/D = "L"; decrement).
The address counter is incremented (I/D = "H") or decremented (I/D = "L") by 1 at this time. Even after the character pattern code is written or read to and from the CG RAM, the address counter (ADC) is incremented (I/D = "H") or decremented (I/D = "L") by 1.
- ② When SH = "H" is set, the character code is written to the DD RAM. Then the cursor and blink stop and the entire display shifts to the left (I/D = "H") or to the right (I/D = "L") by 1 character position.
When the character is read from the DD RAM during SH = "H", or when the character pattern data is written or read to or from the CG RAM during SH = "H", the entire display does not shift, but normal write/read is performed (the entire display does not shift, but the cursor and blink shift to the right (I/D = "H") or to the left (I/D = "L") by 1 character position.
When SH = "L" is set, the display does not shift, but normal write/read is performed.
The execution time when the OSC oscillation frequency is 270 kHz is 37 μs.

(4) Display mode setting

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	L	L	L	H	DI	C	B

- ① The DI bit controls whether the character pattern is displayed or not displayed.
When DI is "H", this bit makes the LCD display the character pattern.
When DI is "L", the LCD character pattern is not displayed. The cursor and blink are also cancelled at this time.

(Note) Unlike the display clear, the character code is not rewritten at all.
- ② The cursor is not displayed when C = "L" and is displayed when DI = "H" and C = "H".
- ③ The blink is cancelled when B = "L" and is executed when DI = "H" and B = "H".
In the blink mode, all dots (including the cursor) and displaying character pattern and cursor are displayed alternately at 379.2 ms (in 5 x 7 dots character font) or 521.5 ms (in 5 x 10 dots character font) when the OSC oscillation frequency is 270 kHz. The execution time when the OSC oscillation frequency is 270 kHz is 37 μs.

(5) Cursor and display shift

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	L	L	H	D/C	R/L	X	X

X: Don't Care

When D/C = "L" and R/L = "L", the cursor and blink positions are shifted to the left by 1 character position (ADC is decremented by 1).

When D/C = L and R/L = "H", the cursor and blink positions are shifted to the right by 1 character position (ADC is incremented by 1).

When D/C = "H" and R/L = "L", the entire display is shifted to the left by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).

When D/C = "H" and R/L = "H", the entire display is shifted to the right by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).

In the 2-line display mode, the cursor and blink positions are shifted from the first to the second line when the cursor is shifted to the right next to the fortieth digit (27; hex.) in the first line. No such shifting is made in other cases.

When shifting the entire display, the display pattern, cursor, and blink positions are in no case shifted between lines (from the first to the second line or vice versa).

The execution time, when the OSC oscillation frequency is 270 kHz, is 37 μs.

(6) Initial setting

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	L	H	8B/4B	N	F	X	X

X: Don't Care

- ① When 8B/4B = "H", the data input/output to and from the CPU is carried out simultaneously by means of 8 bits DB₇ to DB₀.
When 8B/4B = "L", the data input/output to and from the CPU is carried out in two steps through 4 bits of DB₇ to DB₄.
- ② The 2-line display mode of the LCD is selected when N = "H", while the 1-line display mode is selected when N = "L".
- ③ The 5 x 7 dots character font is selected when F = "L", while the 5 x 10 dots character font is selected when F = "H" and N = "L".
This initial setting has to be accessed prior to other instructions except for the busy flag read after the power is supplied to the ML9040A-Axx/-Bxx.

N	F	Number of display lines	Character font	Duty ratio	Number of biases	Number of COMMOM signals
L	L	1 line	5 x 7 dots	1/8	4	8
L	H	1 line	5 x 10 dots	1/11	4	11
H	L	2 lines	5 x 7 dots	1/16	5	16
H	H	2 lines	5 x 7 dots	1/16	5	16

Generate biases externally and input them to V_{DD} , V_1 , V_2 , V_3 , V_4 , and V_5 .
When the number of biases is 4, input the same potential to V_2 and V_3 . The execution time, when the OSC oscillation frequency is 270 kHz, is 37 μ s.

(7) CG RAM address setting

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	L	H	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀

When CG RAM addresses, bits C₅ to C₀ (binary), are set, the CG RAM is specified, until the DD RAM address is set.

Write/read of the character pattern to and from the CPU begins with addresses, bits C₅ to C₀, starting from CG RAM selection.

The execution time, when the OSC oscillation frequency is 270 kHz, is 37 μ s.

(8) DD RAM address setting

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	L	H	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

When the DD RAM addresses D₆ to D₀ (binary) are selected, the DD RAM is specified until the DD RAM address is set.

Write/read of the character code to and from the CPU begins with addresses D₆ to D₀ starting from DD RAM selection.

In the 1-line display mode (N = H), however, D₆ to D₀ (binary) must be set to one of the values among "00" to "4F" (hex.).

Likewise, in the 2-line mode, D₆ to D₀ (binary) must be set to one of the values among "00" to "27" (hex.) or "40" to "67" (hex.).

When any value other than the above is input, it is impossible to make a normal write/read of character codes to and from the DD RAM.

The execution time, when the OSC oscillation frequency is 270 kHz, is 37 μ s.

(9) DD RAM and CG RAM data write

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	L	H	E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀

When E₇ to E₀ (binary) codes are written to the DD RAM or CG RAM, the cursor and display move as described in "(5) Cursor and display shift". The execution time, when the OSC oscillation frequency is 270 kHz, is 37 μ s.

(10) Busy flag and address counter read (Execution time is 1 μ s.)

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	H	L	BF	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀

The busy flag (BF) is output by this instruction to indicate whether the ML9040A-Axx/-Bxx is engaged in internal operations (BF = "H") or not (BF = "L").

When BF = "H", no new instruction is accepted. It is therefore necessary to verify BF = "L" before inputting a new instruction.

When BF = "L", a correct address counter value is output. The address counter value must match the DD RAM address or CG RAM address. The decision of whether it is a DD RAM address or CG RAM address is made by the address previously set.

Since the address counter value when BF = "H" is sometimes incremented or decremented by 1 during internal operations, it is not always a correct value.

(11) DD RAM and CG RAM data read

	R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Instruction code	H	H	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀

Character codes (bits P₇ to P₀) are read from the DD RAM, while character patterns (P₇ to P₀) from the CG RAM.

Selection of DD RAM or CG RAM is decided by the address previously set.

After reading those data, the address counter (ADC) is incremented or decremented by 1 as set by the shift mode mentioned in item "(3) shift mode set".

The execution time, when the OSC oscillation frequency is 270 kHz, is 37 μ s.

(Note) Conditions for the reading of correct data:

- ① When the DD RAM address set or CG RAM address set is input before inputting this instruction.
- ② When the cursor/display shift is input before inputting this instruction in case the character code is read.
- ③ Data after the second reading from RAM when read more than 2 times. Correct data is not output in any other case.

Interface with LCD and MSM5259

Display examples when setting the 5 x 7 dots character font 1-line mode, 5 x 10 dots character font 1-line mode, and 5 x 7 dots character font 2-line mode through instructions are shown in Figures 4, 5, and 6, respectively.

When the 5 x 7 dots character font is set in the 1-line display mode, the COM signals COM₉ to COM₁₆ are output for extinguishing.

Likewise, when the 5 x 10 dots character font (1-line is set), the COM signals COM₁₂ to COM₁₆ are output for display-off.

The display example shows a combination of 16 characters (32 characters for the 2-line display mode) and the LCD. When the number of MSM5259s are increased according to the increase in the number of characters, it is possible to display a maximum of 80 characters.

Besides, it is necessary to generate bias voltage required for LCD operation by splitting resistors outside the IC to input it to ML9040A-Axx/-Bxx and MSM5259.

Examples of these bias voltages are shown in Figures 7, 8, 9, and 10. Basically, this can be done by dividing the voltage by the resistors as shown in Figures 7 and 8. If the value of resistor R is made larger to reduce system power consumption, the LCD operating margin decreases and the LCD driving waveform is distorted. To prevent this, a by-pass capacitor is serially connected to the resistor to lower voltage division impedance caused by the splitting of resistors as shown in Figures 9 and 10.

As the values of R, VR, and C vary according to the LCD size used and V_{LCD} (LCD drive voltage), these values have to be determined through actual experimentation in combination with the LCD.

(Example set values: R = 3.3 to 10kΩ, V_R = 10 to 30kΩ, and C = 0.0022 μF to 0.047 μF)

Figure 17 shows an application circuit for the ML9040A-Axx/-Bxx and MSM5259 including a bias circuit.

The bias voltage has to maintain the following potential relation:

$$V_{DD} > V_1 > V_2 \geq V_3 > V_4 > V_5$$

- In the case of 1-line 16 characters display (5 x 7 dots/font)

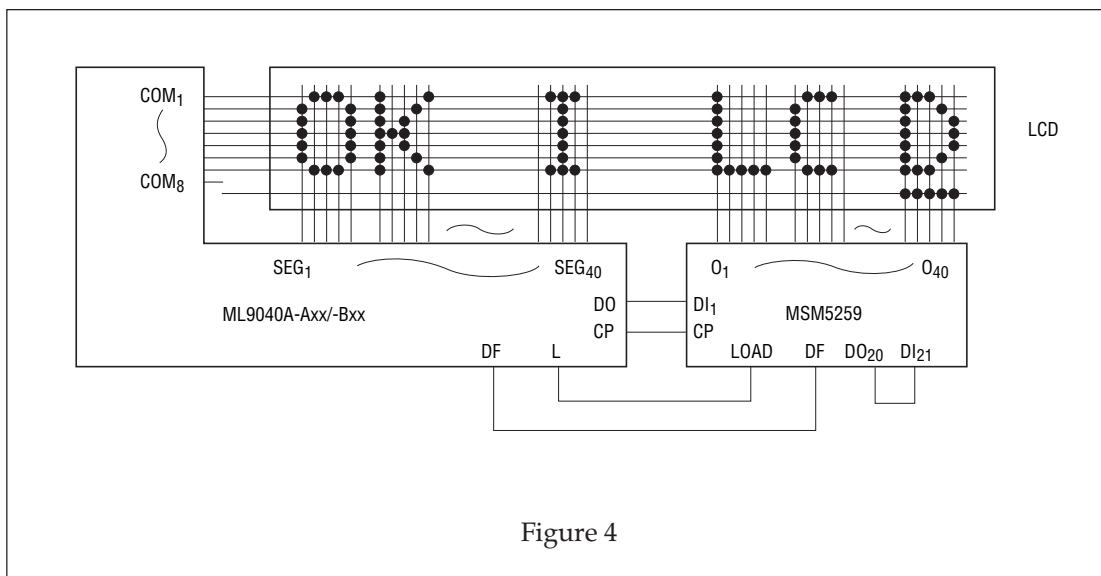
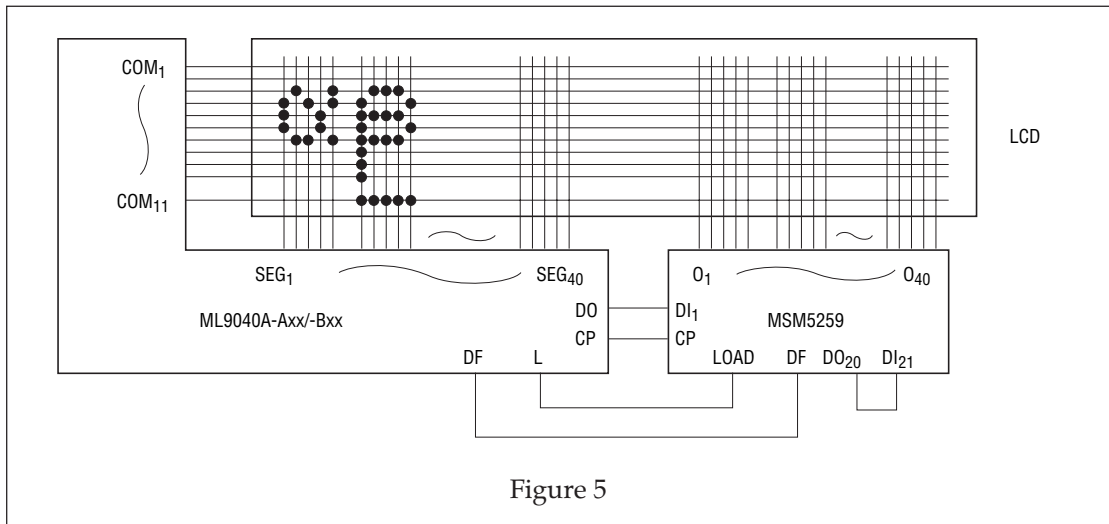
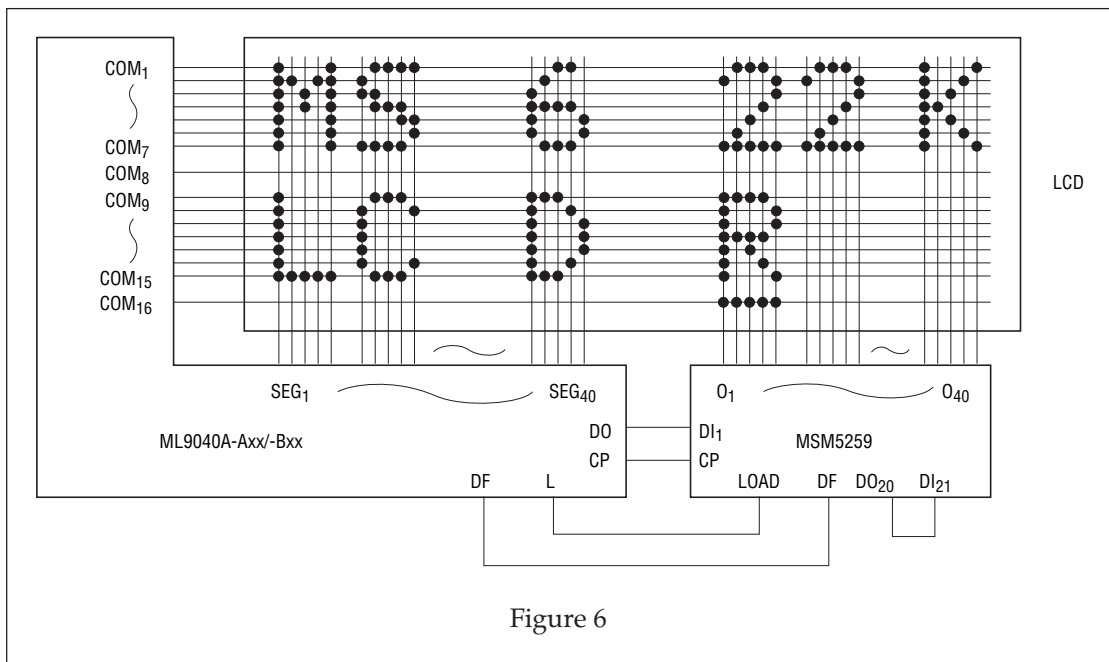


Figure 4

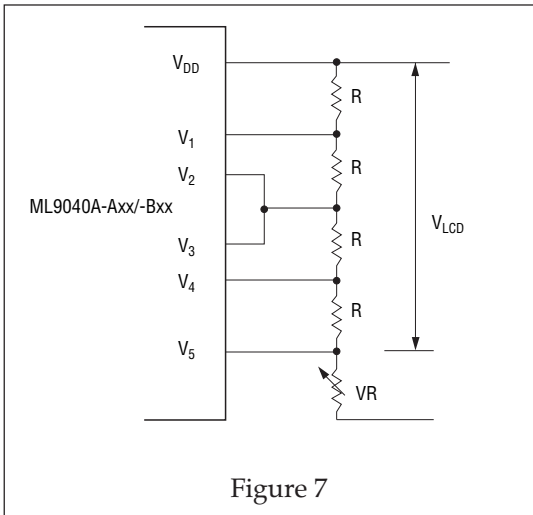
- In the case of 16-character (1 line) display (5 x 10 dots/font)



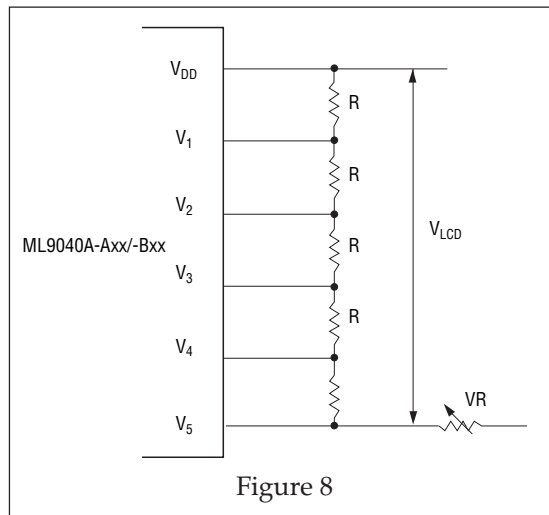
- In the case of 16-character (2 lines) display (5 x 7 dots/font)



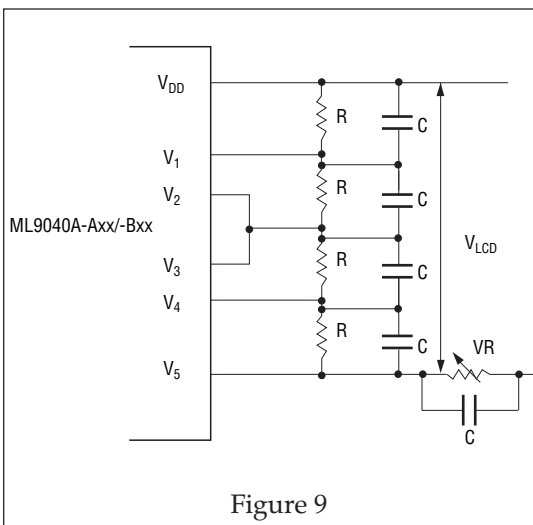
• Bias voltage circuit (1-line display mode)



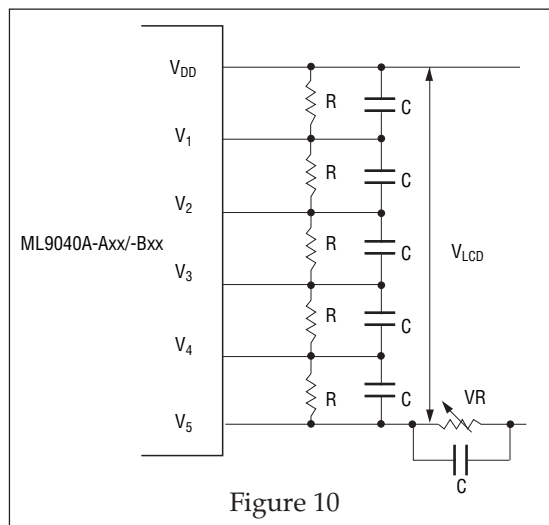
• Bias voltage circuit (2-line display mode)



• Bias voltage circuit (1-line display mode)



• Bias voltage circuit (2-line display mode)



(V_{LCD} : LCD driving voltage)

• Application circuit

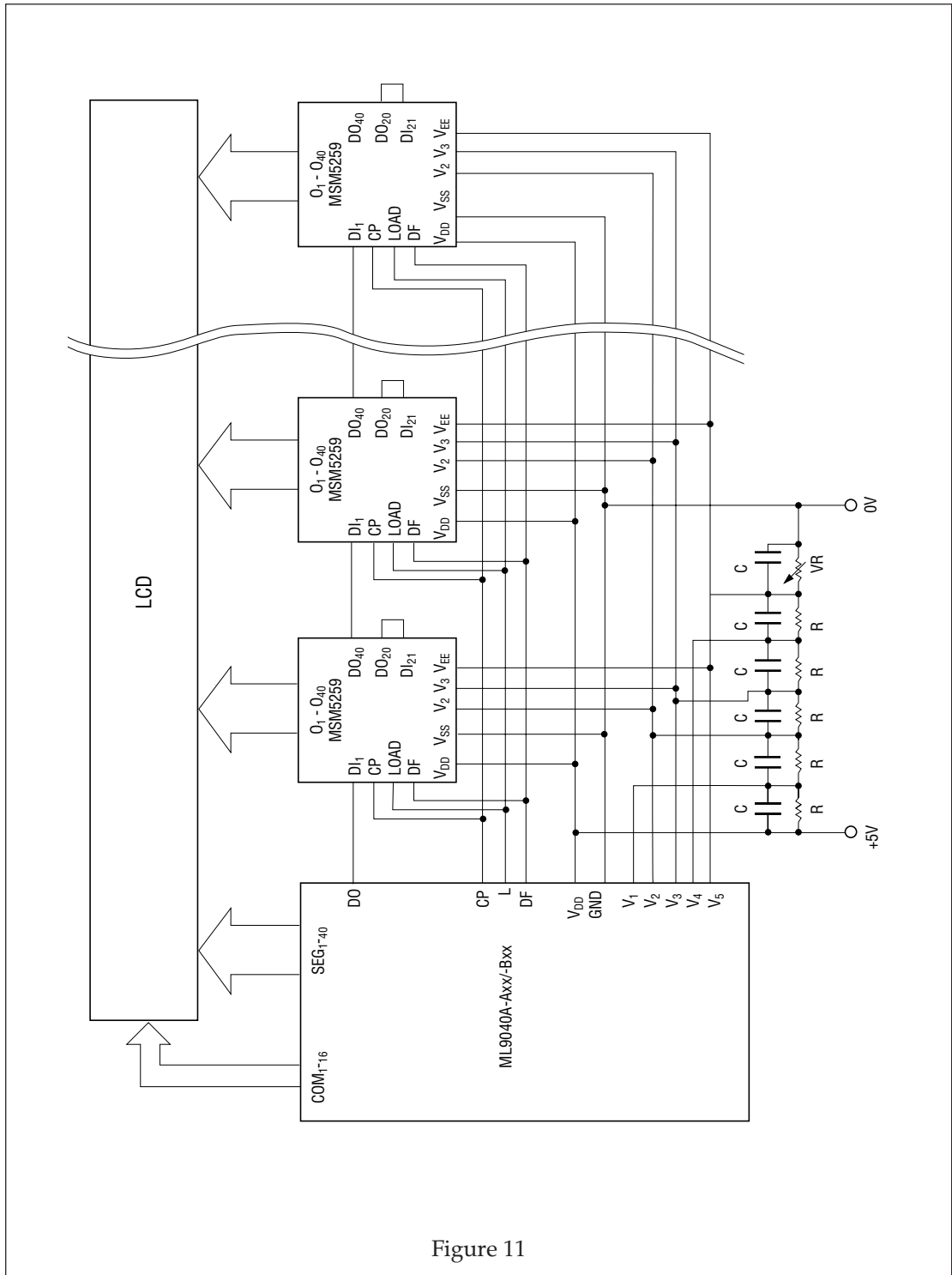


Figure 11

LCD Drive Waveforms

Figures 12, 13 and 17 show the LCD driving waveforms consisting of COM signal, SEG signal, DF signal and L (latch pulse waveform) signal, in the duty of 1/8, 1/11 and 1/16 respectively. The relation between duty and frame frequency is described in the table below.

Duty	Frame frequency
1/8	84.3 Hz
1/11	61.4 Hz
1/16	84.3 Hz

(Note) The OSC oscillation frequency is assumed to be 270 kHz.

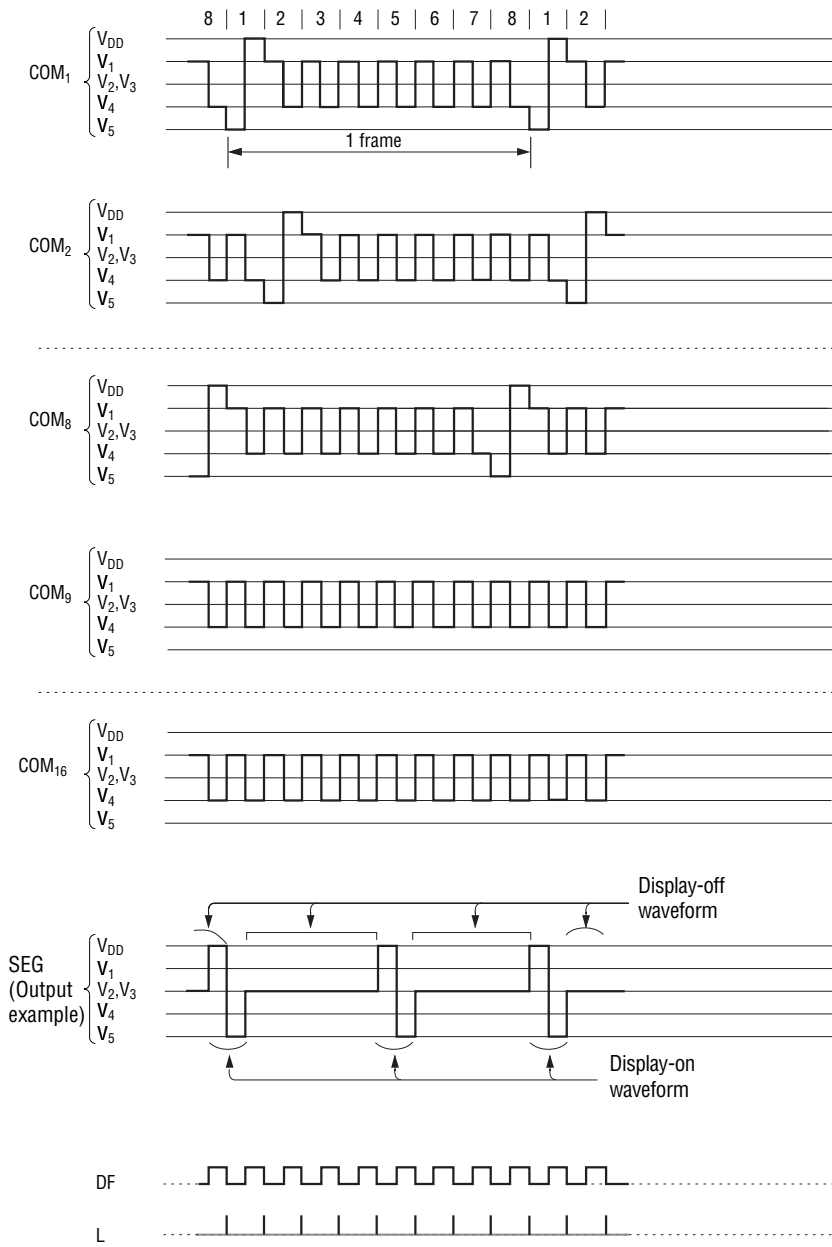


Figure 12. LCD Driving Waveforms (A mode) at 1/8 Duty

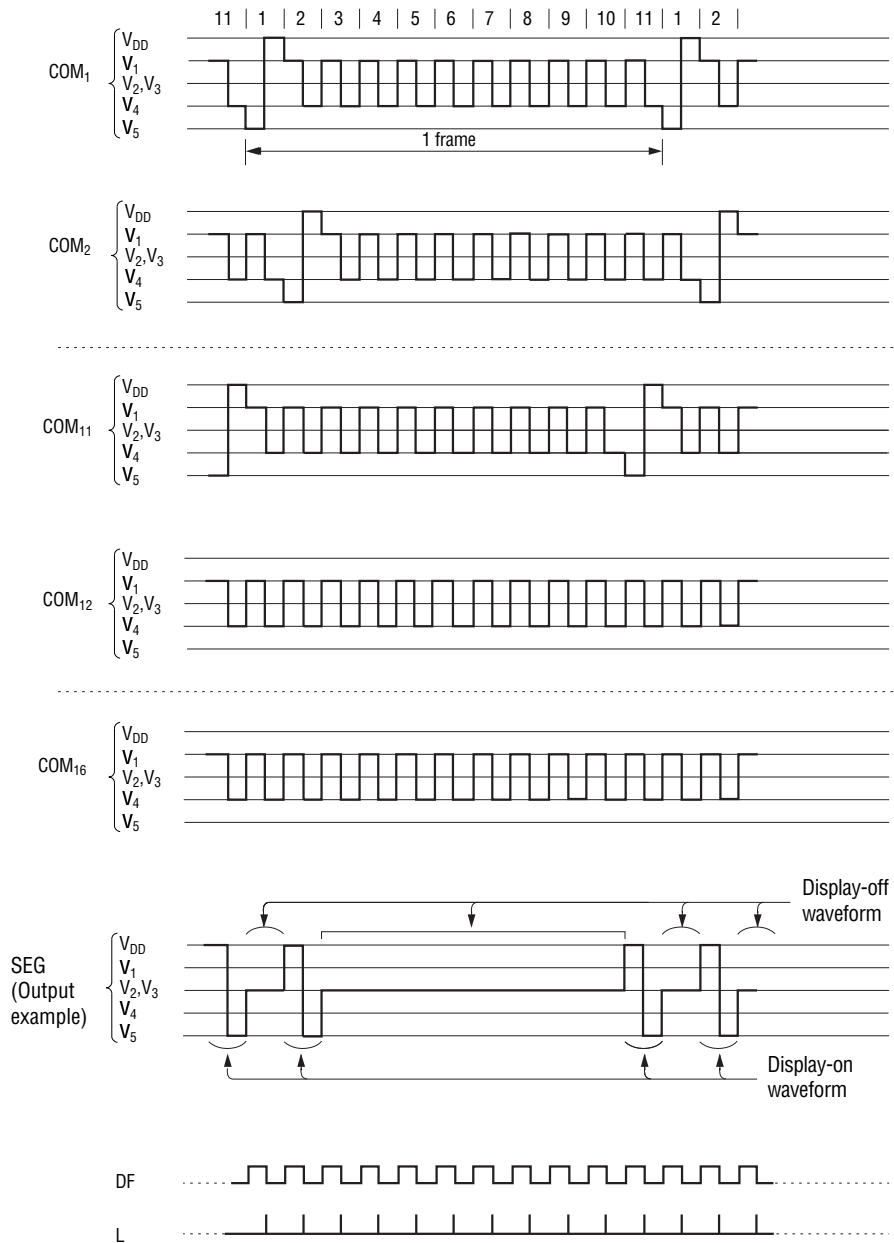


Figure 13. LCD Driving Waveforms (A mode) at 1/11 Duty

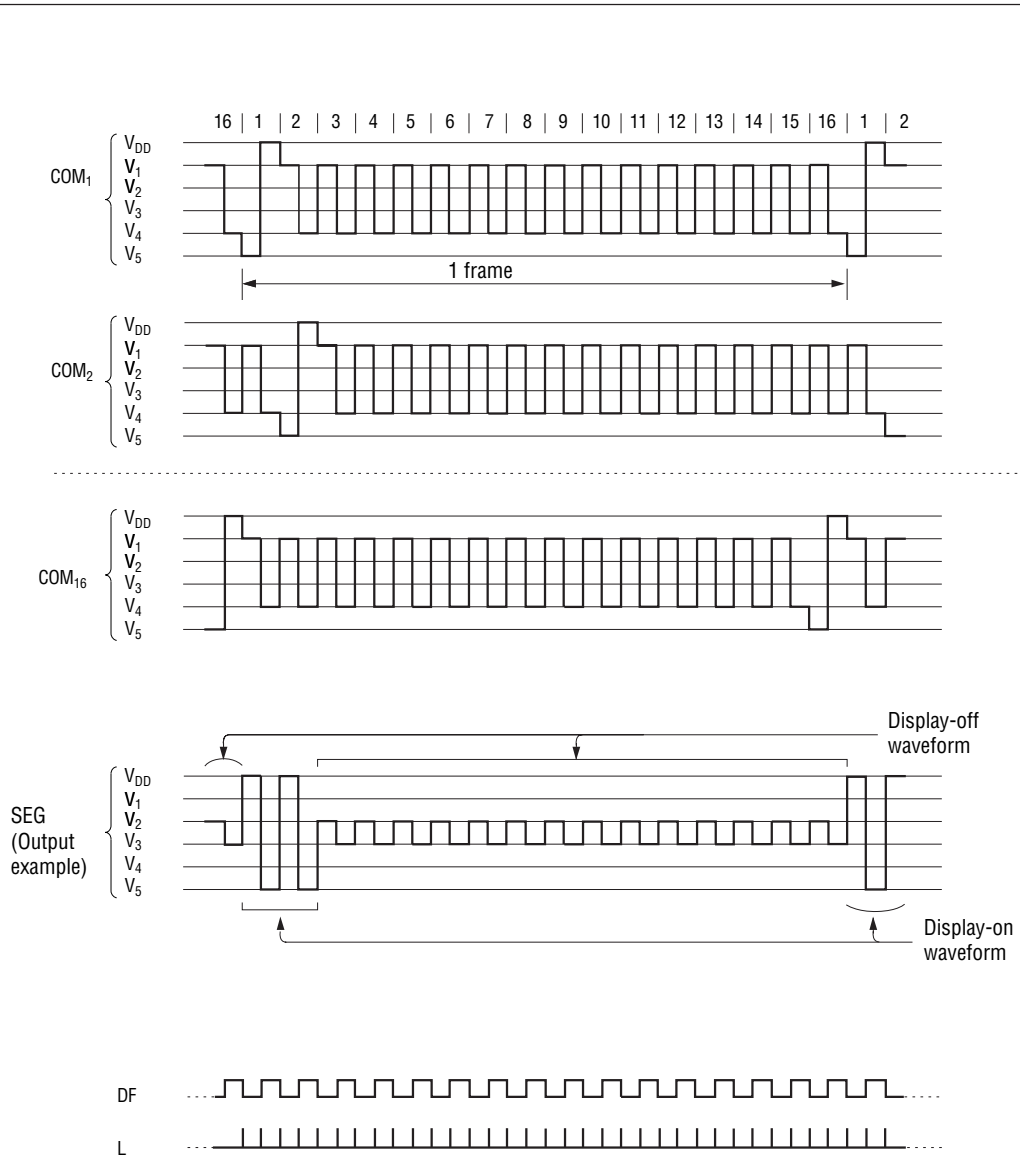


Figure 14. LCD Driving Waveforms (A mode) at 1/16 Duty

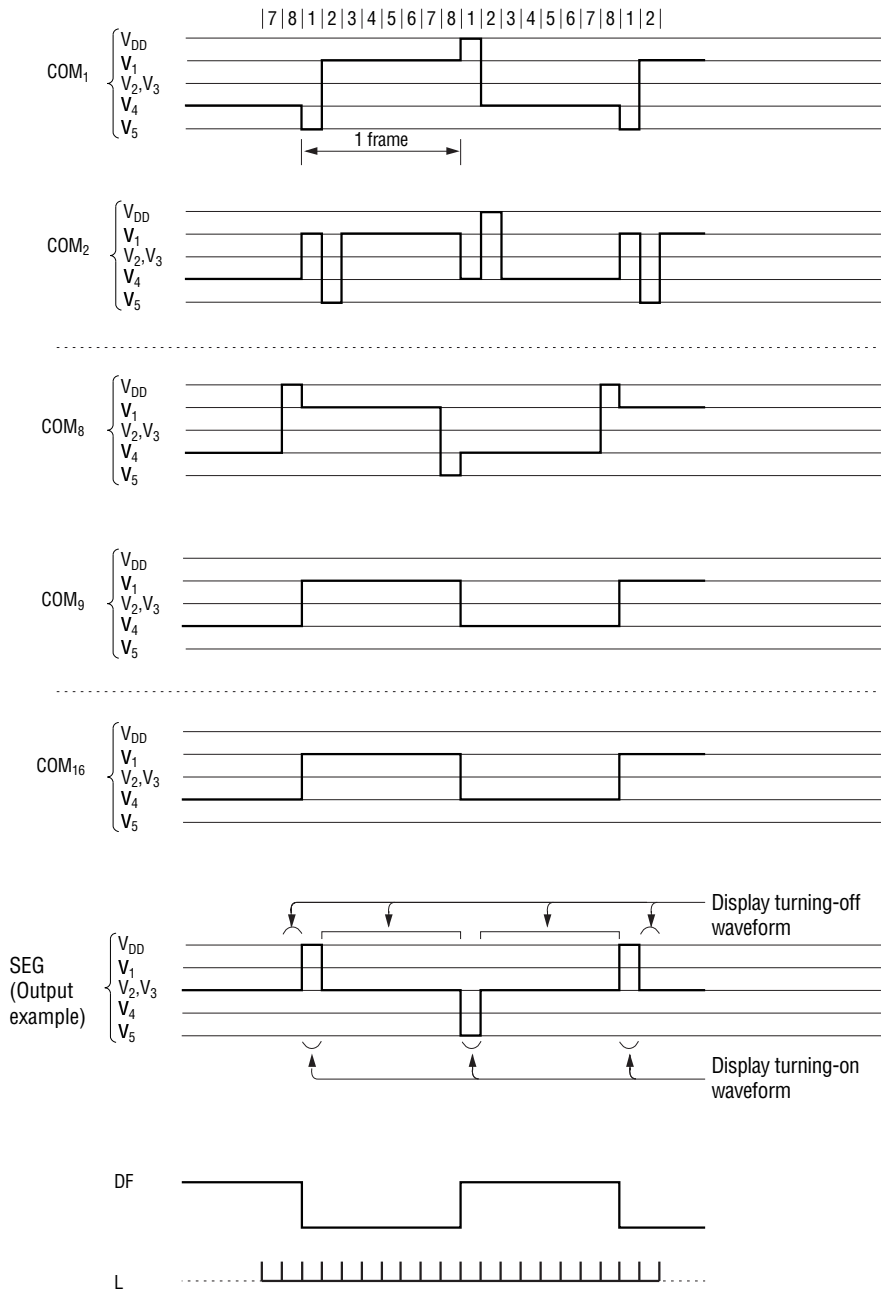


Figure 15. LCD Driving Waveforms (B mode) at 1/8 Duty

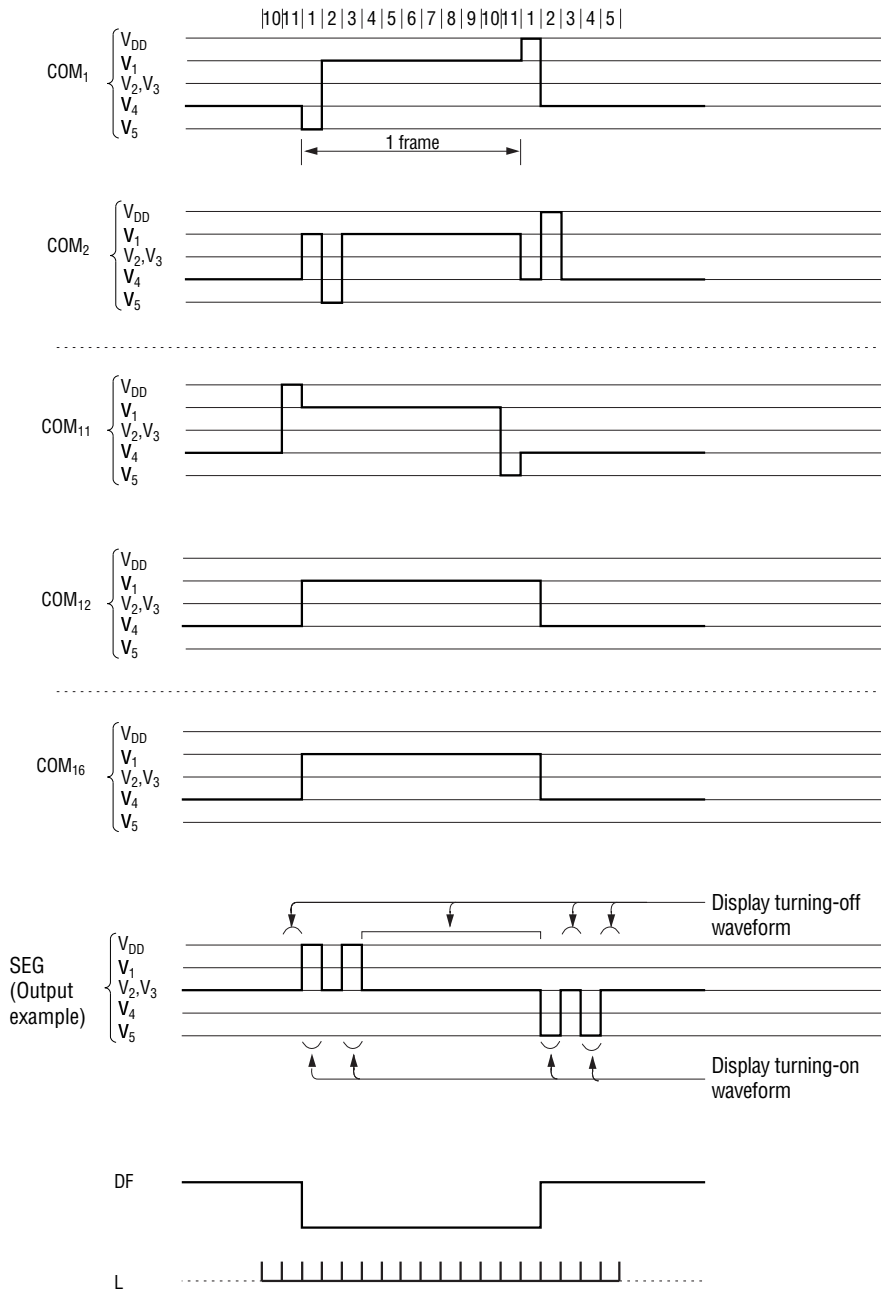


Figure 16. LCD Driving Waveforms (B mode) at 1/11 Duty

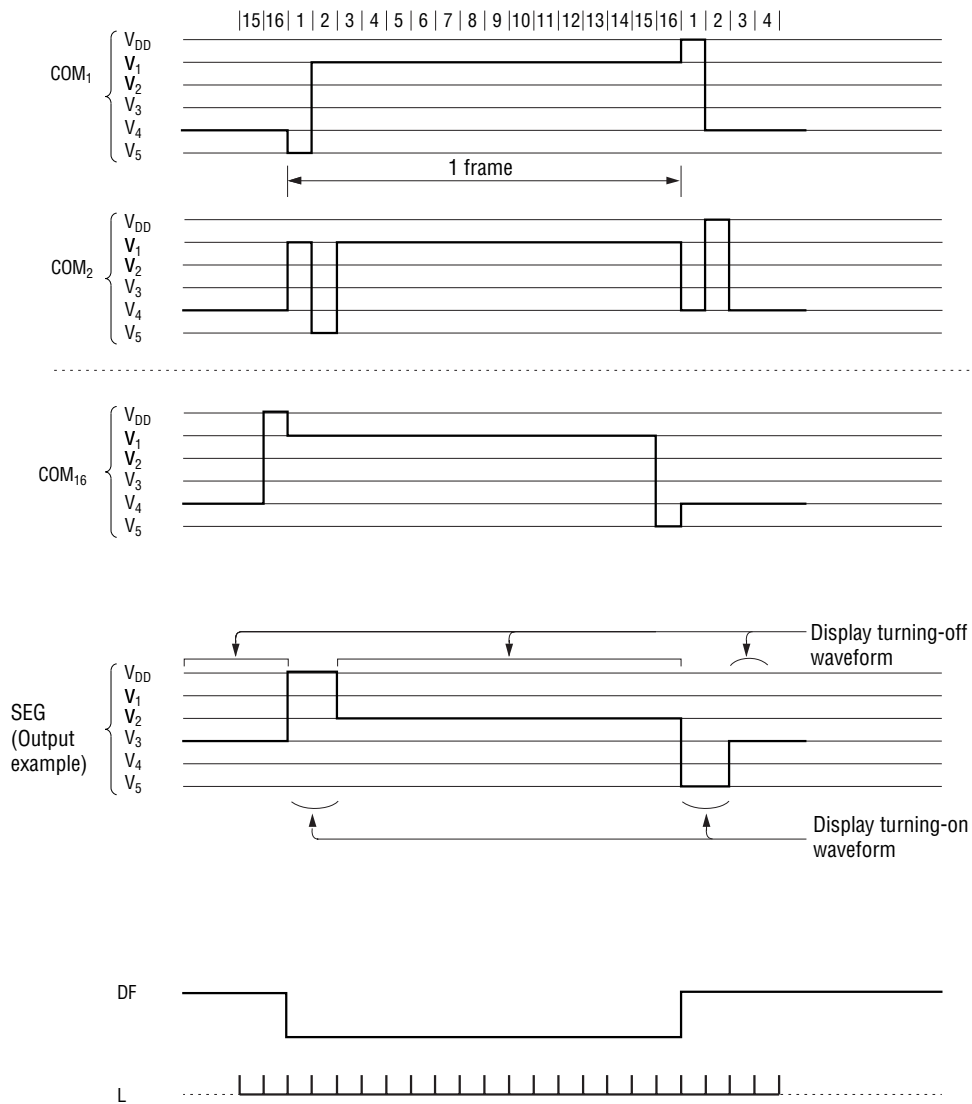


Figure 17. LCD Driving Waveforms (B mode) at 1/16 Duty

Initial Setting of Instruction

(1) When data input/output to and from the CPU is carried out by 8 bits (DB₀ to DB₇):

- ① Turn on the power.
- ② Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
- ③ Set 8B by initial setting of instruction.
- ④ Wait for 4.1 ms or more.
- ⑤ Set 8B by initial setting of instruction.
- ⑥ Wait for 100 μs or more.
- ⑦ Set 8B by initial setting of instruction.
- ⑧ Check the busy flag as No Busy.
- ⑨ Set 8B. Set LCD line number (N) and character font (F).
(After this, the LCD line number and character font cannot be changed.)
- ⑩ Check No Busy.
- ⑪ Clear the display by setting the display mode.
- ⑫ Check No Busy.
- ⑬ Clear the display.
- ⑭ Check No Busy.
- ⑮ Set the shift mode.
- ⑯ Check No Busy.
- ⑰ Initial setting completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
L	L	L	L	H	H	X	X	X	X

X : Don't Care

(2) When data input/output to and from the CPU is carried out by 4 bits (DB₄ to DB₇):

- ① Turn on the power.
- ② Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
- ③ Set 8B by initial setting of instruction.
- ④ Wait for 4.1 ms or more.
- ⑤ Set 8B by initial setting of instruction.
- ⑥ Wait for 100 μs or more.
- ⑦ Set 8B by initial setting of instruction.
- ⑧ Check the busy flag as No Busy.
- ⑨ Set 4B by initial setting of instruction.
- ⑩ Wait for 100 μs or more.
- ⑪ Set 4B, LCD line number (N) and character font (F) by initial setting of instruction.
(After this, the LCD line number and character font cannot be changed.)
- ⑫ Check No Busy.
- ⑬ Clear the display by setting the display mode.
- ⑭ Check No Busy.
- ⑮ Clear the display.
- ⑯ Check No Busy.
- ⑰ Set the shift mode.
- ⑱ Check No Busy.
- ⑲ Initialization completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄
L	L	L	L	H	H

Example of Instruction Code for Step ⑨.

R/W	RS	DB ₇	DB ₆	DB ₅	DB ₄
L	L	L	L	H	L

Example of Instruction Code for Step ⑧.

RS ₁	RS ₀	R/W	DB ₇	DB ₆	DB ₅	DB ₄
H	L	H	BF	Q ₆	Q ₅	Q ₄

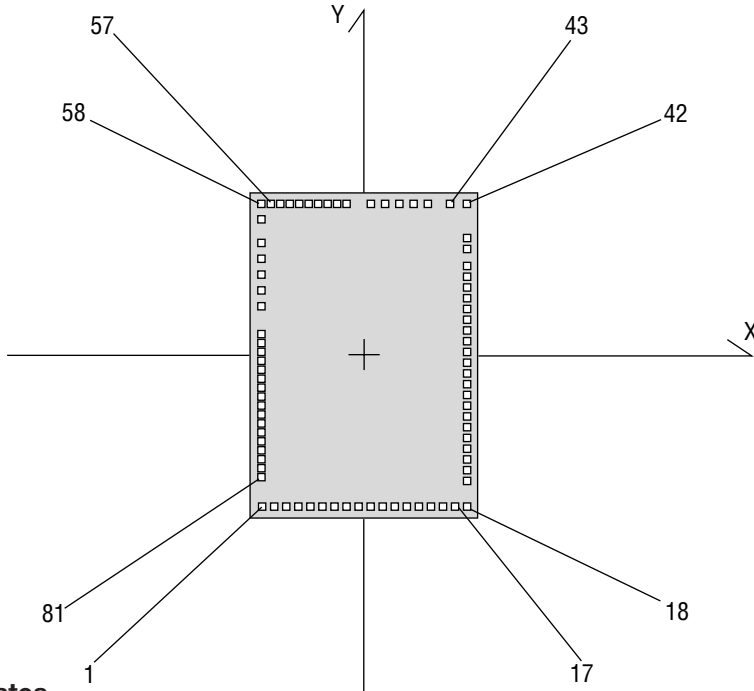
Execute two-step accesses in 4 bits from Step ⑪ to Step ⑱.

PAD CONFIGURATION

Pad Layout

Chip size: 2.94 x 4.32 mm

Passivation film etched hole: 80 x 80 μm



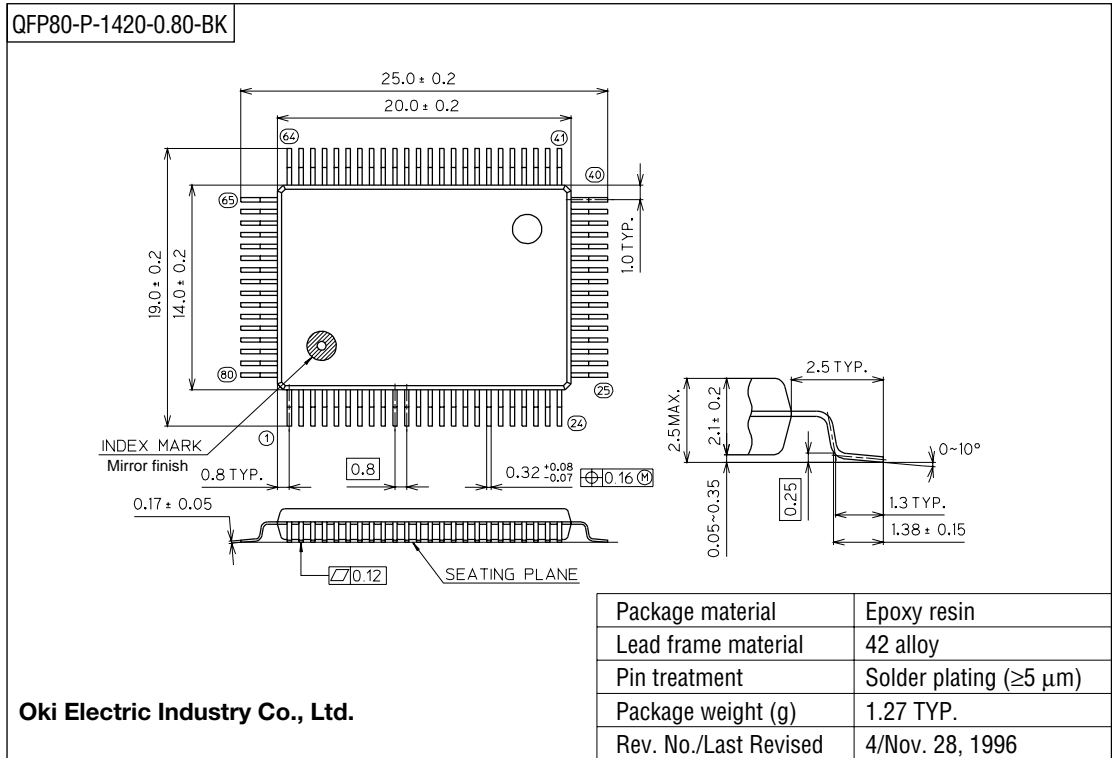
Pad Coordinates

Pad	Pad Name	X(μm)	Y (μm)	Pad	Pad Name	X(μm)	Y (μm)
1	SEG39	-1310	-1955	21	SEG19	1311	-1342
2	SEG38	-1156	-1955	22	SEG18	1311	-1206
3	SEG37	-1002	-1955	23	SEG17	1311	-1070
4	SEG36	-848	-1955	24	SEG16	1311	-934
5	SEG35	-694	-1955	25	SEG15	1311	-797
6	SEG34	-540	-1955	26	SEG14	1311	-661
7	SEG33	-386	-1955	27	SEG13	1311	-525
8	SEG32	-233	-1955	28	SEG12	1311	-389
9	SEG31	-79	-1955	29	SEG11	1311	-253
10	SEG30	75	-1955	30	SEG10	1311	-116
11	SEG29	229	-1955	31	SEG9	1311	20
12	SEG28	383	-1955	32	SEG8	1311	156
13	SEG27	537	-1955	33	SEG7	1311	292
14	SEG26	691	-1955	34	SEG6	1311	428
15	SEG25	845	-1955	35	SEG5	1311	565
16	SEG24	999	-1955	36	SEG4	1311	701
17	SEG23	1153	-1955	37	SEG3	1311	837
18	SEG22	1309	-1955	38	SEG2	1311	973
19	SEG21	1311	-1615	39	SEG1	1311	1109
20	SEG20	1311	-1478	40	TEST	1311	1296

Pad	Pad Name	X(mm)	Y(mm)
41	GND	1311	1426
42	OSC1	1311	1955
43	OSC2	1049	1955
44	V1	738	1955
45	V2	576	1955
46	V3	414	1955
47	V4	252	1955
48	V5	90	1955
49	L	-347	1955
50	CP	-491	1955
51	V _{DD}	-610	1955
52	DF	-710	1955
53	DO	-810	1955
54	RS	-910	1955
55	RW	-1010	1955
56	E	-1111	1955
57	DB0	-1211	1955
58	DB1	-1311	1955
59	DB2	-1311	1783
60	DB3	-1311	1369
61	DB4	-1311	1184
62	DB5	-1311	1000
63	DB6	-1311	816
64	DB7	-1311	632
65	COM1	-1311	148
66	COM2	-1311	48
67	COM3	-1311	-52
68	COM4	-1311	-152
69	COM5	-1311	-253
70	COM6	-1311	-353
71	COM7	-1311	-453
72	COM8	-1311	-553
73	COM9	-1311	-653
74	COM10	-1311	-754
75	COM11	-1311	-854
76	COM12	-1311	-954
77	COM13	-1311	-1054
78	COM14	-1311	-1154
79	COM15	-1311	-1255
80	COM16	-1311	-1355
81	SEG40	-1311	-1455

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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