# LMZ14202 采用带引线 SMT-TO 封装的 SIMPLE SWITCHER® 6V 至 42V、2A 电源模块

## 1 特性

- 集成隔离电感
- 简单的印刷电路板 (PCB) 布局
- 使用外部软启动和精密使能实现灵活启动排序
- 针对浪涌电流以及输入欠压锁定 (UVLO) 和输出短路等故障提供保护
- 结温范围：–40°C 至 125°C
- 用于简单装配和制造的单个外露垫和标准引脚分配
- 针对现场可编程门阵列 (FPGA) 和特定用途集成电路 (ASIC) 供电的快速瞬态响应
- 低输出电压纹波
- 引脚到引脚兼容的系列器件：
  - LMZ14203/2/1（最大值 42V；3A、2A 和 1A）
  - LMZ12003/2/1（最大值 20V；3A、2A 和 1A）
- 针对 WEBENCH® 电源设计工具完全启用
- 电气规范
  - 总输出功率最高可达 12W
  - 输出电流高达 2A
  - 输入电压范围：6V 至 42V
  - 输出电压范围：0.8V 至 6V
  - 效率高达 90%
- 性能优势
  - 在较高环境温度下运行不会降低耐热额定值
  - 高效率有效减少了系统产生的热量
  - 通过低辐射 (EMI) 测试标准 EN55022 B 类
  - 外部组件数较少

## 2 应用

- 12V 和 24V 输入电源轨的负载点转换
- 时间要求严格的项目
- 空间受限类和高散热应用的易用型 7 引脚封装 PFM 7 引脚封装
- 负输出电压应用（请见 AN-2027SNVA425）

## 3 说明

LMZ14202 SIMPLE SWITCHER® 电源模块是一款易用型降压 DC-DC 解决方案，能够驱动高达 2A 的负载并且拥有出色的电源转换效率、线路和负载调节性能以及输出精度。 LMZ14202 采用创新型封装，可提高散热性能并支持手工或机器焊接。

LMZ14202 的输入电压轨范围为 6V 和 42V，提供的高精度可调节输出电压低至 0.8V。LMZ14202 仅需三个外部电阻和四个外部电容即可完善电源解决方案。LMZ14202 的设计可靠而稳健，并且具有以下保护特性：热关断、输入欠压锁定、输出过压保护、短路保护、输出限流以及预偏置输出的启动功能。 单个电阻最高可将开关频率调节至 1MHz。

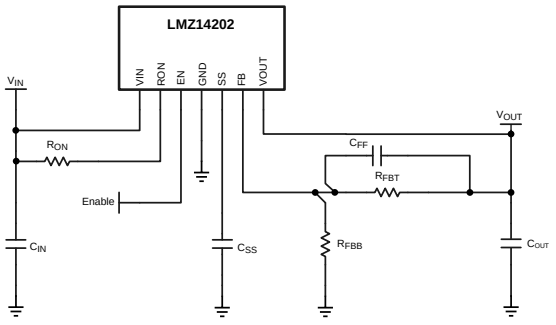
器件信息(1)(2)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| LMZ14202 | TO-PMOD (7) | 10.16mm × 9.85mm |

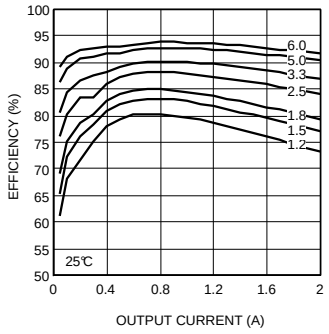
(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。

(2) 峰值回流温度等于 245°C。 更多详细信息，请参见 SNAA214。

简化应用电路原理图




25°C、输入电压为 12V 时的效率



# 目录



## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision I (August 2015) to Revision J** — **Page**

- Added this new bullet to the Power Module SMT Guidelines section ... 23

**Changes from Revision H (June 2015) to Revision I** — **Page**

- 已更改 文档标题 ... 1

**Changes from Revision G (March 2013) to Revision H** — **Page**

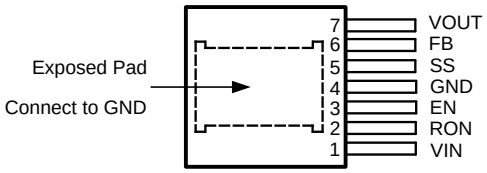
- 已添加 *引脚配置和功能*部分，*处理额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已删除易用型 7 引脚封装 PFM 7 引脚封装图 ... 1

**Changes from Revision F (October 2012) to Revision G** — **Page**

- Changed layout of National Data Sheet to TI format ... 23
- Added *Power Module SMT Guidelines* section ... 23

# 5 Pin Configuration and Functions

**NDW Package**
**7-Pin TO-PMOD**
**Top View**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 3 | Analog | Enable. Input to the precision enable comparator. Rising threshold is 1.18 V nominal, 90 mV hysteresis nominal. Maximum recommended input level is 6.5 V. |
| FB | 6 | Analog | Feedback. nternally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connected the feedback resistor divider between the output and ground to set the output voltage. |
| GND | 4 | Ground | Ground. Reference point for all stated voltages. Must be externally connected to thermal pad. |
| RON | 2 | Analog | ON-time resistor. An external resistor between this pin and the VIN pin sets the ON-time of the application. Typical values range from 25 kΩ to 124 kΩ. |
| SS | 5 | Analog | Soft-start. An internal 8-µA current source charges an external capacitor to produce the soft-start function. This node is discharged at 200 µA during disable, over-current, thermal shutdown and internal UVLO conditions. |
| VIN | 1 | Power | Supply input. Nominal operating range is 6 V to 42 V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad. |
| VOUT | 7 | Power | Output voltage. Output from the internal inductor. Connect the output capacitor between this pin and exposed pad. |
| Thermal pad | | Ground | Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | VIN, RON to GND | –0.3 | 43.5 | V |
| | EN, FB, SS to GND | –0.3 | 7 | V |
| $T_J$ | Junction temperature | | 150 | °C |
| | Peak reflow case temperature (30 s) | | 245 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, refer to the following document: www.ti.com/lit/snoa549c

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 6 | 42 | V |
| EN | Enable voltage | 0 | 6.5 | V |
| $T_J$ | Junction temperature | −40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | | LMZ14202 NDW (TO-PMOD) 7 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 4-layer JEDEC Printed circuit board, 100 vias, No air flow | 19.3 | °C/W |
| | | 2-layer JEDEC Printed circuit board, No air flow | 21.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | No air flow | 1.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

Limits in standard type are for $T_J$ = 25°C only; limits in boldface type apply over the junction temperature ($T_J$) range of –40°C to +125°C. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{VIN}$ = 24 V, $V_{VOUT}$ = 3.3 V

| PARAMETER | | TEST CONDITIONS | | MIN(1) | TYP(2) | MAX(1) | UNIT |
|---|---|---|---|---|---|---|---|
| **ENABLE CONTROL**(3) | | | | | | | |
| $V_{EN}$ | EN threshold trip point | $V_{EN}$ rising | | | 1.18 | | V |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 1.1 | | 1.25 | |
| $V_{EN-HYS}$ | EN threshold hysteresis | $V_{EN}$ falling | | | 90 | | mV |
| **SOFT-START** | | | | | | | |
| $I_{SS}$ | SS source current | $V_{SS}$ = 0 V | | | 8 | | µA |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 5 | | 11 | |
| $I_{SS-DIS}$ | SS discharge current | | | | -200 | | µA |
| **CURRENT LIMIT** | | | | | | | |
| $I_{CL}$ | Current limit threshold | d.c. average | | | 2.6 | | A |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 2.3 | | 3.65 | |
| **ON/OFF TIMER** | | | | | | | |
| $t_{ON-MIN}$ | ON timer minimum pulse width | | | | 150 | | ns |
| $t_{OFF}$ | OFF timer pulse width | | | | 260 | | ns |
| **REGULATION AND OVERVOLTAGE COMPARATOR** | | | | | | | |
| $V_{FB}$ | In-regulation feedback voltage | $V_{SS}$ > 0.8 V, $I_O$ = 2 A | | | 0.795 | | V |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 0.775 | | 0.815 | |
| | | $V_{SS}$ >+ 0.8 V, $I_O$ = 10 mA | | 0.786 | 0.802 | 0.818 | V |
| $V_{FB-OV}$ | Feedback over-voltage protection threshold | | | | 0.92 | | V |
| $I_{FB}$ | Feedback input bias current | | | | 5 | | nA |

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See *AN-2024 LMZ1420x / LMZ1200x Evaluation Board* (SNVA422) and layout for information on device under test.

## Electrical Characteristics (continued)

Limits in standard type are for $T_J$ = 25°C only; limits in boldface type apply over the junction temperature ($T_J$) range of –40°C to +125°C. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{VIN}$ = 24 V, $V_{VOUT}$ = 3.3 V

| PARAMETER | | TEST CONDITIONS | MIN(1) | TYP(2) | MAX(1) | UNIT |
|---|---|---|---|---|---|---|
| $I_Q$ | Non-switching input current | $V_{FB}$ = 0.86 V | | 1 | | mA |
| $I_{SD}$ | Shutdown quiescent current | $V_{EN}$ = 0 V | | 25 | | µA |
| **THERMAL CHARACTERISTICS** | | | | | | |
| $T_{SD}$ | Thermal shutdown | Rising | | 165 | | °C |
| $T_{SD-HYST}$ | Thermal shutdown hysteresis | Falling | | 15 | | °C |
| **PERFORMANCE PARAMETERS** | | | | | | |
| $\Delta V_O$ | Output voltage ripple | | | 8 | | $mV_{P-P}$ |
| $\Delta V_O/\Delta V_{IN}$ | Line regulation | 12 V ≤ $V_{VIN}$ ≤ 42 V, $I_O$ = 2 A | | 0.01% | | |
| $\Delta V_O/I_{OUT}$ | Load regulation | $V_{VIN}$ = 24 V | | 1.5 | | mV/A |
| η | Efficiency | $V_{VIN}$ = 24 V, $V_O$ = 3.3 V, $I_O$ = 1 A | | 86% | | |
| | | $V_{VIN}$ = 24 V, $V_O$ = 3.3 V, $I_O$ = 2 A | | 85% | | |

## 6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 24 V; $C_{IN}$ = 10 µF, X7R ceramic; $C_O$ = 100 µF X7R ceramic; $T_A$ = 25°C.

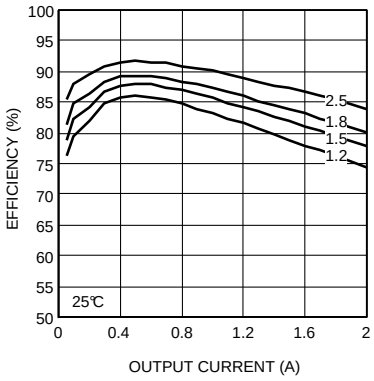



**Figure 1. Efficiency 6-V Input**

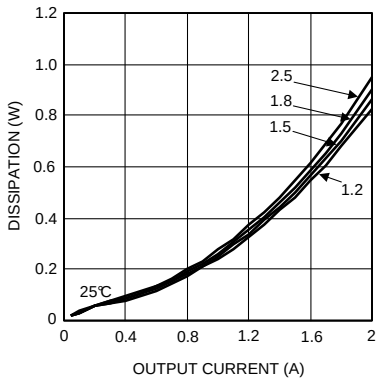



**Figure 2. Dissipation 6-V Input**

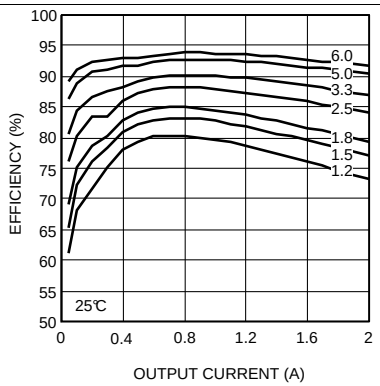



**Figure 3. Efficiency 12-V Input**

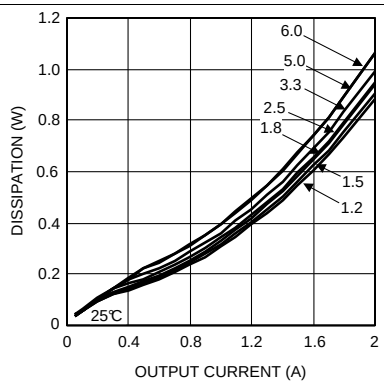



**Figure 4. Dissipation 12-V Input**

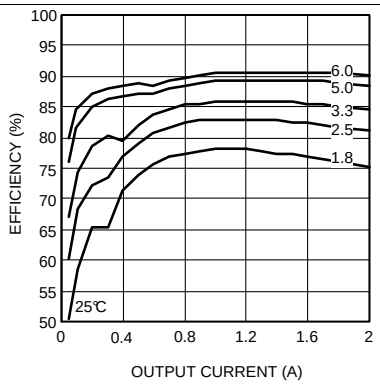



**Figure 5. Efficiency 24-V Input**

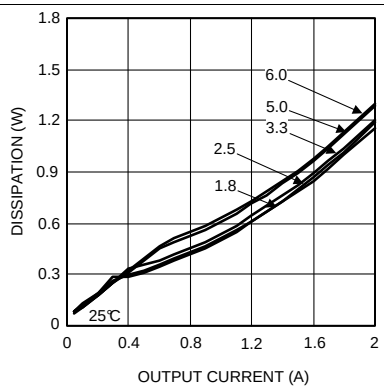



**Figure 6. Dissipation 24-V Input**

## Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 24 V; $C_{IN}$ = 10 µF, X7R ceramic; $C_O$ = 100 µF X7R ceramic; $T_A$ = 25°C.

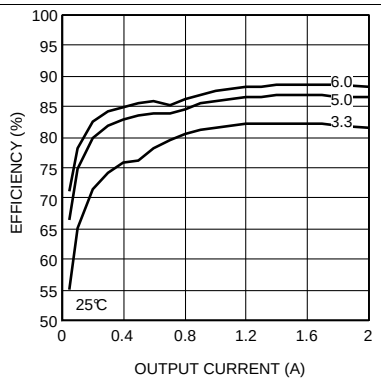



**Figure 7. Efficiency 36-V Input at 25°C**

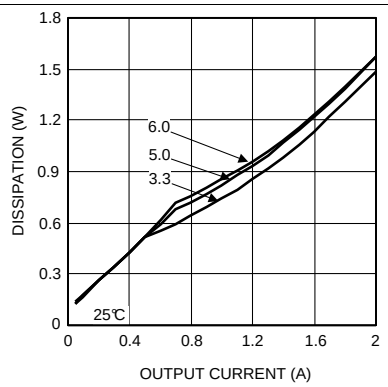



**Figure 8. Dissipation 36-V Input**

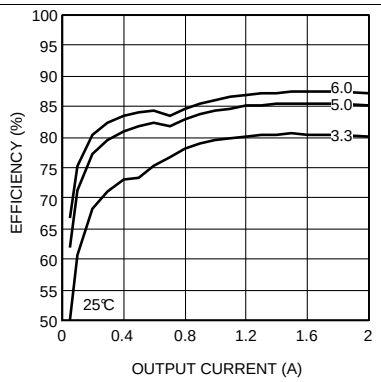



**Figure 9. Efficiency 42-V Input**

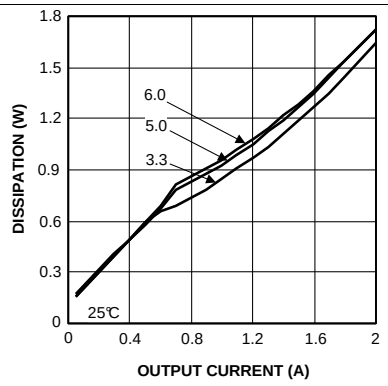



**Figure 10. Dissipation 42-V Input**

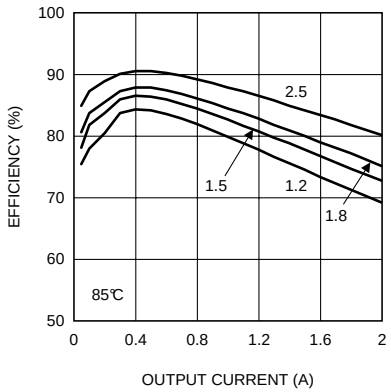



**Figure 11. Efficiency 6-V Input, $T_A$ = 85°C**

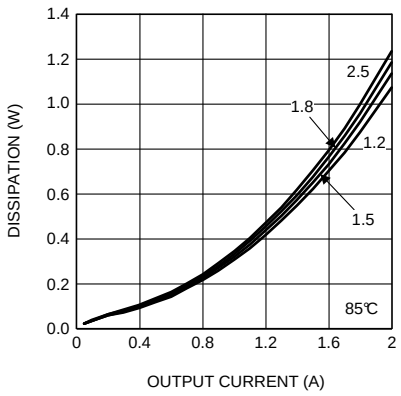



**Figure 12. Dissipation 6-V Input, $T_A$ = 85°C**

## Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 24 V; $C_{IN}$ = 10 µF, X7R ceramic; $C_O$ = 100 µF X7R ceramic; $T_A$ = 25°C.

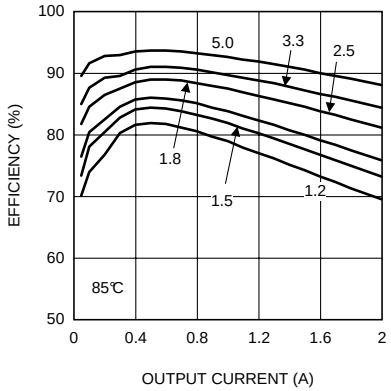



**Figure 13. Efficiency 8 V Input, $T_A$ = 85°C**

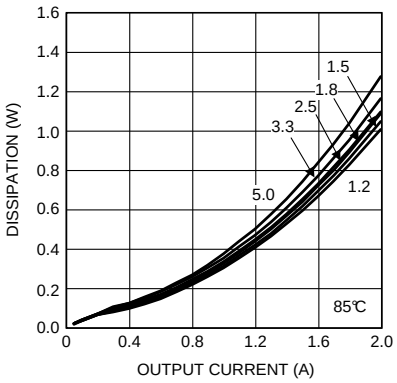



**Figure 14. Dissipation 8-V Input, $T_A$ = 85°C**

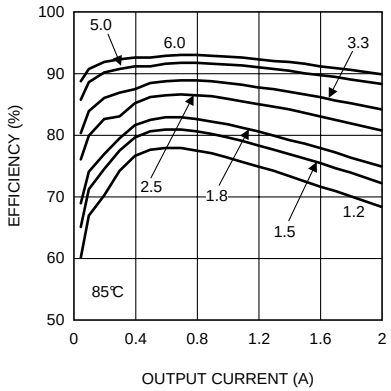



**Figure 15. Efficiency 12-V Input, $T_A$ = 85°C**

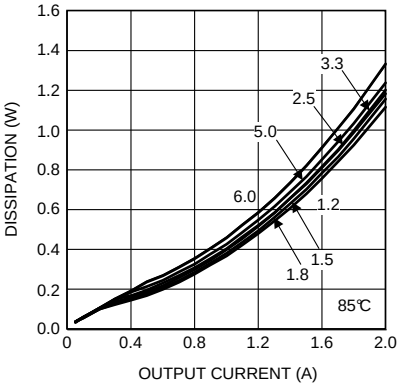



**Figure 16. Dissipation 12-V Input, $T_A$ = 85°C**

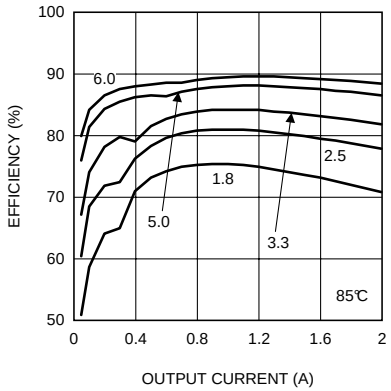



**Figure 17. Efficiency 24-V Input, $T_A$ = 85°C**

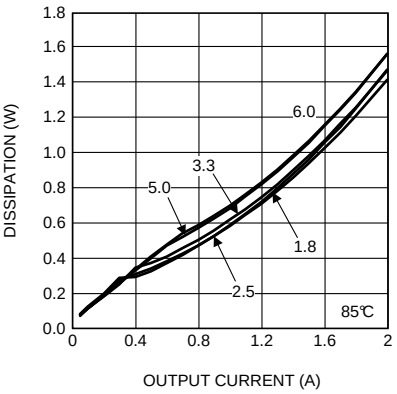



**Figure 18. Dissipation 24-V Input, $T_A$ = 85°C**

## Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 24 V; $C_{IN}$ = 10 µF, X7R ceramic; $C_O$ = 100 µF X7R ceramic; $T_A$ = 25°C.

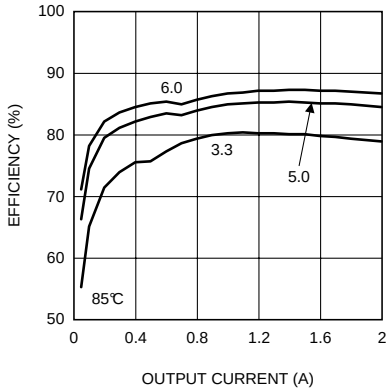



**Figure 19. Efficiency 36-V Input, $T_A$ = 85°C**

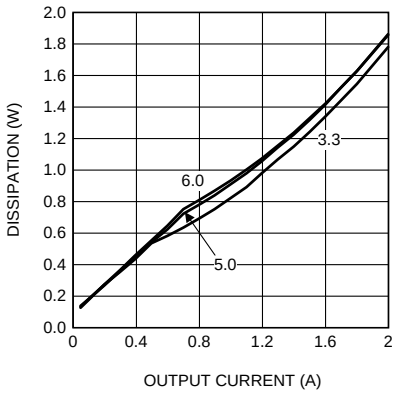



**Figure 20. Dissipation 36-V Input, $T_A$ = 85°C**

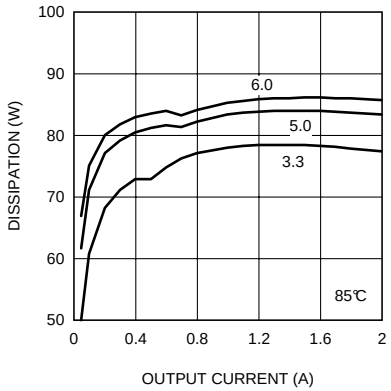



**Figure 21. Efficiency 42-V Input, $T_A$ = 85°C**

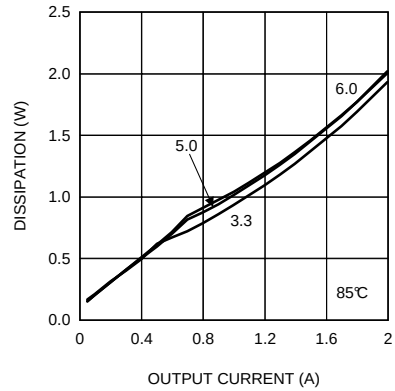



**Figure 22. Dissipation 42-V Input, $T_A$ = 85°C**

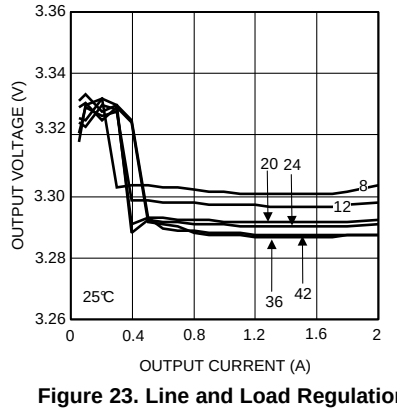



**Figure 23. Line and Load Regulation**

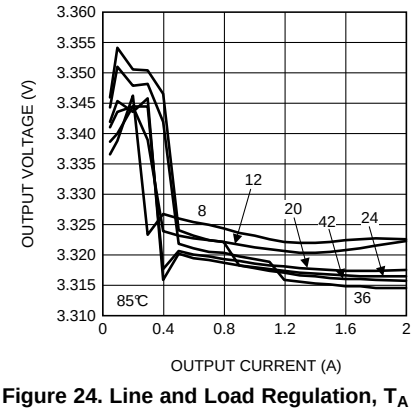



**Figure 24. Line and Load Regulation, $T_A$ = 85°C**

## Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 24 V; $C_{IN}$ = 10 µF, X7R ceramic; $C_O$ = 100 µF X7R ceramic; $T_A$ = 25°C.

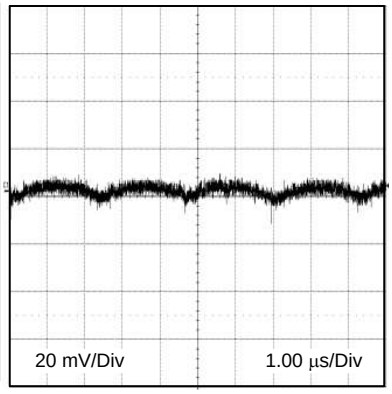



**Figure 25. Output Ripple**
**$V_{IN}$ = 24 V, $V_O$ = 3.3 V, 2 A, BW = 200 MHz**

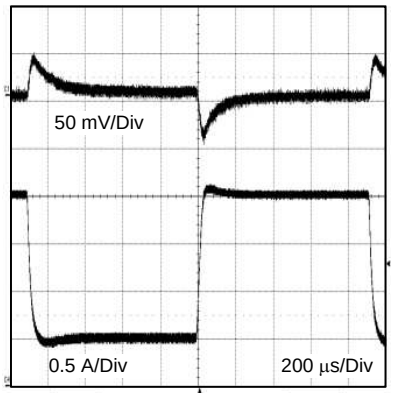



**Figure 26. Transient Response**
**$V_{IN}$ = 24 V, $V_O$ = 3.3 V, 0.6-A to 2-A Step**

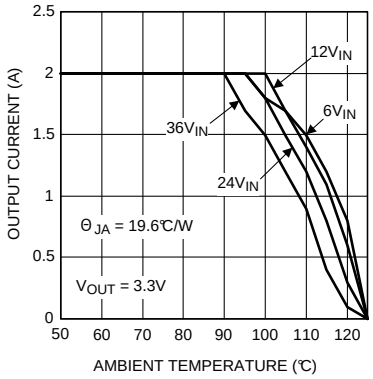



**Figure 27. Thermal Derating, $V_{OUT}$ = 3.3 V**

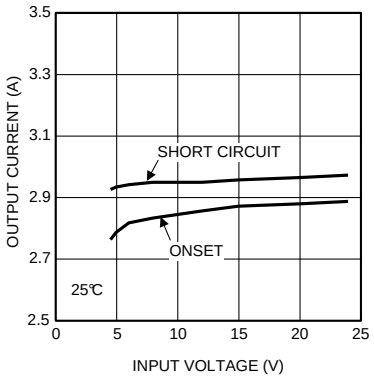



**Figure 28. Current Limit, $V_{OUT}$ = 3.3 V**

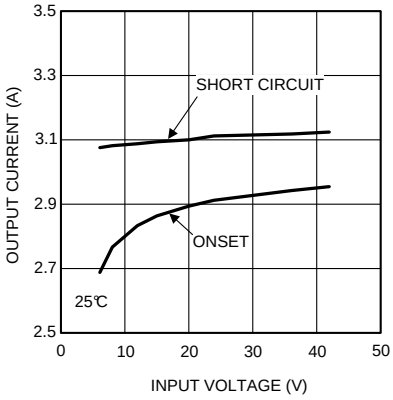



**Figure 29. Current Limit, $V_{OUT}$ = 3.3 V,**

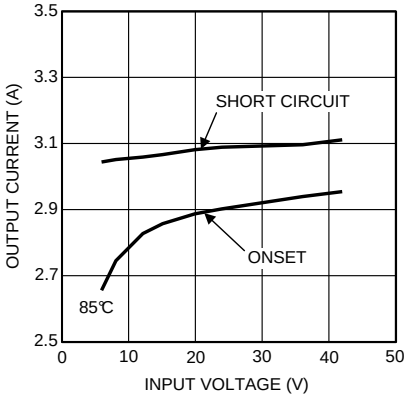


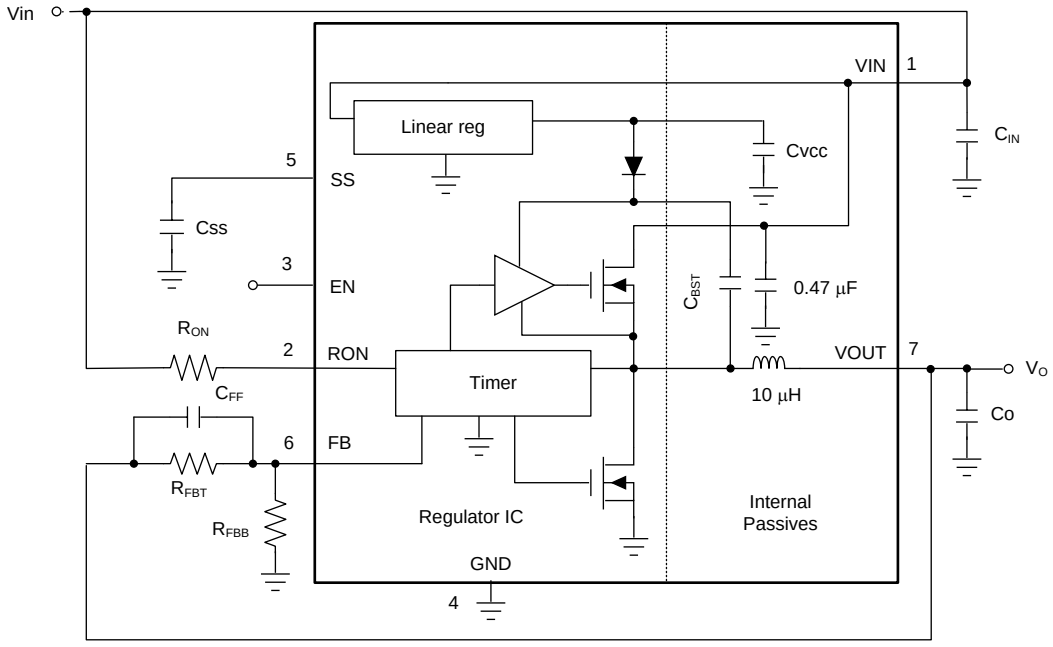

**Figure 30. Current Limit, $V_{OUT}$ = 3.3 V, $T_A$ = 85°C**

# 7 Detailed Description

## 7.1 Overview

The LMZ14202 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Constant On-Time Control (COT) Circuit Overview

Constant on-time control (COT) control is based on a comparator and an ON-time one-shot, with the output voltage feedback compared with an internal 0.8-V reference. If the feedback voltage is below the reference, the main MOSFET is turned on for a fixed ON-time determined by a programming resistor $R_{DS(on)}$ . $R_{DS(on)}$ is connected to $V_{IN}$ such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the main MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

### 7.3.2 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times are inhibited until the condition clears. Additionally, the synchronous MOSFET remains on until the inductor current falls to zero.

## Feature Description (continued)

### 7.3.3 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the *Functional Block Diagram*, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 2.6 A (typical) the current limit comparator disables the start of the next ON-time period. The next switching cycle occurs only if the FB input is less than 0.8 V and the inductor current has decreased below 2.6 A. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. While the inductor current exceeds 2.6 A, further ON-time intervals for the top MOSFET do not occur. Switching frequency is lower during current limit due to the longer OFF-time.

**NOTE**

Current limit is dependent on both duty cycle and temperature as illustrated in the graphs in *Typical Characteristics* section.

### 7.3.4 Thermal Protection

Do not allow the junction temperature of the LMZ14202 device to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing $V_O$ to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature returns to below 145 °C (typical hysteresis = 20 °C) the SS pin is released, $V_O$ rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require application derating at elevated temperatures.

### 7.3.5 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

### 7.3.6 Prebiased Start-Up

The LMZ14202 starts up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. Figure 31 is a scope capture that shows proper behavior during this event.

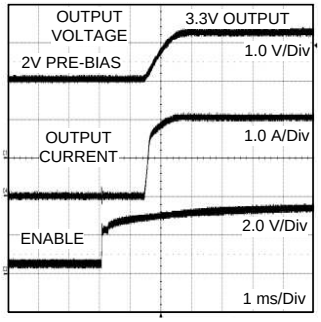



**Figure 31. Prebiased Start-Up**

## 7.4 Device Functional Modes

### 7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light-load, the regulator operates in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it operates in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

## 8.1 Application Information

The LMZ14202 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMZ14202. Alternately, the WEBENCH software may be used to generate complete designs.

WEBENCH software uses an iterative design procedure and accesses comprehensive databases of components. For more details, go to www.ti.com/WEBENCH.

## 8.2 Typical Application

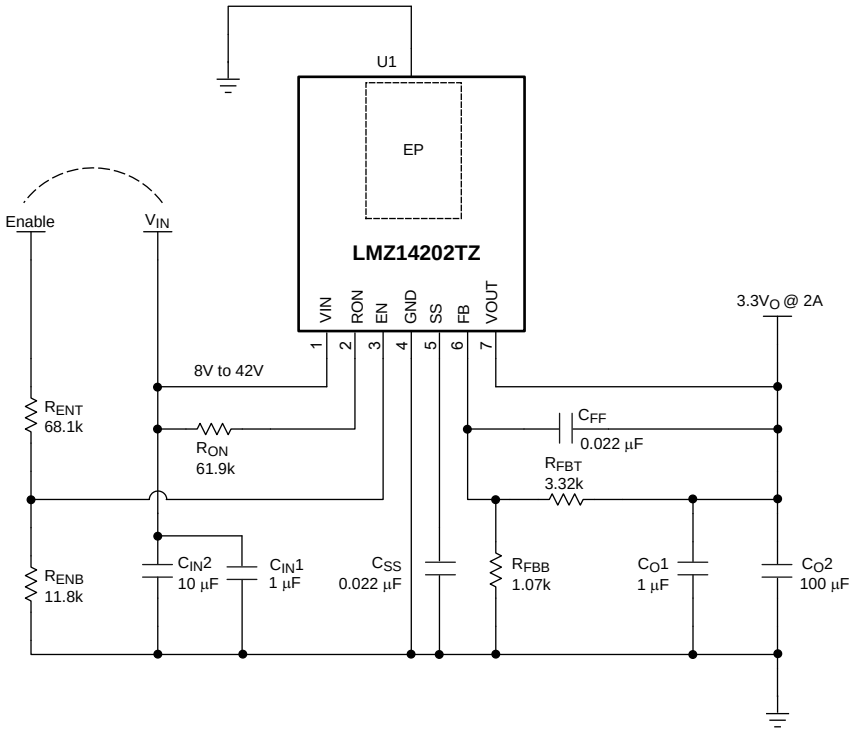



**Figure 32. Evaluation Board Schematic Diagram**

### 8.2.1 Design Requirements

For this example the following application parameters exist.

- $V_{IN}$ range: up to 42 V
- $V_{OUT}$ = 0.8 V to 5 V
- $I_{OUT}$ = 2 A

Refer to Table 2 for more information.

**Table 1. Component Value Combinations**

| VOUT (V) | $R_{FBT}$ (kΩ) | $R_{FBB}$ (kΩ) | $R_{DS(on)}$ (kΩ) | VIN (V) | |
|---|---|---|---|---|---|
| | | | | MIN | MAX |
| 5 | 5.62 | 1.07 | 100 | 7.5 | 42 |
| 3.3 | 3.32 | | 61.9 | 6 | 42 |
| 2.5 | 2.26 | | 47.5 | | 30 |
| 1.8 | 1.87 | 1.5 | 32.4 | | 25 |
| 1.5 | 1 | 1.13 | 28 | | 21 |
| 1.2 | 4.22 | 8.45 | 22.6 | | 19 |
| 0.8 | 0 | 39.2 | 24.9 | | 18 |

**Table 2. List of Materials**

| REF DES | DESCRIPTION | SIZE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| U1 | SIMPLE SWITCHER | PFM-7 | Texas Instruments | LMZ14202TZ |
| $C_{IN1}$ | 1 µF, 50 V, X7R | 1206 | Taiyo Yuden | UMK316B7105KL-T |
| $C_{IN2}$ | 10 µF, 50 V, X7R | 1210 | Taiyo Yuden | UMK325BJ106MM-T |
| $C_{O1}$ | 1 µF, 50 V, X7R | 1206 | Taiyo Yuden | UMK316B7105KL-T |
| $C_{O2}$ | 100 µF, 6.3 V, X7R | 1210 | Taiyo Yuden | JMK325BJ107MM-T |
| $R_{FBT}$ | 3.32 kΩ | 0603 | Vishay Dale | CRCW06033K32FKEA |
| $R_{FBB}$ | 1.07 kΩ | 0603 | Vishay Dale | CRCW06031K07FKEA |
| $R_{DS(on)}$ | 61.9 kΩ | 0603 | Vishay Dale | CRCW060361k9FKEA |
| $R_{ENT}$ | 68.1 kΩ | 0603 | Vishay Dale | CRCW060368k1FKEA |
| $R_{ENB}$ | 11.8 kΩ | 0603 | Vishay Dale | CRCW060311k8FKEA |
| $C_{FF}$ | 22 nF, ±10%, X7R, 16 V | 0603 | TDK | C1608X7R1H223K |
| $C_{SS}$ | 22 nF, ±10%, X7R, 16 V | 0603 | TDK | C1608X7R1H223K |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Design Steps for the LMZ14202 Application*

The LMZ14202 is fully supported by WEBENCH and offers the following: Component selection, electrical and thermal simulations as well as the build-it board for a reduction in design time. The following list of steps can be used to manually design the LMZ14202 application.

1. Select minimum operating $V_{IN}$ with enable divider resistors
2. Program $V_O$ with divider resistor selection
3. Program turnon time with soft-start capacitor selection
4. Select $C_O$
5. Select $C_{IN}$
6. Set operating frequency with $R_{DS(on)}$
7. Determine module dissipation
8. Carefully consider thermal performance required when designing the PCB layout

##### 8.2.2.1.1 Enable Divider, $R_{ENT}$ and $R_{ENB}$ Selection

The enable input provides a precise, 1.18-V band-gap rising threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as $V_{IN}$. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of this resistive divider is to allow the designer to choose an input voltage below which the circuit becomes disabled. This implements the feature of programmable undervoltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation must be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14202 output rail. Choose the two resistors based on Equation 1.

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.18\ V) - 1 \quad (1)$$

The LMZ14202 demonstration and evaluation boards use 11.8 kΩ for $R_{ENB}$ and 68.1 kΩ for $R_{ENT}$ resulting in a rising UVLO of 8 V. This divider presents 6.25 V to the EN input when the divider input is raised to 42 V.

The EN pin is internally pulled up to VIN and can be left floating for always-on operation.

#### 8.2.2.1.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between $V_O$ and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The main MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles does not occur.

The regulated output voltage determined by the external divider resistors $R_{FBT}$ and $R_{FBB}$ is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8\ V) - 1 \quad (3)$$

Choose these resistors from values between 1 kΩ and 10 kΩ.

For $V_O$ = 0.8 V the FB pin can be connected to the output directly so long as an output preload resistor remains that draws more than 20 µA. Converter operation requires this minimum load to create a small inductor ripple current and maintain proper regulation when no load is present.

A feed-forward capacitor is placed in parallel with $R_{FBT}$ to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for $R_{FBT}$ , $R_{FBB}$ , $C_{FF}$ and $R_{DS(on)}$ is included in the applications schematic.

#### 8.2.2.1.3 Soft-Start Capacitor Selection

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8 µA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / I_{SS} = 0.8\ V \times C_{SS} / 8\ \mu A \quad (4)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (5)$$

Use of a 0.022-µF capacitor results in 2.2-ms soft-start duration which is recommended as a minimum value.

As the soft-start input exceeds 0.8 V the output of the power stage comes into regulation. The soft-start capacitor continues charging until it reaches approximately 3.8 V on the SS pin. Voltage levels between 0.8 V and 3.8 V have no effect on other circuit operation. The following conditions reset the soft-start capacitor by discharging the SS input to ground with an internal 200-µA current sink.

- The enable input being pulled low
- Thermal shutdown condition
- Over-current fault
- Internal $V_{CC}$ UVLO (approximately 4-V input to $V_{IN}$)

#### 8.2.2.1.4 $C_O$ Selection

None of the required $C_O$ output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst-case minimum ripple current rating of 0.5 × $I_{LR(P-P)}$, as calculated in Equation 17 below. Beyond the worst-case minimum, additional capacitance reduces output ripple as long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Expect to experiment when designing an application to operate with a minimum value. Ceramic capacitors or other low ESR types are recommended. See *AN-2024 LMZ1420x / LMZ1200x Evaluation Board* (SNVA422) for more detail.

Equation 6 provides a good first-pass approximation of $C_O$ for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT\text{-}TRAN}) \quad (6)$$

Solving:

$$C_O \geq 2\ A \times 0.8\ V \times 10\ \mu H \times 24\ V / (4 \times 3.3\ V \times (24\ V - 3.3\ V) \times 33\ mV) \geq 43\ \mu F \quad (7)$$

The LMZ14202 demonstration and evaluation boards are populated with a 100-µF 6.3-V X5R output capacitor. Locations for extra output capacitors are provided. See See *AN-2024 LMZ1420x / LMZ1200x Evaluation Board* (SNVA422) for locations.

#### 8.2.2.1.5 Input Capacitance ($C_{IN}$) Selection

The LMZ14202 module contains an internal 0.47-µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance must be very close to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst-case input ripple current rating is dictated by Equation 8:

$$I_{CIN(rms)} \cong \frac{1}{2} \times I_O \times \sqrt{\frac{D}{1-D}}$$

where

- $D \cong V_O / V_{IN}$ (8)

The worst-case ripple current occurs when the module is presented with full load current and when $V_{IN}$ = (2 × $V_O$).

Recommended minimum input capacitance is 10-µF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature deratings of the capacitor selected.

**NOTE**

If the capacitor data sheet omits ripple current rating of the ceramic capacitors, contact the capacitor manufacturer to obtain this rating.

If the system design requires a certain minimum value of input ripple voltage $\Delta V_{IN}$ be maintained then Equation 9 may be used.

$$C_{IN} \geq I_O \times D \times (1\text{–}D) / f_{SW\text{-}CCM} \times \Delta V_{IN} \quad (9)$$

If $\Delta V_{IN}$ is 1% of $V_{IN}$ for a 24V input to 3.3V output application this equals 240 mV and $f_{SW}$ = 400 kHz.

$C_{IN} \geq 2\ A \times 3.3\ V / 24V \times (1\text{–}\ 3.3\ V/24\ V) / (400000 \times 0.240\ V)$

$\geq 2.5\ \mu F$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

#### 8.2.2.1.6 $R_{DS(on)}$ Resistor Selection

Many designs begin with a desired switching frequency in mind. For that purpose Equation 10 can be used.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{DS(on)}) \quad (10)$$

This can be rearranged as

$$R_{DS(on)} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (11)$$

The selection of RON and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the *Constant On-Time Control (COT) Circuit Overview* section.

The ON-time of the LMZ14202 timer is determined by the resistor $R_{DS(on)}$ and the input voltage $V_{IN}$. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{DS(on)}) / V_{IN} \quad (12)$$

The inverse relationship of $t_{ON}$ and $V_{IN}$ gives a nearly constant switching frequency as $V_{IN}$ is varied. Select an $R_{DS(on)}$ level to fascilitate an ON-time at maximum $V_{IN}$ is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for $t_{ON}$. This function imits the maximum operating frequency, which is governed by Equation 13:

$$f_{SW(max)} = V_O / (V_{IN(max)} \times 150 \text{ ns}) \quad (13)$$

Use Equation 14 to select $R_{DS(on)}$ a particular operating frequency while maintaining the minimum ON-time of 150 ns.

$$R_{DS(on)} \geq V_{IN(max)} \times 150 \text{ ns} / (1.3 \times 10^{-10}) \quad (14)$$

If $R_{DS(on)}$ calculated in Equation 11 is less than the minimum value determined in Equation 14, select a lower frequency. Alternatively, $V_{IN(max)}$ can also be limited to keep the frequency unchanged.

**NOTE**

The minimum OFF-time of 260 ns limits the maximum duty ratio. Select a larger $R_{DS(on)}$ (lower $f_{SW}$) for any application requiring large duty ratio.

#### *8.2.2.1.6.1 Discontinuous Conduction and Continuous Conduction Mode Selection*

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 10\ \mu H \times 1.18 \times 10^{20} \times I_O/(V_{IN}–V_O) \times R_{DS(on)}{}^2 \quad (15)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 7 above.

Following is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

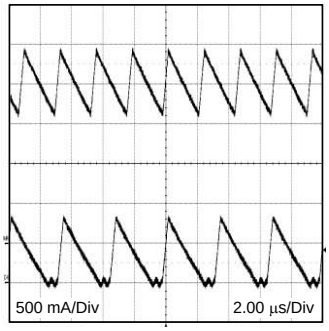



**Figure 33. CCM and DCM Operating Modes**
**$V_{IN}$ = 24 V, $V_O$ = 3.3 V, $I_O$ = 2 A/0.32 A 2 µs/div**

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN}– V_O)/(2 \times 10\ \mu H \times f_{SW(CCM)} \times V_{IN}) \quad (16)$$

Following is a typical waveform showing the boundary condition.

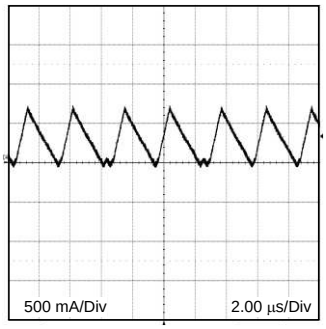



**Figure 34. Transition Mode Operation**
**$V_{IN}$ = 24 V, $V_O$ = 3.3 V, $I_O$ = 0.35 A 2 µsec/div**

The inductor internal to the module is 10 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current ($I_{LR}$). $I_{LR}$ can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} - V_O)/(10\ \mu H \times f_{SW} \times V_{IN}) \quad (17)$$

where

- $V_{IN}$ is the maximum input voltage and $f_{SW}$ is determined from Equation 10.

If the output current $I_O$ is determined by assuming that $I_O = I_L$, the higher and lower peak of $I_{LR}$ can be determined. Be aware that the lower peak of $I_{LR}$ must be positive if CCM operation is required.

### 8.2.3 Application Curves

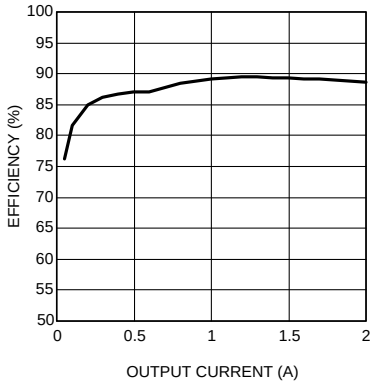



**Figure 35. Efficiency $V_{IN}$ = 24 V $V_{OUT}$ = 5 V**

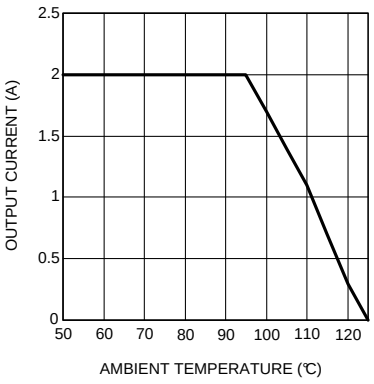



**Figure 36. Thermal Derating Curve $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V,**

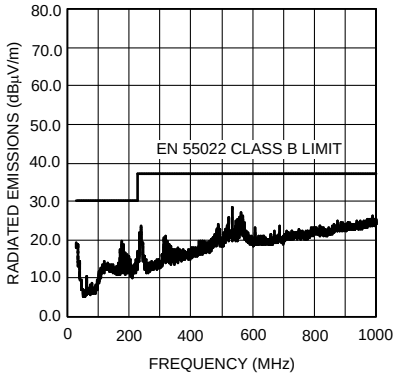



**Figure 37. Radiated Emissions (EN 55022 Class B) From Evaluation Board**

# 9 Power Supply Recommendations

The LMZ14202 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. Use a well-regulated input supply that can withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZ14202 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ14202, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

# 10 Layout

## 10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

- **Minimize area of switched current loops.** Wehn considering EMI reduction, it is imperative to minimize the high di/dt paths during PC board layout. The high-current loops that do not overlap have high di/dt content that cause observable high frequency noise on the output pin if the input capacitor ($C_{IN1}$) is placed at a distance away from the LMZ14202. Therefore place $C_{IN1}$ as close as possible to the LMZ14202 VIN and GND exposed thermal pad. This placement minimizes the high di/dt area and reduce radiated EMI. Additionally, ensure that grounding for both the input and output capacitor consists of a localized top side plane that connects to the GND exposed thermal pad (EP).
- **Have a single point ground.** Route the ground connections for the feedback, soft-start, and enable components to the GND pin of the device. This routing prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to the exposed thremal pad.
- **Minimize trace length to the FB pin.** Place both feedback resistors, $R_{FBT}$ and $R_{FBB}$, and the feed forward capacitor $C_{FF}$, close to the FB pin. Because the FB node is high impedance, maintain the copper area as small as possible. To minimize noise, route the traces from $R_{FBT}$, $R_{FBB}$, and $C_{FF}$ away from the body of the LMZ14202 device.
- **Make input and output bus connections as wide as possible.** Width reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load to correct for voltage drops and provide optimum output accuracy.
- **Provide adequate device heat-sinking.** Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 10 mils (254 µm) thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to maintain the junction temperature below 125°C.

## 10.2 Layout Example

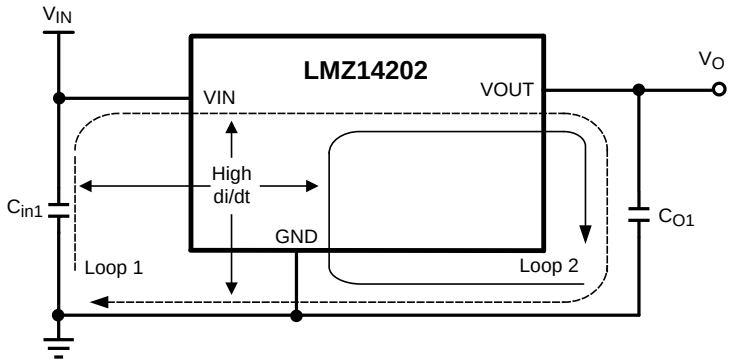



**Figure 38. Minimize Area of Current Loops in Buck Module**

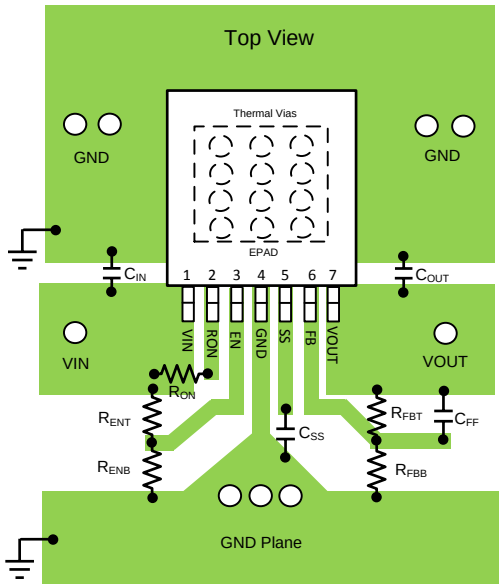



**Figure 39. PCB Layout Guide**

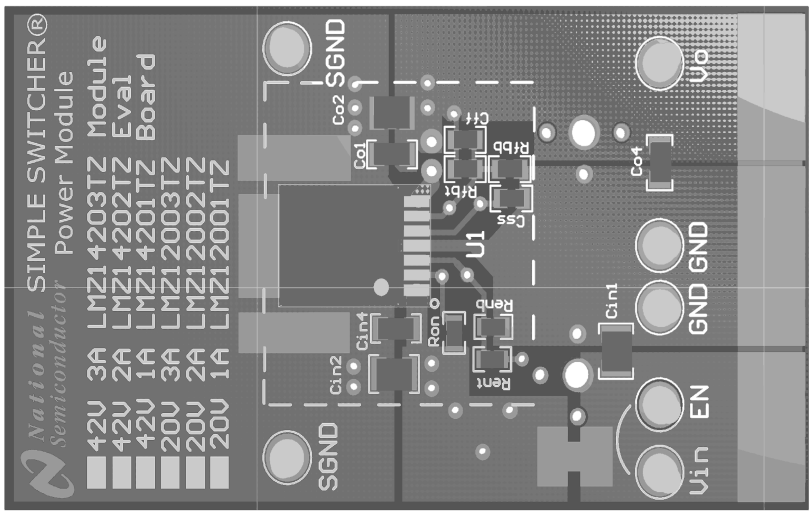



**Figure 40. EVM Board Layout - Top View**

## Layout Example (continued)

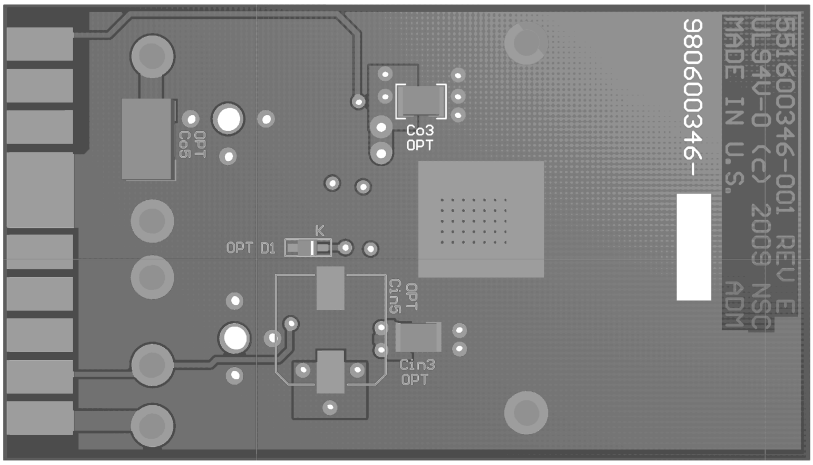



**Figure 41. EVM Board Layout - Bottom View**

## 10.3 Power Dissipation and Board Thermal Requirements

When $V_{IN}$ = 24 V, $V_O$ = 3.3 V, $I_O$ = 2 A, $T_{A(max)}$ = 85°C , and $T_J$ = 125°C, the device must achieve a thermal resistance from case-to-ambient described by Equation 18.

$$R_{\theta CA} < (T_{J(max)} - T_{A(max)}) / P_{IC\text{-}LOSS} - R_{\theta JC} \quad (18)$$

Given the typical thermal resistance from junction to case to be 1.9 °C/W, use the 85°C power dissipation curves in *Typical Characteristics* to estimate the $P_{IC\text{-}LOSS}$ for the application. In this application it is 1.5 W.

$$R_{\theta CA} = (125 - 85) / (1.5\ W - 1.9) = 24.8 \quad (19)$$

To reach $R_{\theta CA}$ = 24.8, the PCB is required to dissipate heat effectively. With no airflow and no external heat, use Equation 20 to estimate the required board area covered by 1 oz. copper on both the top and bottom metal layers.

$$\text{Board Area\_cm}^2 = 500°C \times \text{cm}^2/W / R_{\theta JC} \quad (20)$$

As a result, approximately 20.2 square cm of 1 oz copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately thirty-six, 10 mils (254 µm) thermal vias spaced 59 mils (1.5 mm) apart must connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout, refer to the *AN-2024 LMZ1420x / LMZ1200x Evaluation Board* (SNVA422) .

## 10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- **Land Pattern** Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- **Stencil Aperture**
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- **Solder Paste** Use a standard SAC Alloy such as SAC 305, type 3 or higher
- **Stencil Thickness**: 0.125 to 0.15 mm
- **Reflow**: Refer to solder paste supplier recommendation and optimized per board size and density
  - Refer to AN SNAA214 for reflow information
  - Maximum number of reflows allowed is one

## Power Module SMT Guidelines (continued)

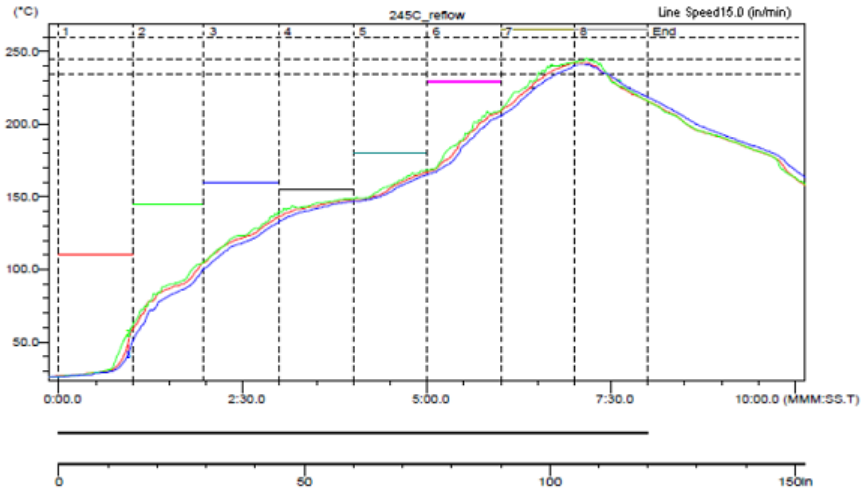



**Figure 42. Sample Reflow Profile**

**Table 3. Sample Reflow Profile Table**

| Probe | Max Temp (°C) | Reached Max Temp | Time Above 235°C | Reached 235°C | Time Above 245°C | Reached 245°C | Time Above 260°C | Reached 260°C |
|---|---|---|---|---|---|---|---|---|
| #1 | 242.5 | 6.58 | 0.49 | 6.39 | 0.00 | – | 0.00 | – |
| #2 | 242.5 | 7.10 | 0.55 | 6.31 | 0.00 | 7.10 | 0.00 | – |
| #3 | 241.0 | 7.09 | 0.42 | 6.44 | 0.00 | – | 0.00 | – |

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 Third-Party Products Disclaimer

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### 11.1.2 开发支持

WEBENCH 软件采用一种迭代设计过程并可访问综合元件数据库。 欲了解更多信息，请访问 www.ti.com/WEBENCH。

## 11.2 文档支持

### 11.2.1 相关文档

本节包含了以下附加支持文档。

- *《LMZ1 和 LMZ2 电源模块设计摘要》*，SNAA214
- *《AN-2027 LMZ14203 SIMPLE SWITCHER 电源模块的反向应用》*，SNVA425
- *《评估板应用手册 AN-2024》*，SNVA422
- *《焊接相关的最大绝对额定值》*，SNOA549

## 11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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## 11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMZ14202TZ-ADJ/NOPB | ACTIVE | TO-PMOD | NDW | 7 | 250 | RoHS & Green | SN | Level-3-245C-168 HR | -40 to 125 | LMZ14202 TZ-ADJ | Samples |
| LMZ14202TZE-ADJ/NOPB | ACTIVE | TO-PMOD | NDW | 7 | 45 | RoHS & Green | SN | Level-3-245C-168 HR | -40 to 125 | LMZ14202 TZ-ADJ | Samples |
| LMZ14202TZX-ADJ/NOPB | ACTIVE | TO-PMOD | NDW | 7 | 500 | RoHS & Green | SN | Level-3-245C-168 HR | -40 to 125 | LMZ14202 TZ-ADJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

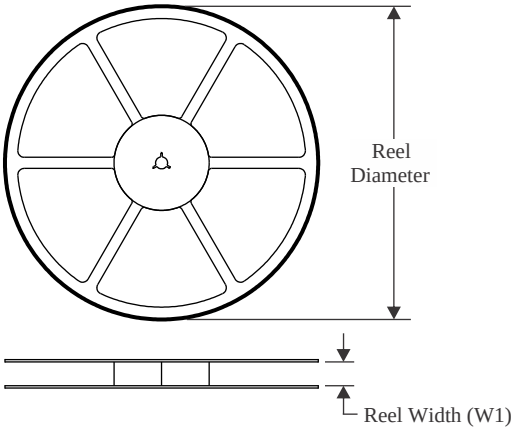
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

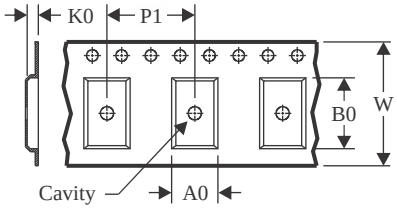
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

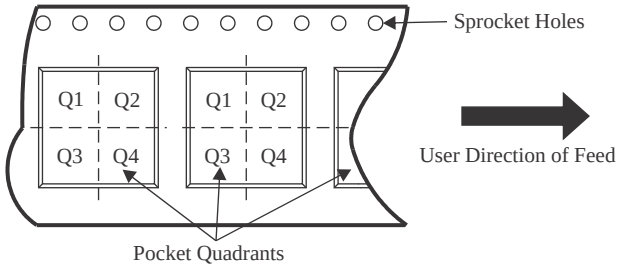



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

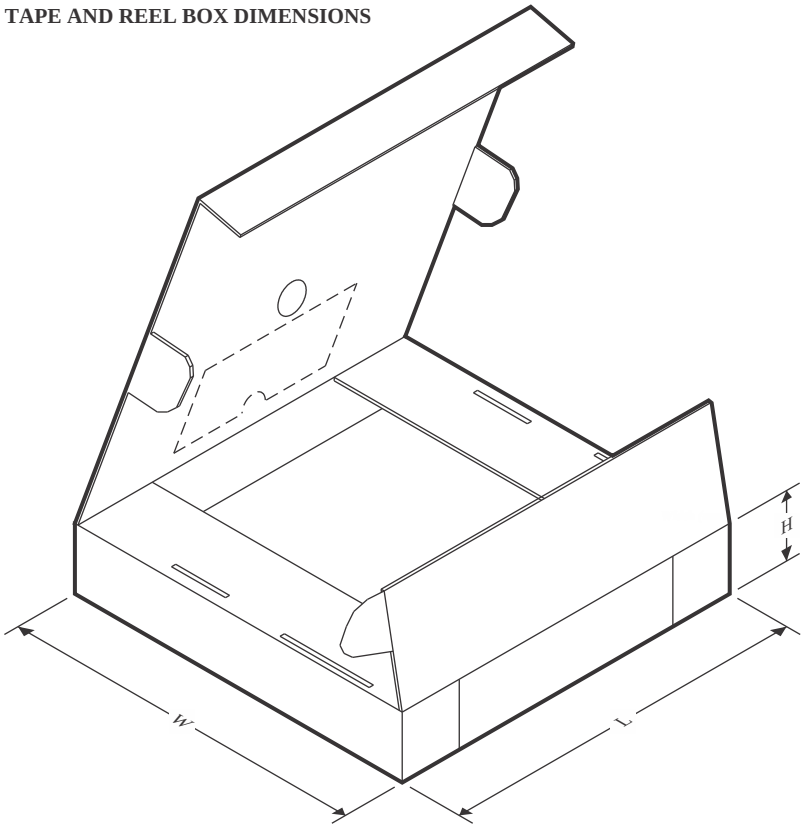
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMZ14202TZ-ADJ/NOPB | TO-PMOD | NDW | 7 | 250 | 330.0 | 24.4 | 10.6 | 14.22 | 5.0 | 16.0 | 24.0 | Q2 |
| LMZ14202TZX-ADJ/NOPB | TO-PMOD | NDW | 7 | 500 | 330.0 | 24.4 | 10.6 | 14.22 | 5.0 | 16.0 | 24.0 | Q2 |

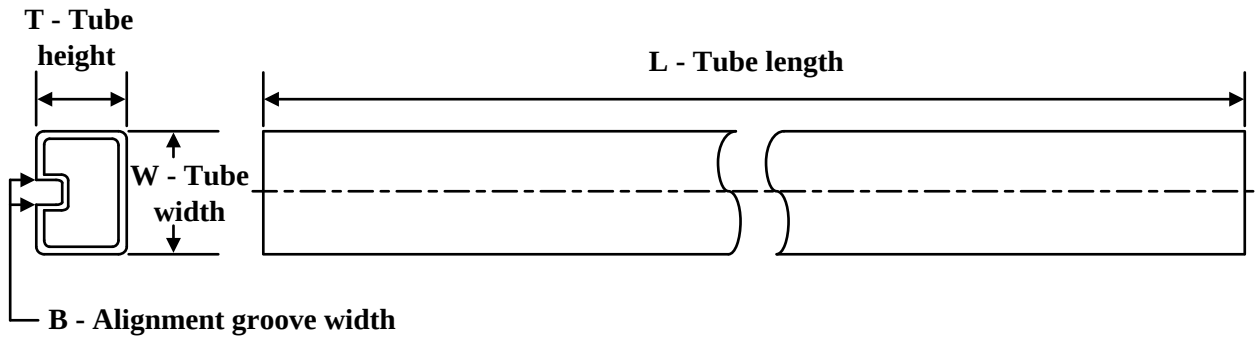
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMZ14202TZ-ADJ/NOPB | TO-PMOD | NDW | 7 | 250 | 356.0 | 356.0 | 45.0 |
| LMZ14202TZX-ADJ/NOPB | TO-PMOD | NDW | 7 | 500 | 356.0 | 356.0 | 45.0 |

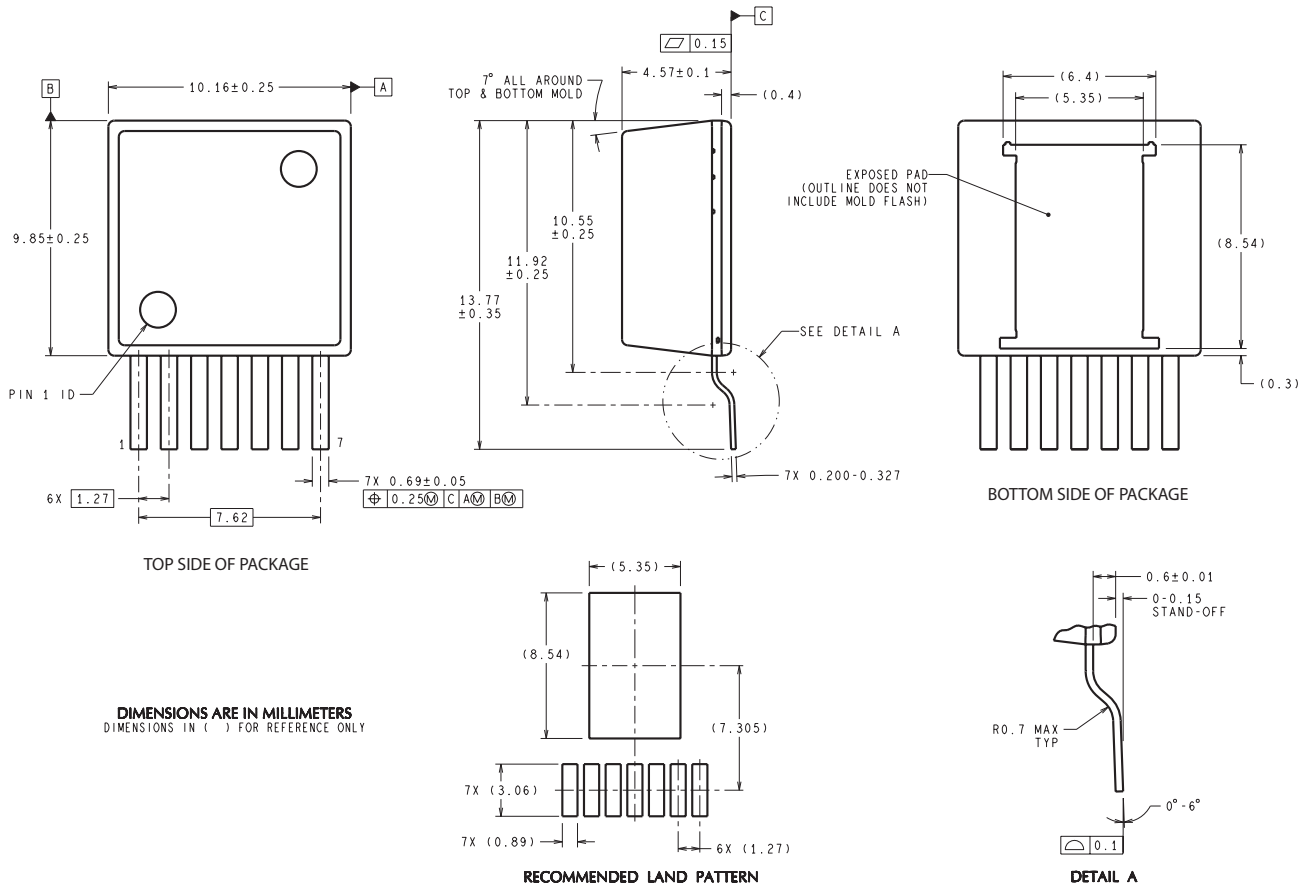
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LMZ14202TZE-ADJ/NOPB | NDW | TO-PMOD | 7 | 45 | 502 | 17 | 6700 | 8.4 |

# NDW0007A




TZA07A (Rev D)

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