# VOICE SYNTHESIZER

## GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

### Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I²C bus
- Software readable status word (parallel bus or I²C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

## QUICK REFERENCE DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | – | 5 | – | V |
| Supply current | $I_{DD}$ | – | 12 | # | mA |
| Supply current (stand-by) | $I_{DD(SB)}$ | – | 1 | – | μA |
| **Inputs** | | | | | |
| Input voltage | $V_{IH}$ | 2,0 | – | $V_{DD}$ | V |
| Input voltage | $V_{IL}$ | 0 | – | 0,8 | V |
| Input capacitance | $C_I$ | – | 7 | – | pF |
| **Outputs** (D5 to D7) | | | | | |
| Output voltage high | $V_{OH}$ | 3,5 | – | $V_{DD}$ | V |
| Output voltage low | $V_{OL}$ | 0 | – | 0,4 | V |
| Load capacitance | $C_L$ | – | – | 80 | pF |
| Operating ambient temperature range | $T_{amb}$ | −40 | – | + 85 | °C |

# Value not yet available.

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

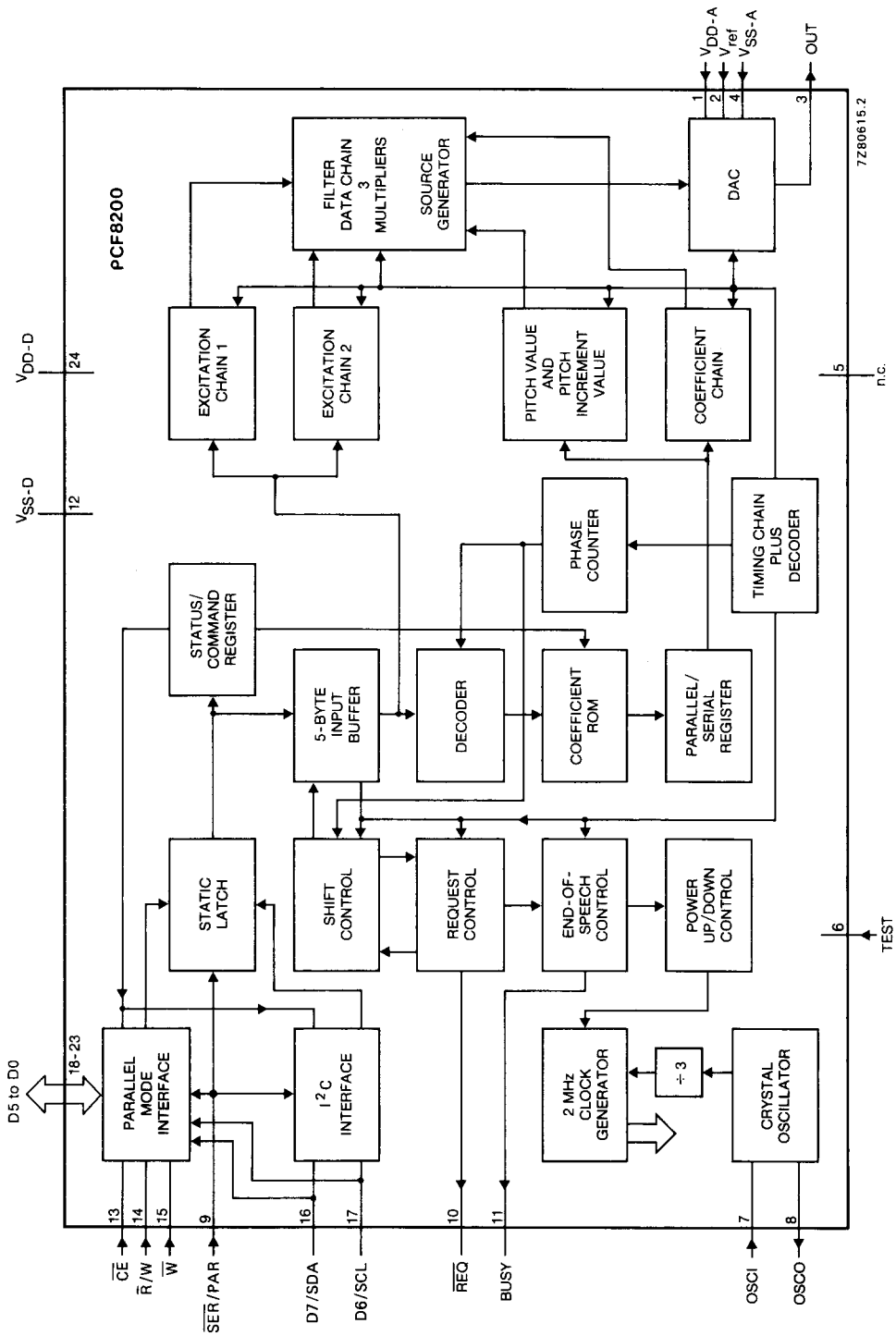



Fig. 1 Block diagram.

## PINNING

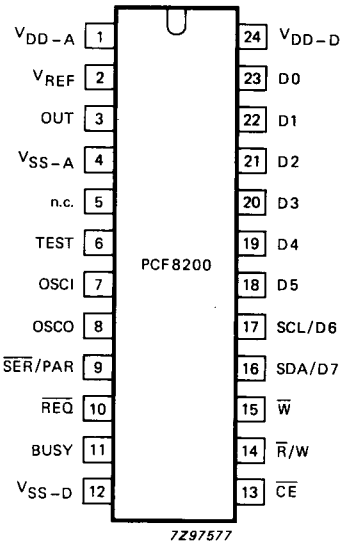



Fig. 2 Pinning diagram.

DEVELOPMENT DATA

| | | |
|---|---|---|
| 1 | $V_{DD-A}$ | positive supply voltage for DAC output stage |
| 2 | $V_{REF}$ | DAC reference voltage input |
| 3 | OUT | speech output |
| 4 | $V_{SS-A}$ | negative supply voltage for DAC stage |
| 5 | n.c. | not connected |
| 6 | TEST | for normal operation this pin must be grounded ($V_{SS}$) |
| 7 | OSCI | oscillator input |
| 8 | OSCO | oscillator output |
| 9 | $\overline{SER}$/PAR | for parallel data bus operation this pin is hard-wired to $V_{DD}$, or to $V_{SS}$ to enable the $I^2C$ bus |
| 10 | $\overline{REQ}$ | status bit indicating request for data |
| 11 | BUSY | status indicating synthesizer busy |
| 12 | $V_{SS-D}$ | negative supply voltage for digital circuits |
| 13 | $\overline{CE}$ | chip-enable input |
| 14 | $\overline{R}$/W | read/write control input |
| 15 | $\overline{W}$ | write input |
| 16 | SDA/D7 | $I^2C$ bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode) |
| 17 | SCL/D6 | $I^2C$ bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode) |
| 18 | D5 | parallel data input/outputs |
| 19 | D4 | |
| 20 | D3 | |
| 21 | D2 | |
| 22 | D1 | |
| 23 | D0 | |
| 24 | $V_{DD-D}$ | positive supply voltage for digital circuits |

## FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

## OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

| FD1, FD0 | 10 | 01 | 00 | 11 | FS0, FS1 |
|---|---|---|---|---|---|
| 00 | 8,8 | 10,4 | 12,8 | 17,6 | ms |
| 01 | 17,6 | 20,8 | 25,6 | 35,2 | ms |
| 10 | 26,4 | 31,2 | 38,4 | 52,8 | ms |
| 11 | 44,0 | 52,0 | 64,0 | 88,0 | ms |

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

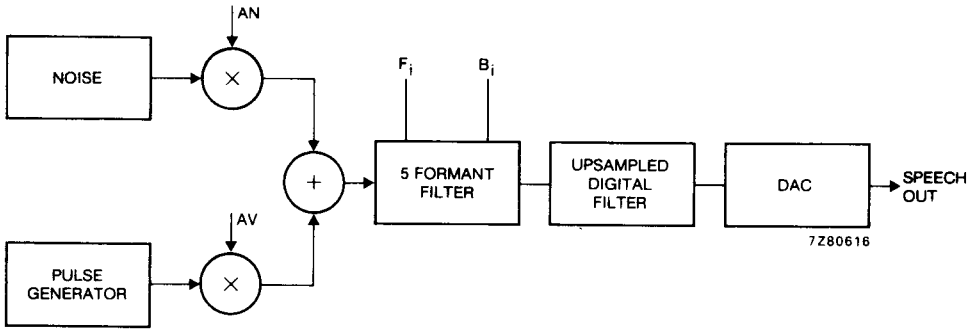



Fig. 3 Block diagram of formant synthesizer.

## DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

### DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or $V_{DD}$ on. Table 2 indicates the amplitude factor.

| byte | factor | dB |
|---|---|---|
| 01110000 | 3,5 | 10,88 |
| 10110000 | 3,25 | 10,24 |
| 00110000 | 3,0 | 9,54 |
| 11010000 | 2,75 | 8,97 |
| 01010000 | 2,5 | 7,96 |
| 10010000 | 2,25 | 7,04 |
| 00010000 | 2,0 | 6,02 |
| 11100000 | 1,75 | 4,86 |
| 01100000 | 1,5 | 3,52 |
| 10100000 | 1,25 | 1,94 |
| 00100000 | 1,0 | 0,00 |
| 11000000 | 0,75 | −2,50 |
| 01000000 | 0,5 | −6,02 |
| 10000000 | 0,25 | −12,04 |
| 00000000 | 0,0 | |
| 11110000 | HEX code F0 is not allowed as a DAC amplitude | |

Table 2 DAC amplitude factor.

### Start pitch

The second byte after a STOP or BADSTOP, or $V_{DD}$ on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

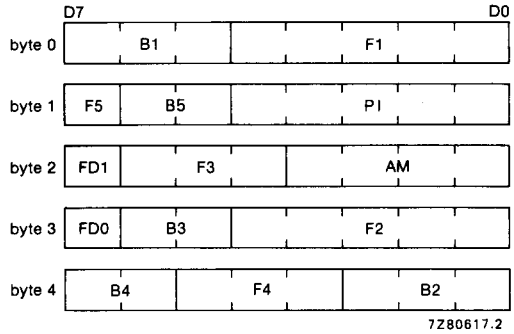
### Frame Data

The frame data is a five byte block which contains the filter and source information:

| | |
|---|---|
| pitch increment/decrement value | 5 bits |
| amplitude | 4 bits |
| frame duration | 2 bits |
| frequency of 1st formant | 5 bits |
| frequency of 2nd formant | 5 bits |
| frequency of 3rd formant | 3 bits |
| frequency of 4th formant | 3 bits |
| frequency of 5th formant | 1 bit |
| bandwidth of 1st formant | 3 bits |
| bandwidth of 2nd formant | 3 bits |
| bandwidth of 3rd formant | 2 bits |
| bandwidth of 4th formant | 2 bits |
| bandwidth of 5th formant | 2 bits |
| | 40 bits = 5 bytes |

The frame-data bits are organized as shown in Fig. 4.

DEVELOPMENT DATA




It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

## CONTROL FORMAT

### Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

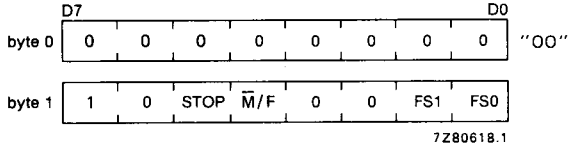



Fig. 5 Control write: first byte fixed, second byte control.

**FS0, FS1 speed option**

| FS1 | FS0 | speech speed | standard-frame duration |
|---|---|---|---|
| 0 | 0 | 100% | 12,8 ms |
| 0 | 1 | 145% | 8,8 ms |
| 1 | 0 | 123% | 10,4 ms |
| 1 | 1 | 73% | 17,6 ms |

**$\overline{M}$/F, male/female option**

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

**STOP**

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

### Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

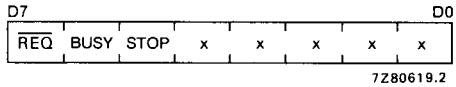



Fig. 6 Status read.

| | | |
|---|---|---|
| $\overline{REQ}$ | = 1 | No data required |
| | = 0 | Synthesizer requesting for new data |
| BUSY | = 1 | Busy (an utterance is pronounced) |
| | = 0 | Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode |
| STOP | | The STOP bit is the same as the stop bit written to the synthesizer during a command write.<br>STOP = 1, BUSY = 0 stopped by the user.<br>STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time. |

After initial power-up the status/command register is set to the following status:

| | | |
|---|---|---|
| FS0, FS1 | = 0 | Standard-frame duration of 12,8 ms |
| $\overline{M}$/F | = 0 | Male quantization table |
| STOP | = 0 | |
| BUSY | = 0 | Idle |
| $\overline{REQ}$ | = 1 | No data required |

DEVELOPMENT DATA

### INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The $I^2C$ transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

### $I^2C$ ADDRESS

On chip there is a $I^2C$ slave receiver/transmitter with the address:

7 6 5 4 3 2 1 0
0 0 1 0 0 0 0 R/W

## POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The $I^2C$ transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

## POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial $V_{DD}$ the synthesizer is in power-down mode.

## HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| parameter | conditions | symbol | min. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage | any pin with respect to $V_{SS}$ | $V_{DD}$ | −0,3 | 7,5 | V |
| Input voltage | any pin with respect to $V_{SS}$ | $V_I$ | −0,3 | 7,5 | V |
| Output voltage | any pin with respect to $V_{SS}$ | $V_O$ | −0,3 | 7,5 | V |
| D.C. input diode current | $V_I < V_{SS}$ | $-I_{IK}$ | – | 20 | mA |
| | $V_I > V_{DD}$ | $I_{IK}$ | – | 20 | mA |
| D.C. output diode current | $V_O < V_{SS}$ | $-I_{OK}$ | – | 20 | mA |
| | $V_O > V_{DD}$ | $I_{OK}$ | – | 20 | mA |
| Operating ambient temperature range | | $T_{amb}$ | −40 | 85 | °C |
| Storage temperature range | | $T_{stg}$ | −55 | 125 | °C |

## CHARACTERISTICS

$T_{amb}$ = −45 to + 85 °C; supply voltage ($V_{DD}$ to $V_{SS}$) = 4,5 to 5,5 V with respect to $V_{SS}$, unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage | $V_{DD}$ | 4,5 | 5,0 | 5,5 | V |
| Supply current | $I_{DD}$ | – | 10 | – | mA |
| Standby current | $I_{DD(SB)}$ | – | 200 | – | μA |
| **Inputs** | | | | | |
| **$\overline{CE}$, R/$\overline{W}$, $\overline{W}$** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V |
| Input leakage current $V_{in}$ = 0 to 5,5 V | $I_{IR}$ | −10 | – | 10 | μA |
| Rise and fall times (note 2) | $t_{rf}$ | – | – | 50 | ns |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **OSCI** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,2 | – | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V |
| Input leakage current $V_{in}$ = 0 to 5,5 V | $I_{IR}$ | −10 | – | 10 | μA |
| Rise and fall times (note 2) | $t_{rf}$ | – | – | 50 | ns |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **PARALLEL MODE** | | | | | |
| **Input Characteristics (D0 to D7)** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V |
| Input leakage current ($V_{in}$ = 0 to 5,5 V, output off) | $I_{IR}$ | −10 | – | 10 | μA |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Output Characteristics (D5 to D7 only)** | | | | | |
| Output voltage HIGH ($I_{OH}$ = −100 μA) | $V_{OH}$ | 3,5 | – | $V_{DD}$ | V |
| Output voltage LOW ($I_{OL}$ = 3,2 mA) | $V_{OL}$ | 0 | – | 0,4 | V |
| Load capacitance | $C_L$ | – | – | 80 | pF |
| Rise and fall times (note 3) | $t_{rf}$ | – | – | 50 | ns |
| **SERIAL MODE** | | | | | |
| **Input characteristics (SDA and SDL)** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 3,0 | – | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 1,5 | V |
| Input leakage current ($V_{in}$ = 0 to 5,5 V, output off) | $I_{IR}$ | −10 | – | 10 | μA |
| Input capacitance | $C_I$ | – | – | 10 | pF |

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| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Output Characteristics (SDA only, open drain)** | | | | | |
| Output voltage LOW ($I_{OL}$ = 3 mA) | $V_{OL}$ | 0 | – | 0,4 | V |
| **OSCILLATOR** | | | | | |
| Crystal frequency | $f_{XTAL}$ | – | 6 | 6,1 | MHz |
| **$V_{REF}$** | | | | | |
| Reference voltage | $V_{REF}$ | 1,9 | – | $\frac{V_{DD}-1,5}{1,25}$ | V |
| Input leakage current (active) | $I_{IR}$ | – | 5 | – | μA |
| **Outputs** | | | | | |
| **$\overline{REQ}$, BUSY** | | | | | |
| Output voltage HIGH ($I_{OH}$ = 100 μA) | $V_{OH}$ | 3,5 | – | $V_{DD}$ | V |
| Output voltage LOW ($I_{QL}$ = 3,2 mA) | $V_{OL}$ | 0 | – | 0,4 | V |
| Load capacitance | $C_L$ | – | – | 80 | pF |
| Rise and fall times (note 3) | $t_{rf}$ | – | – | 50 | ns |
| **OUT** | | | | | |
| Output voltage | $V_{OUT}$ | 0,66 x $V_{REF}$ | | 1,34 x $V_{REF}$ | V |
| Minimum external load | | 600 | – | – | Ω |
| **Timing characteristics** (note 1) (Figs 8 and 9) | | | | | |
| Write enable | $t_{WR}$ | 200 | – | – | ns |
| Data set-up for write | $t_{DS}$ | 150 | – | – | ns |
| Data hold for write | $t_{DH}$ | 30 | – | – | ns |
| Read enable | $t_{RD}$ | 200 | – | – | ns |
| Data delay for read (note 2) | $t_{DD}$ | – | – | 150 | ns |
| Data floating for read (note 2) | $t_{DF}$ | – | – | 150 | ns |
| Control set-up | $t_{CS}$ | 0 | – | – | ns |
| Control hold | $t_{CH}$ | 0 | – | – | ns |
| REQ new (new byte of the same speech frame) | $t_{RN}$ | – | # (≈ 3) | | μs |
| REQ Valid | $t_{RV}$ | 0 | – | – | ns |
| REQ Hold | $t_{RH}$ | – | 250 | # | ns |

**NOTES TO THE CHARACTERISTICS**

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

# Values not yet available.

DEVELOPMENT DATA

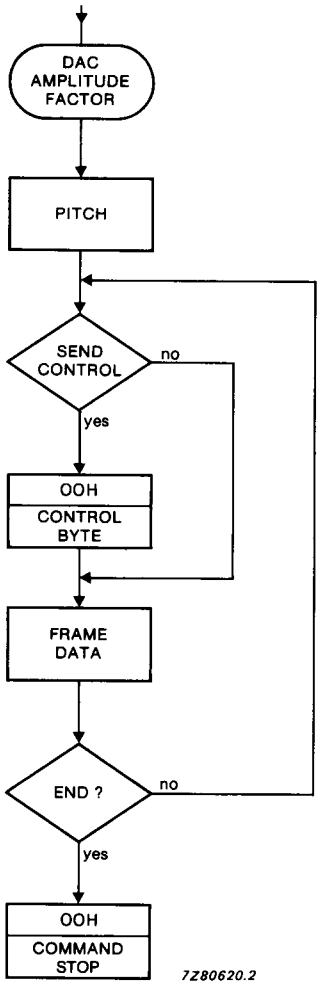
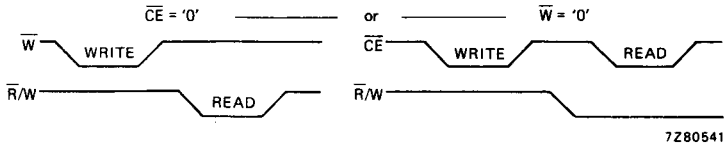



Fig. 7 Interface protocol.

### Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.




Typical connection of control signals.

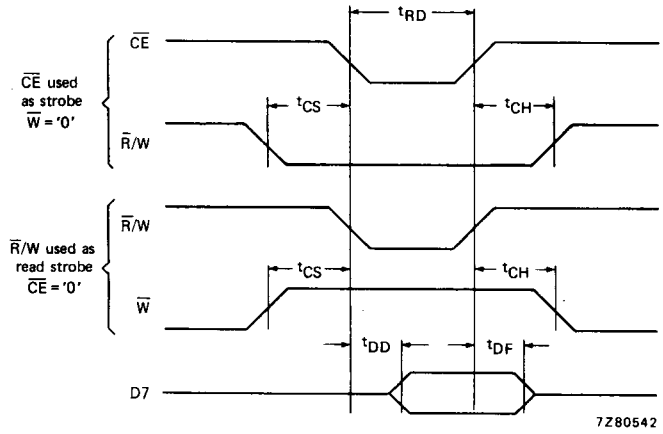



Fig. 8 Read timing.

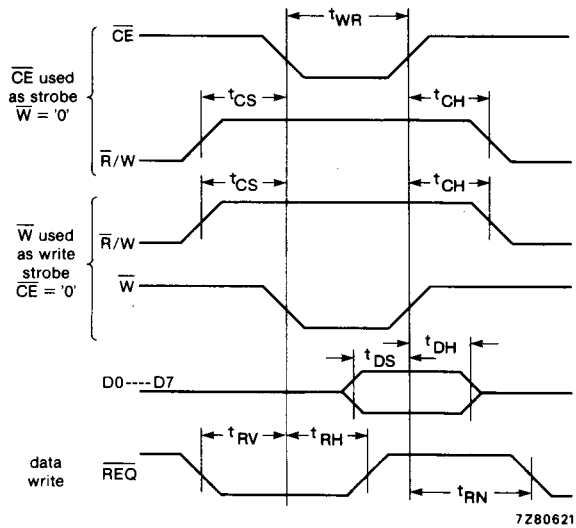



Fig. 9 Write timing.

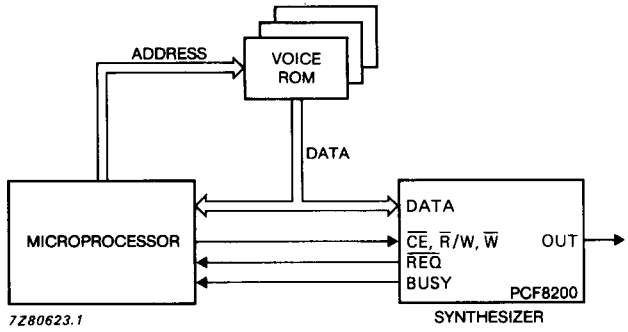



Fig. 10 Typical application configuration with parallel interface.



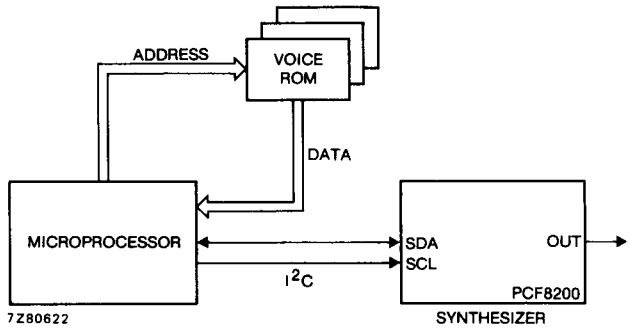



Fig. 11 Typical application configuration with series interface.

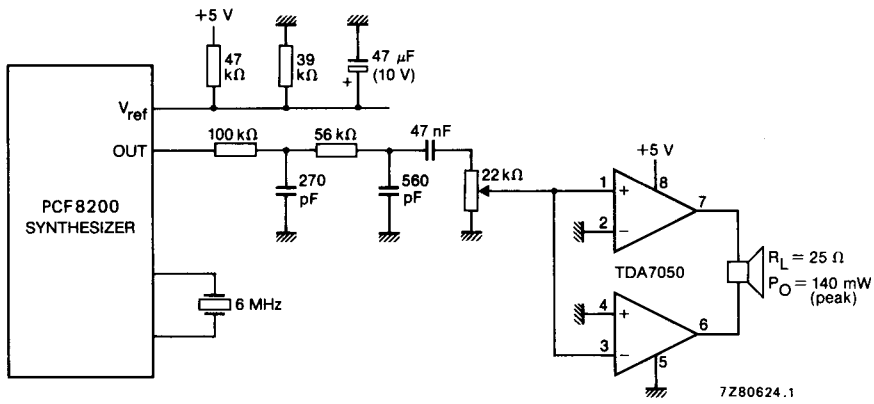



Fig. 12 An example of an output configuration.

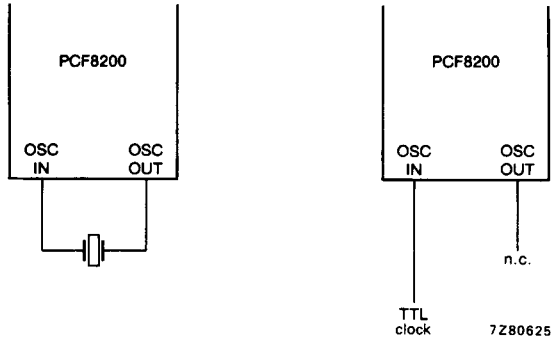



Fig. 13 Oscillator clock configurations.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.