12MHz Rail-to-Rail Input-Output Operational Amplifier

EL5220T

The EL5220T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5220T contains two amplifiers. Each amplifier exhibits beyond the rail input capability, rail-to-rail output capability and is unity gain stable.

The maximum operating voltage range is from 4.5V to 19V. It can be configured for single or dual supply operation, and typically consumes only 550µA per amplifier. The EL5220T has an output short circuit capability of ±200mA and a continuous output current capability of ±65mA.

The EL5220T features a slew rate of 12V/µs. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the amplifiers to offer maximum dynamic range at any supply voltage. These features make the EL5220T an ideal amplifier solution for use in TFT-LCD panels as a V_{COM} or static gamma buffer, and in high speed filtering and signal conditioning applications. Other applications include battery power and portable devices, especially where low power consumption is important.

The EL5220T is available in an 8 Ld MSOP package, and a thermally enhanced 8 Ld DFN package. Both feature a standard operational amplifier pinout. The devices operate over an ambient temperature range of -40°C to +85°C.

Features

- 12MHz (-3dB) Bandwidth
- 4.5V to 19V Maximum Supply Voltage Range
- 12V/µs Slew Rate
- 550µA Supply Current (per Amplifier)
- ±65mA Continuous Output Current
- ±200mA Output Short Circuit Current
- Unity-gain Stable
- Beyond the Rails Input Capability
- Rail-to-rail Output Swing
- Built-in Thermal Protection
- -40°C to +85°C Ambient Temperature Range
- Pb-free (RoHS Compliant)

Applications* (see page 13)

- TFT-LCD Panels
- V_{COM} Amplifiers
- Static Gamma Buffers
- Electronics Notebooks
- Electronics Games
- Touch-screen Displays
- Personal Communication Devices
- Personal Digital Assistants (PDA)
- Portable Instrumentation
- Sampling ADC Amplifiers
- Wireless LANs
- Office Automation
- Active Filters
- ADC/DAC Buffer

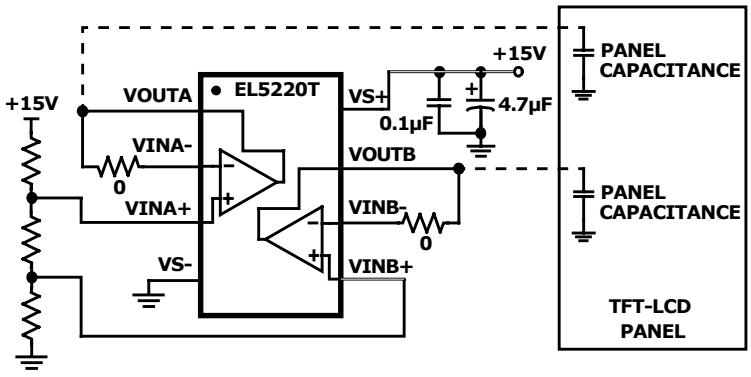


FIGURE 1. TYPICAL TFT-LCD V_{COM} APPLICATION

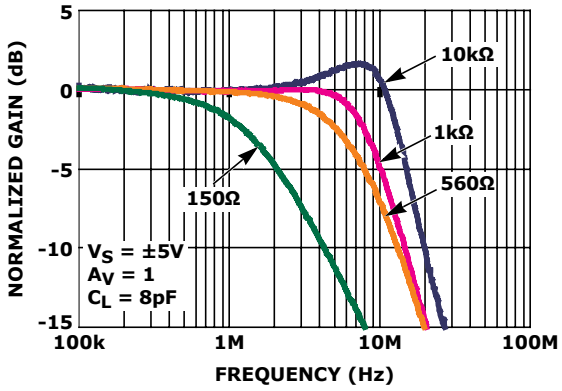
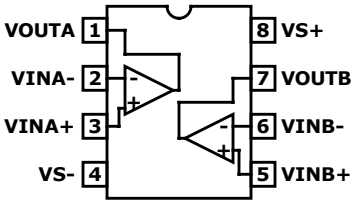


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS R_L

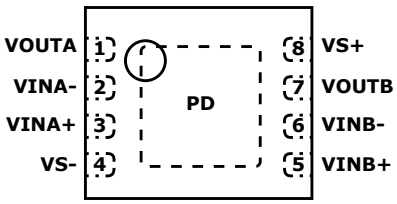
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pin Configuration

EL5220T
(8 LD MSOP)
TOP VIEW



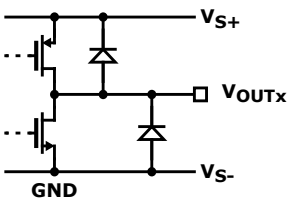
EL5220T
(8 LD DFN)
TOP VIEW



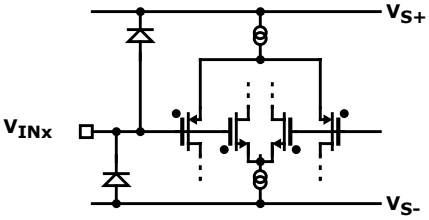
THERMAL PAD IS ELECTRICALLY CONNECTED TO VS-

Pin Descriptions

PIN NUMBER (MSOP, DFN)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUTA	Amplifier A output	(Reference Circuit 1)
2	VINA-	Amplifier A inverting input	(Reference Circuit 2)
3	VINA+	Amplifier A non-inverting input	(Reference Circuit 2)
4	VS-	Negative power supply	
5	VINB+	Amplifier B non-inverting input	(Reference Circuit 2)
6	VINB-	Amplifier B inverting input	(Reference Circuit 2)
7	VOUTB	Amplifier B output	(Reference Circuit 1)
8	VS+	Positive power supply	
PD	Thermal Pad	Functions as a heat sink. Electrically connected to VS-. Connect the thermal pad to VS- plane on the PCB for optimum thermal performance.	



CIRCUIT 1



CIRCUIT 2

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL5220TILZ-T13 (Note 1)	20T	8 Ld DFN	L8.2x3
EL5220TIYZ	BBBMA	8 Ld MSOP	M8.118A
EL5220TIYZ-T7 (Note 1)	BBBMA	8 Ld MSOP	M8.118A
EL5220TIYZ-T13 (Note 1)	BBBMA	8 Ld MSOP	M8.118A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL5220T. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . +19.8V
Input Voltage Range (V_{INx+}, V_{INx-}) . . . V_S- - 0.5V, V_S+ + 0.5V
Input Differential Voltage (V_{INx+} - V_{INx-}) . . . . . (V_S+ + 0.5V)-(V_S- - 0.5V)
Maximum Continuous Output Current . . . . . ±65mA
ESD Rating
Human Body Model 3000V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld MSOP (Notes 6, 7)	170	60
8 Ld DFN (Notes 4, 5)	58	8

Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Maximum Junction Temperature . . . . . +150°C
Power Dissipation . . . . . See Figures 32 and 33
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ to 0V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	18	mV
TCV_{OS}	Average Offset Voltage Drift (Note 8)	8 Ld MSOP package		5		µV/°C
		8 Ld DFN package		3		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For V_{INx} from -5.5V to +5.5V	50	75		dB
A_{VOL}	Open Loop Gain	-4.5V ≤ V_{OUTx} ≤ +4.5V	75	105		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.94	-4.85	V
V_{OH}	Output Swing High	I_L = +5mA	4.85	4.94		V
I_{SC}	Short Circuit Current	V_{CM} = 0V, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±200		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
(V_S+) - (V_S-)	Supply Voltage Range		4.5		19	V
I_S	Supply Current (Per Amplifier)	V_{CM} = 0V, No load		550	750	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from ±2.25V to ±9.5V	60	75		dB

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $R_L = 10k\Omega$ to 0V, $T_A = +25°C$, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 9)	$-4.0V \le V_{OUTx} \le +4.0V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 10)	$A_V = +1$, $V_{OUTx} = 2V$ step, $R_L = 10k\Omega$, $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 8pF$		12		MHz
GBWP	Gain-Bandwidth Product	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		50		°
CS	Channel Separation	f = 5MHz		85		dB

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 2.5V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3	18	mV
TCV_{OS}	Average Offset Voltage Drift (Note 8)	8 Ld MSOP package		5		µV/°C
		8 Ld DFN package		3		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For V_{INx} from -0.5V to +5.5V	45	70		dB
A_{VOL}	Open Loop Gain	$0.5V \le V_{OUTx} \le +4.5V$	75	105		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -2.5mA$		30	150	mV
V_{OH}	Output Swing High	$I_L = +2.5mA$	4.85	4.97		V
I_{SC}	Short Circuit Current	$V_{CM} = 2.5V$, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±125		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current (Per Amplifier)	$V_{CM} = 2.5V$, No load		550	750	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 9)	$1V \le V_{OUTx} \le 4V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 10)	$A_V = +1$, $V_{OUTx} = 2V$ step, $R_L = 10k\Omega$, $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 8pF$		12		MHz
GBWP	Gain-Bandwidth Product	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		50		°
CS	Channel Separation	f = 5MHz		85		dB

Electrical Specifications $V_S+ = +18V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 9V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 9V		5	18	mV
TCV_{OS}	Average Offset Voltage Drift (Note 8)	8 Ld MSOP package		6		µV/°C
		8 Ld DFN package		4		µV/°C
I_B	Input Bias Current	V_{CM} = 9V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+18.5	V
CMRR	Common-Mode Rejection Ratio	For V_{INx} from -0.5V to +18.5V	53	78		dB
A_{VOL}	Open Loop Gain	$0.5V \le V_{OUTx} \le 17.5V$	75	90		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -9mA		120	150	mV
V_{OH}	Output Swing High	I_L = +9mA	17.85	17.88		V
I_{SC}	Short Circuit Current	V_{CM} = 9V, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±200		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current (Per Amplifier)	V_{CM} = 9V, No load		650	850	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 9)	$1V \le V_{OUTx} \le 17V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 10)	A_V = +1, V_{OUTx} = 2V step, $R_L = 10k\Omega$, C_L = 8pF		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, C_L = 8pF		12		MHz
GBWP	Gain-Bandwidth Product	A_V = -50, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, C_L = 8pF		8		MHz
PM	Phase Margin	A_V = -50, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, C_L = 8pF		50		°
CS	Channel Separation	f = 5MHz		85		dB

NOTES:

8. Measured over -40°C to +85°C ambient operating temperature range. See the typical TCV_{OS} production distribution shown in the "Typical Performance Curves" on page 6.
9. Typical slew rate is an average of the slew rates measured on the rising (20% to 80%) and the falling (80% to 20%) edges of the output signal.
10. Settling time measured as the time from when the output level crosses the final value on rising/falling edge to when the output level settles within a ±0.1% error band. The range of the error band is determined by: Final Value(V)±[Full Scale(V)*0.1%]

Typical Performance Curves

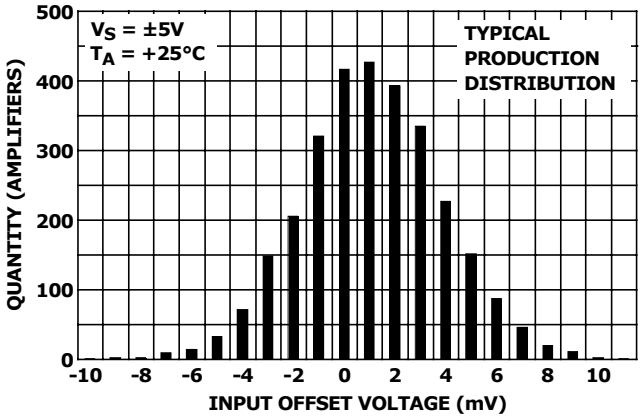


FIGURE 3. INPUT OFFSET VOLTAGE DISTRIBUTION

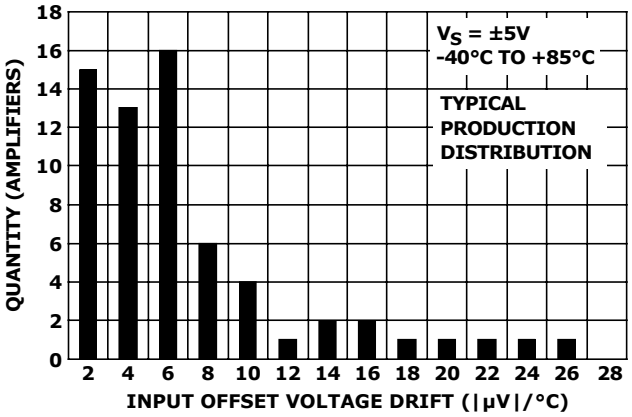


FIGURE 4. INPUT OFFSET VOLTAGE DRIFT (MSOP)

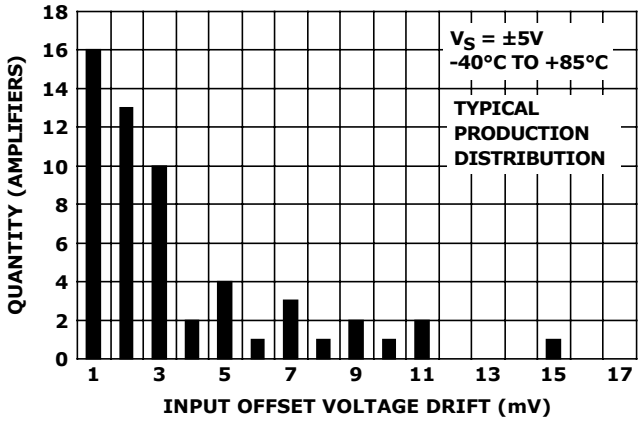


FIGURE 5. INPUT OFFSET VOLTAGE DRIFT (DFN)

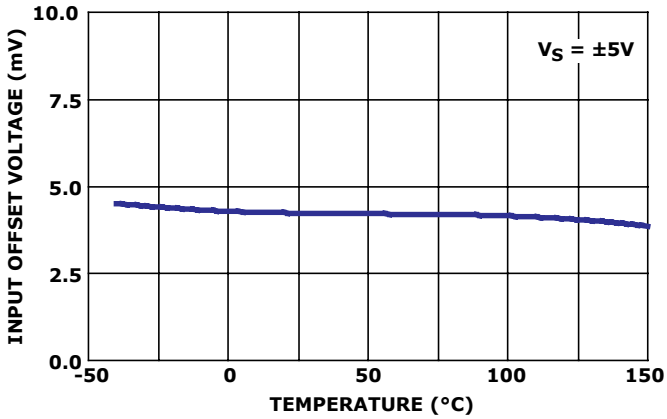


FIGURE 6. INPUT OFFSET VOLTAGE vs TEMPERATURE

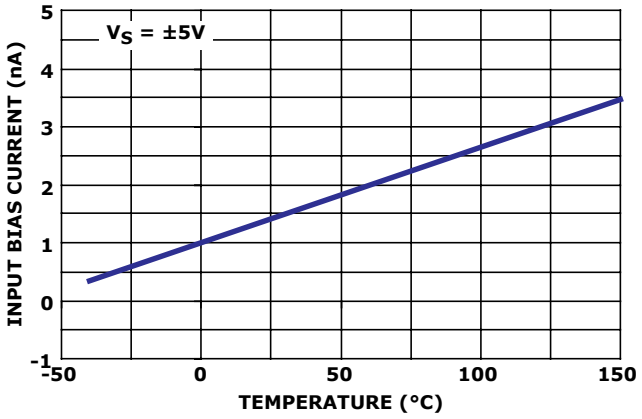


FIGURE 7. INPUT BIAS CURRENT vs TEMPERATURE

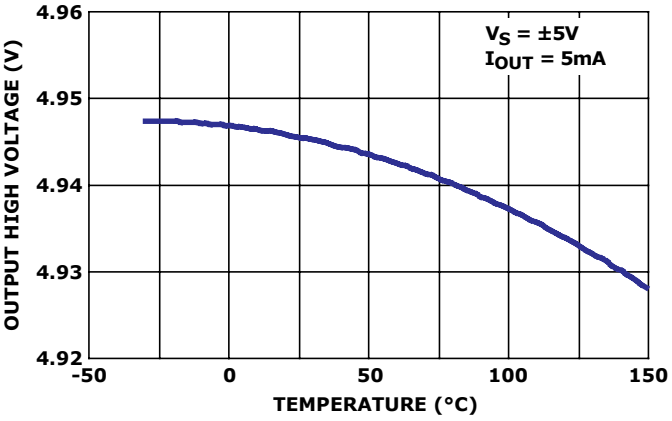


FIGURE 8. OUTPUT HIGH VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

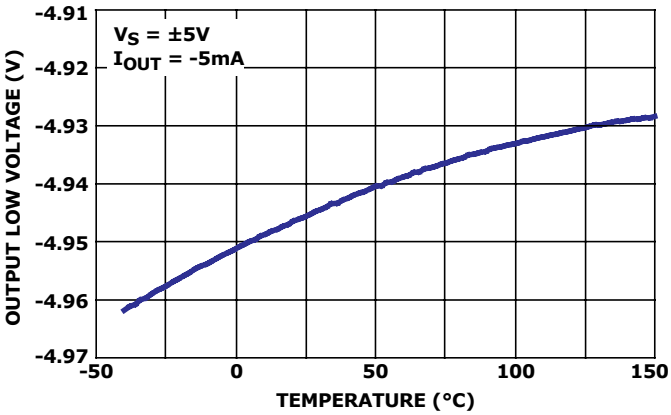


FIGURE 9. OUTPUT LOW VOLTAGE vs TEMPERATURE

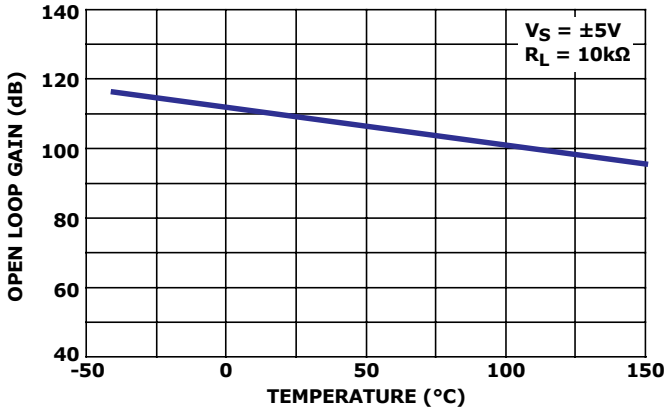


FIGURE 10. OPEN-LOOP GAIN vs TEMPERATURE

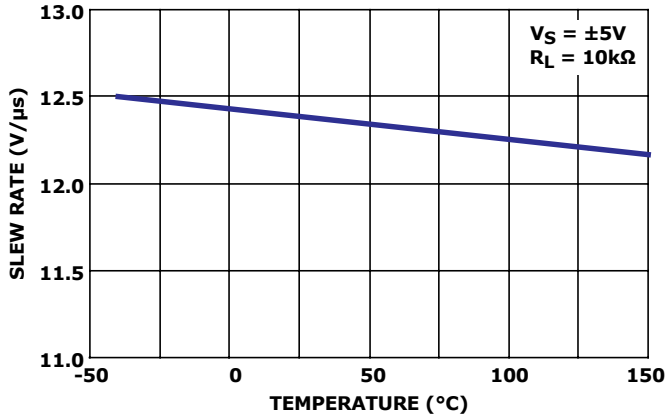


FIGURE 11. SLEW RATE vs TEMPERATURE

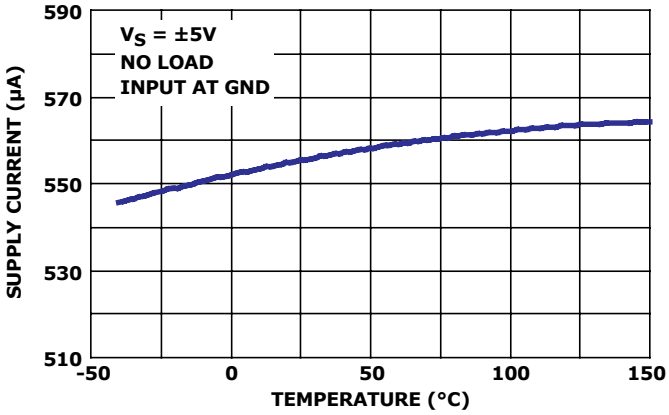


FIGURE 12. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

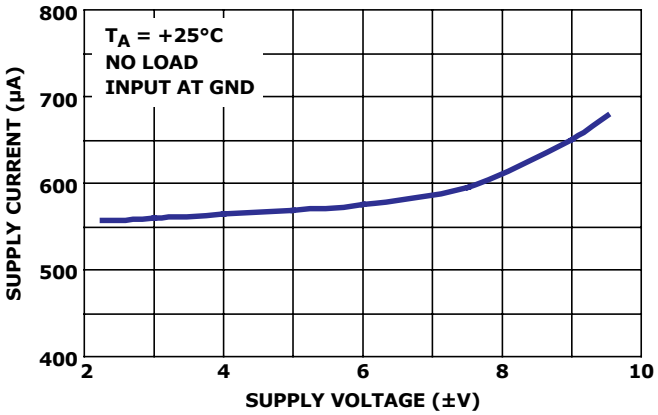


FIGURE 13. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

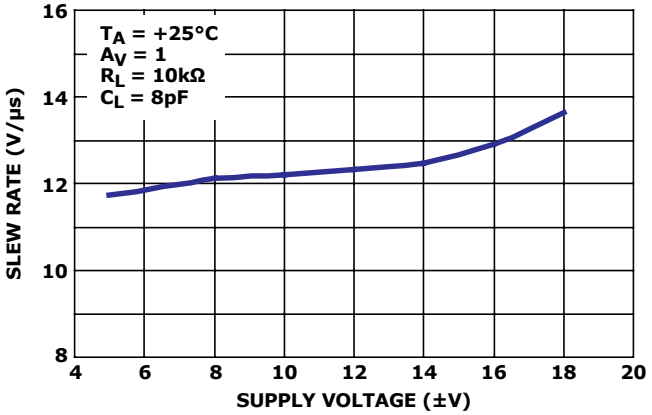


FIGURE 14. SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

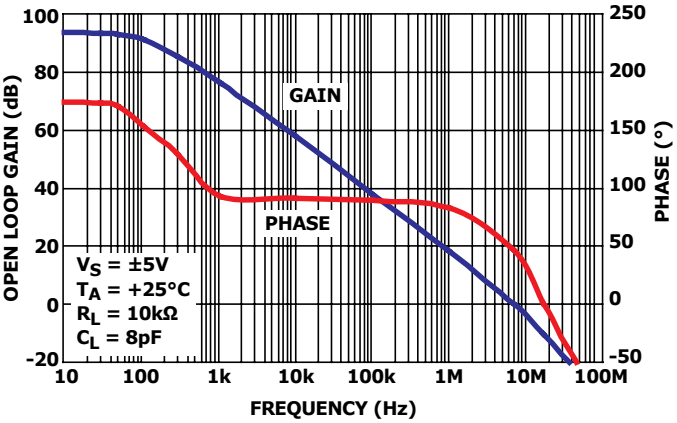


FIGURE 15. OPEN LOOP GAIN AND PHASE vs FREQUENCY

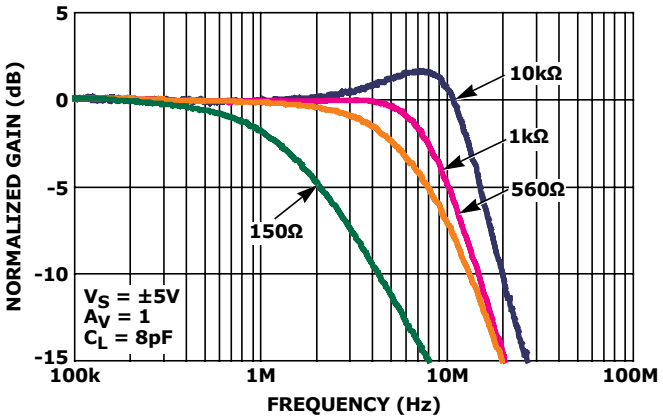


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS R_L

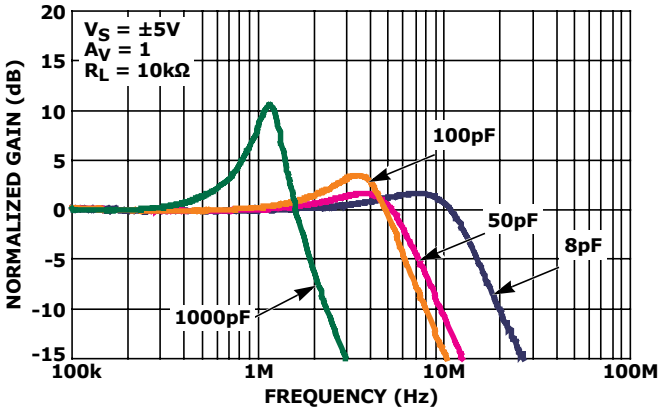


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS C_L

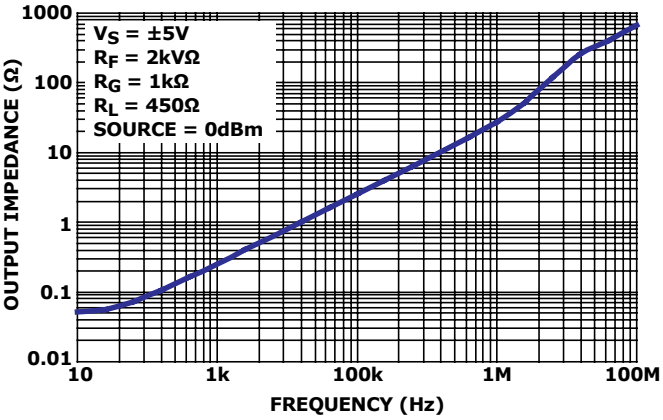


FIGURE 18. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

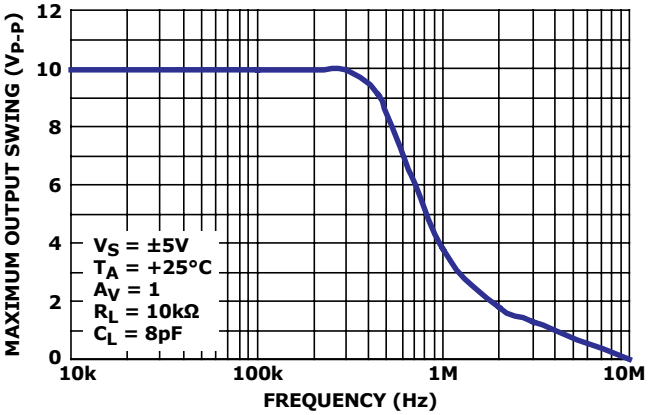


FIGURE 19. MAXIMUM OUTPUT SWING vs FREQUENCY

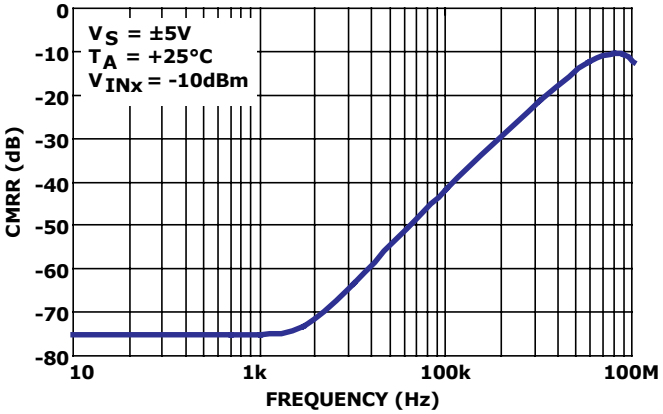


FIGURE 20. CMRR vs FREQUENCY

Typical Performance Curves (Continued)

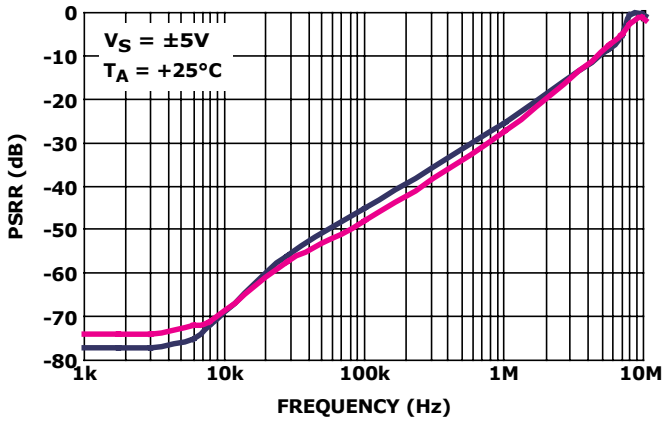


FIGURE 21. PSRR vs FREQUENCY

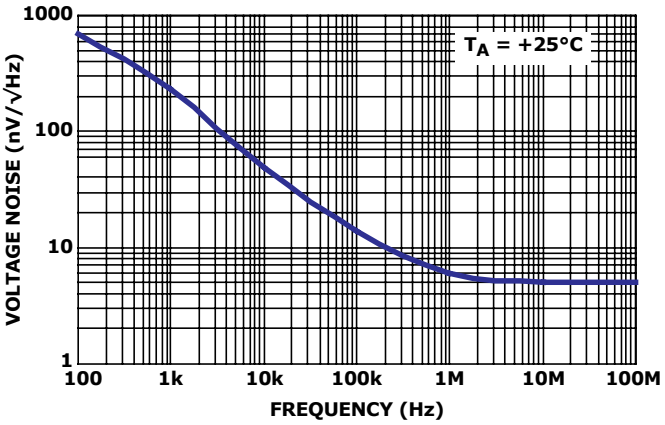


FIGURE 22. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

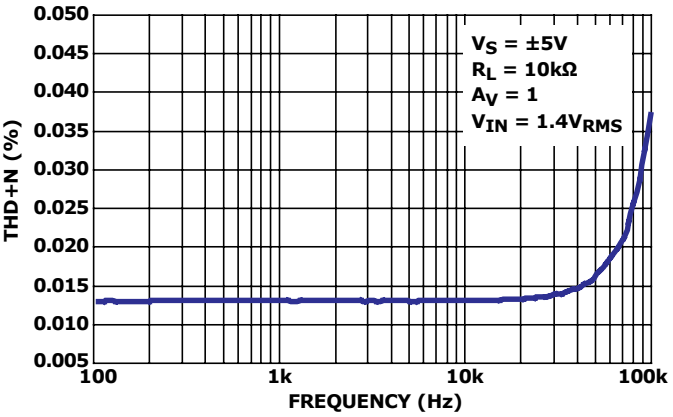


FIGURE 23. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

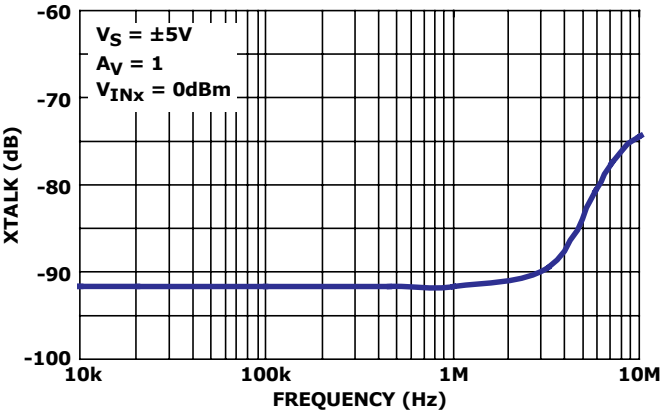


FIGURE 24. CHANNEL SEPARATION vs FREQUENCY RESPONSE

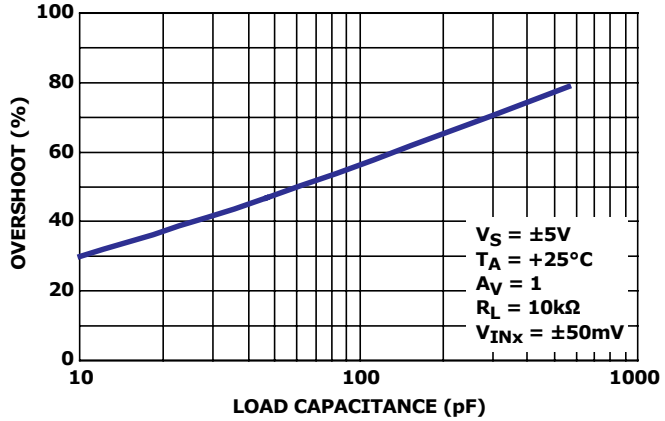


FIGURE 25. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

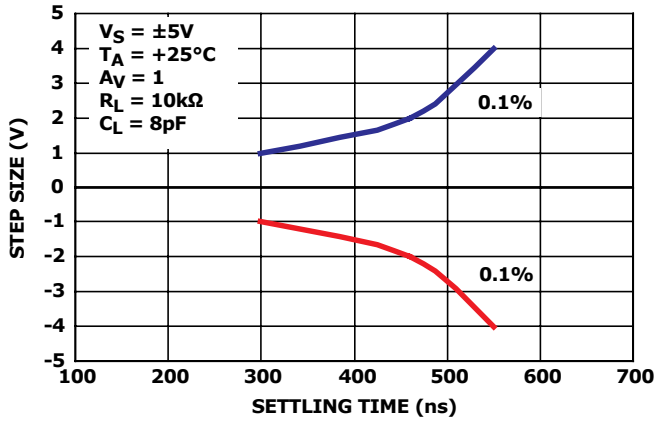


FIGURE 26. STEP SIZE vs SETTLING TIME

Typical Performance Curves (Continued)

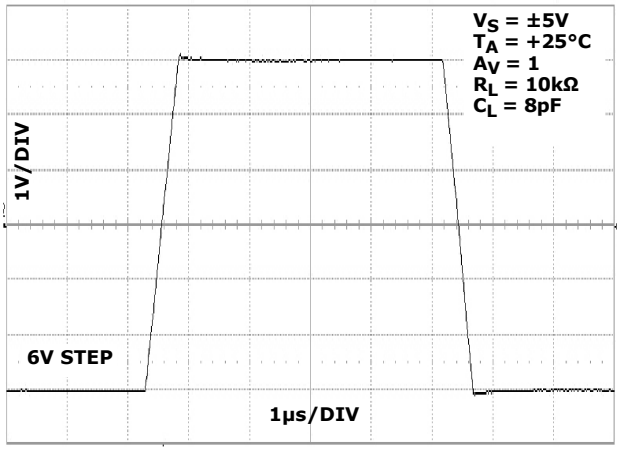


FIGURE 27. LARGE SIGNAL TRANSIENT RESPONSE

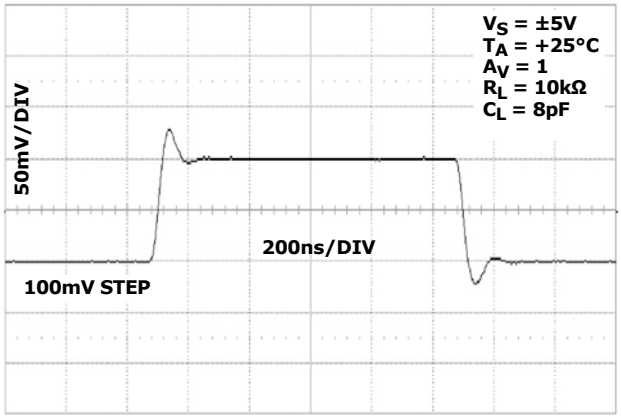


FIGURE 28. SMALL SIGNAL TRANSIENT RESPONSE

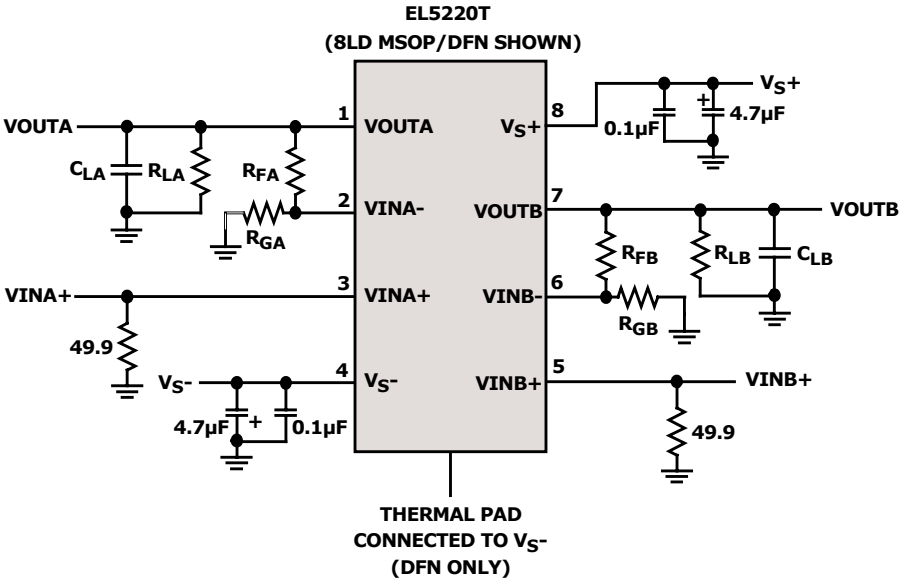


FIGURE 29. BASIC TEST CIRCUIT

Applications Information

Product Description

The EL5220T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5220T contains two amplifiers. Each amplifier exhibits beyond the rail input capability, rail-to-rail output capability, and is unity gain stable.

The EL5220T features a slew rate of 12V/µs. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the amplifiers to offer maximum dynamic range at any supply voltage.

Operating Voltage, Input and Output Capability

The EL5220T can operate on a single supply or dual supply configuration. The EL5220T operating voltage ranges from a minimum of 4.5V to a maximum of 19V. This range allows for a standard 5V (or ±2.5V) supply voltage to dip to -10%, or a standard 18V (or ±9V) to rise by +5.5% without affecting performance or reliability.

The input common-mode voltage range of the EL5220T extends 500mV beyond the supply rails. Also, the EL5220T is immune to phase reversal. However, if the common mode input voltage exceeds the supply voltage by more than 0.5V, electrostatic protection diodes in the input stage of the device begin to conduct. Even though phase reversal will not occur, to maintain optimal reliability it is suggested to avoid input overvoltage conditions. Figure 30 shows the input voltage driven 500mV beyond the supply rails and the device output swinging between the supply rails.

The EL5220T output typically swings to within 50mV of positive and negative supply rails with load currents of ±5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 31 shows the input and output waveforms for the device in a unity-gain configuration. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid and the output voltage is approximately $9.9V_{P-P}$.

Refer to the "Electrical Specifications" Table beginning on page 3 for specific device parameters. Parameter variations with operating voltage, loading and/or temperature are shown in the "Typical Performance Curves" on page 6.

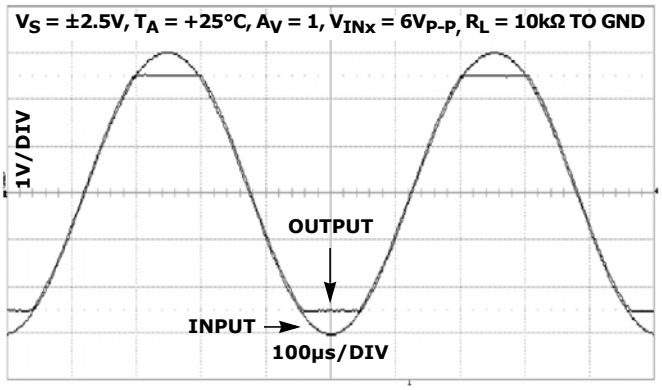


FIGURE 30. OPERATION WITH BEYOND-THE-RAILS INPUT

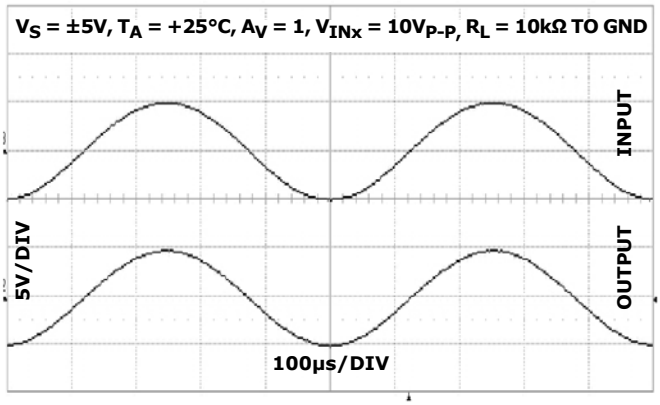


FIGURE 31. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Output Current

The EL5220T is capable of output short circuit currents of 200mA (source and sink), and the device has built-in protection circuitry which limits the output current to ±200mA (typical).

To maintain maximum reliability the continuous output current should never exceed ±65mA. This ±65mA limit is determined by the characteristics of the internal metal interconnects. Also, see "Power Dissipation" on page 12 for detailed information on ensuring proper device operation and reliability for temperature and load conditions.

Unused Amplifiers

It is recommended that any unused amplifiers be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground.

Thermal Shutdown

The EL5220T has a built-in thermal protection which ensures safe operation and prevents internal damage to the device due to overheating. When the die temperature reaches +165°C (typical) the device automatically shuts OFF the outputs by putting them in a high impedance state. When the die cools by +15°C

(typical) the device automatically turns ON the outputs by putting them in a low impedance (normal) operating state.

Driving Capacitive Loads

As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it may be necessary to reduce peaking and to improve device stability. To improve device stability, a snubber circuit or a series resistor may be added to the output of the EL5220T.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the phase margin and the stability of the EL5220T. The advantage of a snubber circuit is that it does not draw any DC load current or reduce the gain.

Another method to reduce peaking is to add a series output resistor (typically between 1Ω to 10Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

Power Dissipation

With the high-output drive capability of the EL5220T amplifiers, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. It is important to calculate the maximum power dissipation of the EL5220T in the application. Proper load conditions will ensure that the EL5220T junction temperature stays within a safe operating region.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation allowed

The total power dissipation produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power dissipation in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S+ - V_{OUT}i) \times I_{LOAD}i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S-) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking, where:

- i = 1 to 2
  (1, 2 corresponds to Channel A, B respectively)
- V_S = Total supply voltage (V_S+ - V_S-)
- V_S+ = Positive supply voltage
- V_S- = Negative supply voltage
- I_{SMAX} = Maximum supply current per amplifier (I_{SMAX} = EL5220T quiescent current ÷ 2)
- V_{OUT} = Output voltage
- I_{LOAD} = Load current

Device overheating can be avoided by calculating the minimum resistive load condition, R_{LOAD}, resulting in the highest power dissipation. To find R_{LOAD} set the two P_{DMAX} equations equal to each other and solve for V_{OUT}/I_{LOAD}. Reference the package power dissipation curves, Figures 32 and 33, for further information.

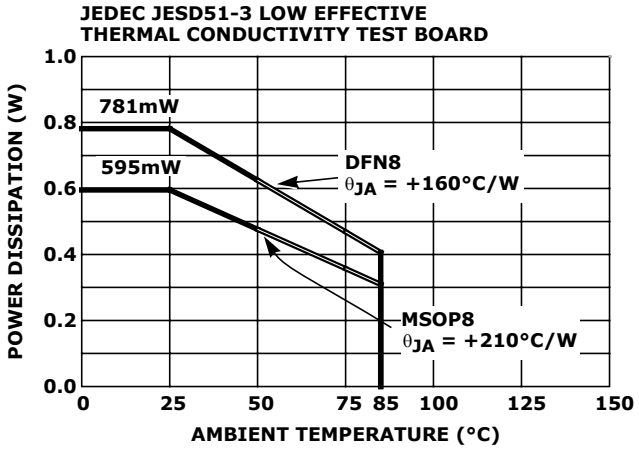


FIGURE 32. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

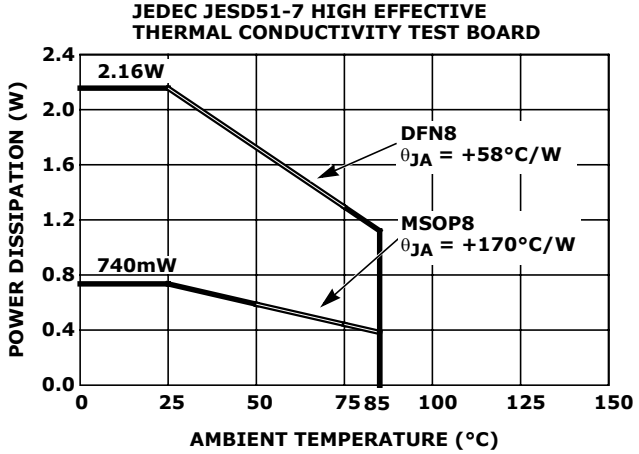


FIGURE 33. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Power Supply Bypassing and Printed Circuit Board Layout

The EL5220T can provide gain at high frequency, so good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, trace lengths should be as short as possible and the power supply pins must be well bypassed to reduce any risk of oscillation.

For normal single supply operation (the V_S- pin is connected to ground) a 4.7µF capacitor should be placed from V_S+ to ground, then a parallel 0.1µF capacitor should be connected as close to the amplifier as possible. One 4.7µF capacitor may be used for multiple devices. For dual supply operation the same capacitor combination should be placed at each supply pin to ground.

It is highly recommended that EL5220T exposed thermal pad packages should always have the pad connected to the lowest potential, V_S-, to optimize thermal and operating performance. PCB vias should be placed below the device's exposed thermal pad to transfer heat to the V_S- plane and away from the device.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/4/10	FN6892.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: EL5220T

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

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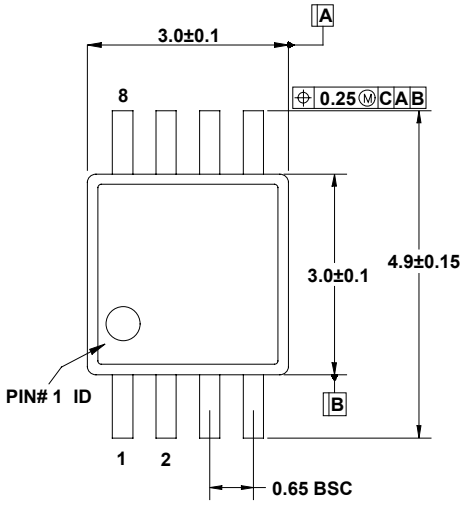
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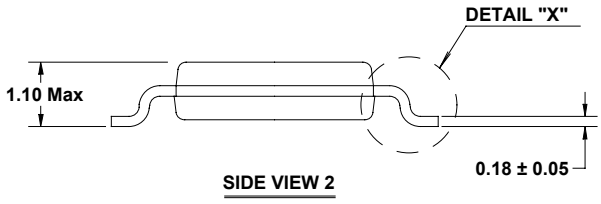
Package Outline Drawing

M8.118A

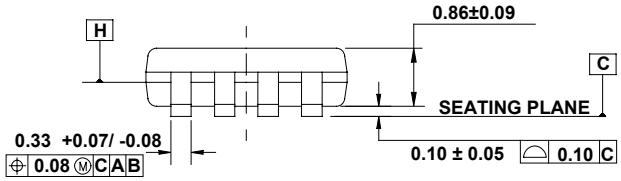
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



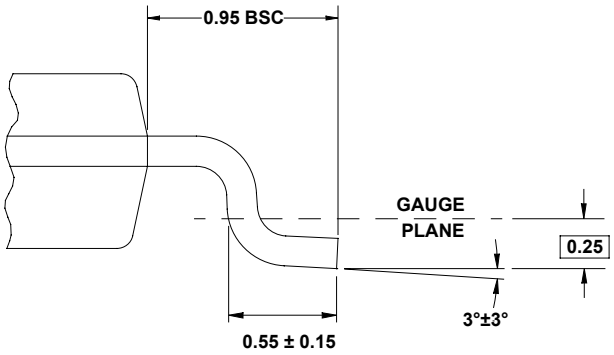
TOP VIEW



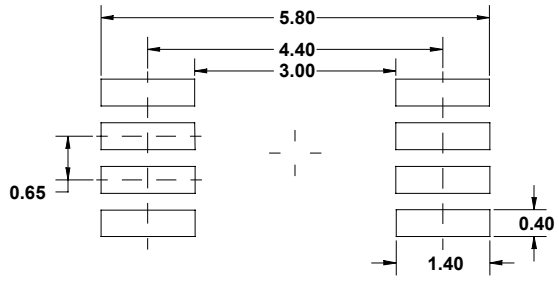
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

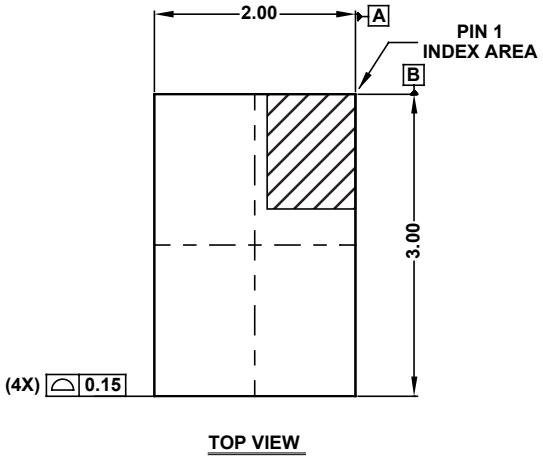
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

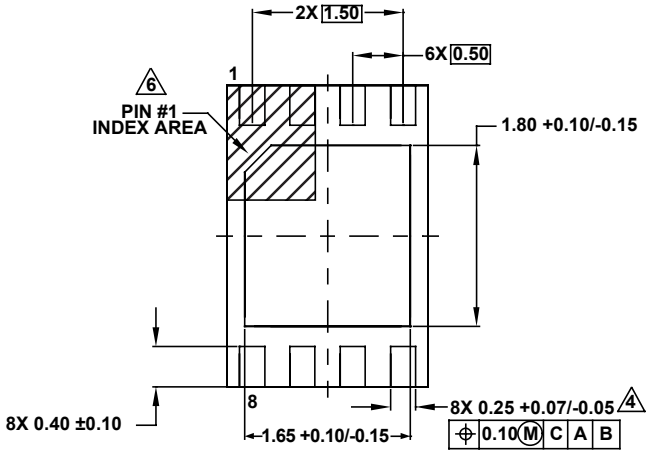
Package Outline Drawing

L8.2x3

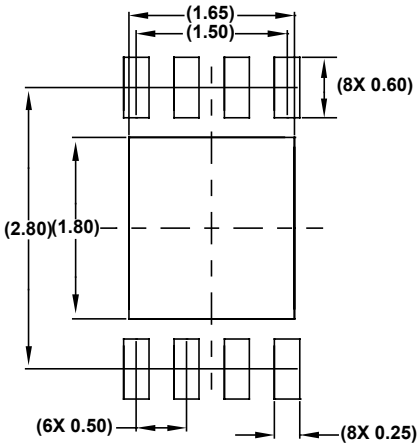
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



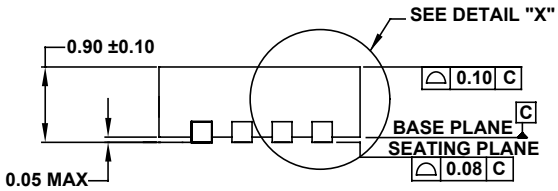
TOP VIEW



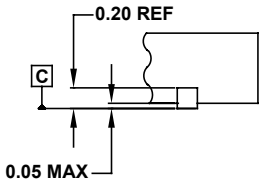
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compies to JEDEC MO-229 VCED-2.