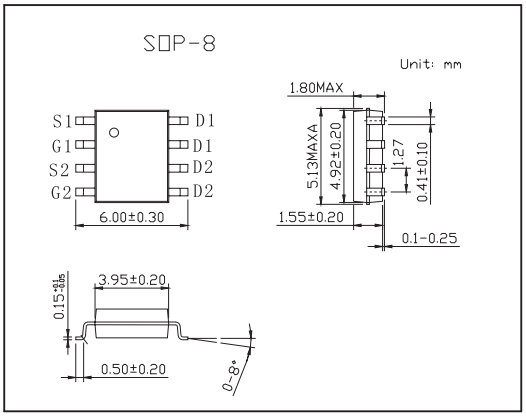
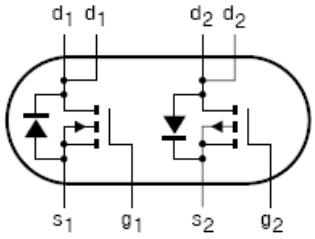
Complementary Enhancement Mode MOS Transistors KHC2300



■ Features

- High-speed switching
- No secondary breakdown.



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage	V_{DSS}	300	-300	V
Gate to Source Voltage	V_{GS}	±20	±20	V
Drain Current Ts = 80℃ *1	I_D	340	-235	A
peak drain current *2	I_{DM}	14	-0.9	A
total power dissipation Ts = 80℃; *3	P_{tot}	1.6		W
T_{amb} = 25 ℃; * 4		1.8		
T_{amb} = 25℃; * 5		0.9		
T_{amb} = 25 ℃; *6		1.2		
storage temperature	T_{stg}	-55 to 150		℃
operating junction temperature	T_j	-55 to 150		℃
thermal resistance from junction to soldering point	$R_{th\ j\text{-}s}$	43		K/W

*1. Ts is the temperature at the soldering point of the drain leads.

*2. Pulse width and duty cycle limited by maximum junction temperature.

*3. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 1.6 W at the same time).

*4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an Rth a-tp (ambient to tie-point) of 27.5 K/W.

*5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

*6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

KHC2300

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Type	Min	Typ	Max	Unit
drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0; I_D = 10 μA	N-Ch	300			V
		V_{GS} = 0; I_D = -10 μA	P-Ch	-300			V
gate-source threshold voltage	V_{GSth}	V_{GS} = V_{DS}; I_D = 1 mA	N-Ch	0.8		2	V
		V_{GS} = V_{DS}; I_D = -1 mA	P-Ch	-0.8		-2	V
drain-source leakage current	I_{DSS}	V_{GS} = 0; V_{DS} = 240 V	N-Ch			100	nA
		V_{GS} = 0; V_{DS} = -240 V	P-Ch			-100	nA
gate leakage current	I_{GSS}	V_{GS} = ±20 V; V_{DS} = 0	N-Ch			±100	nA
			P-Ch			±100	nA
drain-source on-state resistance	R_{DSon}	V_{GS} = 10 V; I_D = 170m A	N-Ch			8	Ω
		V_{GS} = -10 V; I_D = -115m A	P-Ch			17	Ω
input capacitance	C_{iss}	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	N-Ch		57		pF
		V_{GS} = 0; V_{DS} = -50 V; f = 1 MHz	P-Ch		45		pF
output capacitance	C_{oss}	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	N-Ch		15		pF
		V_{GS} = 0; V_{DS} = -50 V; f = 1 MHz	P-Ch		15		pF
reverse transfer capacitance	C_{rss}	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	N-Ch		2.6		pF
		V_{GS} = 0; V_{DS} = -50 V; f = 1 MHz	P-Ch		3		pF
total gate charge	Q_G	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170m A	N-Ch		2097		nC
		V_{GS} = 10 V; V_{DS} = -50 V; I_D =-115m A	P-Ch		2137		nC
gate-source charge	Q_{GS}	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170m A	N-Ch		75		nC
		V_{GS} = -10 V; V_{DS} = -50 V; I_D = -115m A	P-Ch		68		nC
gate-drain charge	Q_{GD}	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170m A	N-Ch		527		nC
		V_{GS} = -10 V; V_{DS} = -50 V; I_D = -115m A	P-Ch		674		nC
turn-on time	t_{on}	V_{GS} =0 to 10 V; V_{DD}=50V;I_D=170mA	N-Ch		2.5	10	ns
		V_{GS} = 0 to -10 V; V_{DD} = -50 V;I_D = -115mA	P-Ch		4	10	ns
turn-off time	t_{off}	V_{GS}=10 to 0 V;V_{DD}=50V;I_D=170mA	N-Ch		17	30	ns
		V_{GS}=-10 to 0 V;V_{DD}=-50V;I_D=-115mA	P-Ch		25	35	ns