

LM4051-N 精密低功耗并联电压基准

1 特性

- 无需输出电容器
- 能够承受电容负荷
- 1.225V 的反向击穿电压选项且可调节
- 主要规格：
 - 输出电压容差（A 级，25℃）± 0.1%（最大值）
 - 输出噪声（10Hz 至 10kHz）20μV rms
 - 工作电流范围：60μA 至 12mA
 - 工业温度范围：-40℃ 至 +85℃
 - 扩展温度范围：-40℃ 至 +125℃
 - 温度系数：50ppm/℃（最大值）

2 应用

- 便携式、电池供电类设备
- 数据采集系统
- 仪表
- 工艺控制
- 能源管理
- 汽车和工业
- 精密音频组件
- 基站
- 电池充电器
- 医疗设备
- 通信

3 说明

LM4051-N 精密电压基准非常适合空间关键型应用，可采用超小型 (3mm x 1.3mm) SOT-23 表面贴装封装。LM4051-N 采用了先进的设计，无需使用外部稳定电容器，同时可确保任何电容负荷下的稳定性，这使得 LM4051-N 非常易于使用。它还提供了固定 (1.225V) 和可调节反向击穿电压，可帮助设计人员进一步减少设计工作。LM4051-1.2 和 LM4051-ADJ 的最低工作电流为 60μA。两个版本都具有 12mA 的最高工作电流。

LM4051-N 具有三种级别（A、B 和 C）。最佳级别器件 (A) 的初始精度为 0.1%，而 B 级的初始精度为 0.2%，C 级的初始精度为 0.5%，所有级别的温度系数均为 50 ppm/℃，保证范围为 -40℃ 至 125℃。

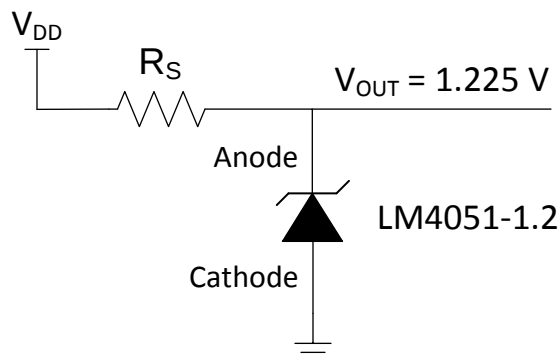
LM4051-N 在晶圆筛选期间使用了保险丝和基准电压齐纳击穿修整，以确保主要部件在 25℃ 下的精度优于 ± 0.1%（A 级）。

器件信息⁽¹⁾

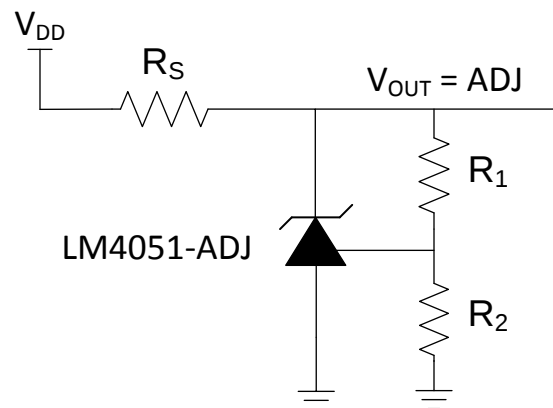
器件编号	封装	封装尺寸（标称值）
LM4051-N	SOT-23 (3)	3.00mm x 1.30mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

1.2 V_{REF} 简化原理图



可调基准简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

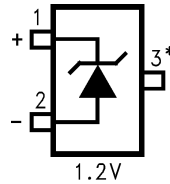
Changes from Revision C (March 2005) to Revision D

Page

- 添加了器件信息表、器件比较表、ESD 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。 **1**

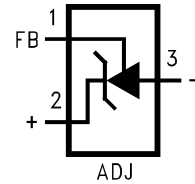
5 Pin Configuration and Functions

DBZ Package
1.2-V, 3-Pin SOT-23
Top View



* This pin must be left floating or connected to pin 2.

DBZ Package
Adjustable, 3-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	1.2 V	ADJ		
Anode	2	3	O	Shunt Current/Voltage input
Cathode	1	2	I/O	Common pin, normally connected to ground
NC	3	-	-	Must float or connect to anode
FB	-	1	I	Threshold relative to cathode

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Reverse current		20	mA
Forward current		10	mA
Maximum output voltage (LM4051-ADJ)		15	V
Power dissipation (T _A = 25°C) ⁽²⁾ M3 package		280	mW
Lead temperature M3 packages	Vapor phase (60 seconds)		215
	Infrared (15 seconds)		220
Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A) / θ_{JA} or the number given in the *Absolute Maximum Ratings*, whichever is lower. For the LM4051-N, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 280°C/W for the SOT-23 package.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾⁽²⁾	±2000
	Machine model (MM) ⁽³⁾	200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (3) The machine model is a 200-pF capacitor discharged directly into each pin.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature ($T_{\min} \leq T_A \leq T_{\max}$)	Industrial temperature	–40		85	°C
	Extended temperature	–40		125	
Reverse current	LM4051-1.2	0.06		12	mA
	LM4051-ADJ	0.06		12	
Output voltage	LM4051-ADJ	1.24		10	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM4051-ADJ, LM4051-1.2 V	UNIT
		DBZ	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 LM4051-1.2 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_R	Reverse Breakdown Voltage	$I_R = 100 \mu A$			1.225		V
	Reverse Breakdown Voltage Tolerance ⁽¹⁾	$I_R = 100 \mu A$	LM4051AIM3 ⁽²⁾			±1.2	mV
			LM4051BIM3 LM4051BEM3 ⁽²⁾			±2.4	
			LM4051CIM3 ⁽²⁾			±6	
		Industrial Temp. Range $T_A = T_J = T_{\min}$ to $T_{\max}$	LM4051AIM3 ⁽²⁾			±5.2 ⁽¹⁾	
			LM4051BIM3 ⁽²⁾			±6.4 ⁽¹⁾	
			LM4051CIM3 ⁽²⁾			±10.1 ⁽¹⁾	
		Extended Temp. Range $T_A = T_J = T_{\min}$ to $T_{\max}$	LM4051BEM3 ⁽²⁾			±8.6 ⁽¹⁾	
I_{RMIN}	Minimum Operating Current	$T_J = 25^\circ C$			39		μA
		Industrial Temp. Range $T_A = T_J = T_{\min}$ to $T_{\max}$				65	
		Extended Temp. Range $T_A = T_J = T_{\min}$ to $T_{\max}$				70	

- (1) This overtemperature limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance $\pm [(\Delta V_R / \Delta T)(\max \Delta T)(V_R)]$. Where, $\Delta V_R / \Delta T$ is the VR temperature coefficient, $\max \Delta T$ is the maximum difference in temperature from the reference point of $25^\circ C$ to $T_{\max}$ or $T_{\min}$, and V_R is the reverse breakdown voltage. The total overtemperature tolerance for the different grades in the industrial temperature range where $\max \Delta T = 65^\circ C$ is shown below:
- (a) A-grade: $\pm 0.425\% = \pm 0.1\% \pm 50 \text{ ppm}/^\circ C \times 65^\circ C$
(b) B-grade: $\pm 0.525\% = \pm 0.2\% \pm 50 \text{ ppm}/^\circ C \times 65^\circ C$
(c) C-grade: $\pm 0.825\% = \pm 0.5\% \pm 50 \text{ ppm}/^\circ C \times 65^\circ C$
Therefore, as an example, the A-grade LM4051-1.2 has an over-temperature Reverse Breakdown Voltage tolerance of $\pm 1.2V \times 0.425\% = \pm 5.2 \text{ mV}$.
- (2) Limits are 100% production tested at $25^\circ C$. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

LM4051-1.2 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient ⁽¹⁾	$I_R = 10 \text{ mA}$			± 20		ppm/°C
		$I_R = 1 \text{ mA}$			± 15		
		$I_R = 100 \text{ }\mu\text{A}$ $\Delta T = -40^\circ\text{C to } 125^\circ\text{C}$	$T_J = 25^\circ\text{C}$		± 15		
			$T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$			$\pm 50^{(1)}$	
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{\text{RMIN}} \leq I_R \leq 1 \text{ mA}$	$T_J = 25^\circ\text{C}$		0.3		mV
			Industrial Temp. Range $T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$			1.1 ⁽¹⁾	
			Extended Temp. Range $T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$			1.5 ⁽¹⁾	
		$1 \text{ mA} \leq I_R \leq 12 \text{ mA}$	$T_J = 25^\circ\text{C}$		1.8		
			Industrial Temp. Range $T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$			6 ⁽¹⁾	
			Extended Temp. Range $T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$			8 ⁽¹⁾	
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}, f = 120 \text{ Hz}$			0.5		Ω
e_N	Wideband Noise	$I_R = 100 \text{ }\mu\text{A}$ $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$			20		μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability ⁽³⁾	$t = 1000 \text{ hrs}, T = 25^\circ\text{C} \pm 0.1^\circ\text{C}, I_R = 100 \text{ }\mu\text{A}$			120		ppm
V_{HYS}	Thermal Hysteresis ⁽⁴⁾	$\Delta T = -40^\circ\text{C to } 125^\circ\text{C}$			0.36		mV/V

(3) Long-term stability is V_R at 25°C measured during 1000 hrs.

(4) Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ\text{C}$ after cycling to temperature -40°C and the 25°C measurement after cycling to temperature $+125^\circ\text{C}$.

6.6 LM4051-ADJ Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$I_R = 100 \text{ }\mu\text{A}, V_{\text{OUT}} = 5 \text{ V}$			1.212		V
	Reference Voltage Tolerance ⁽¹⁾⁽²⁾	$I_R = 100 \text{ }\mu\text{A}, V_{\text{OUT}} = 5 \text{ V}$	LM4051AIM3 ⁽³⁾			± 1.2	mV
			LM4051BIM3 ⁽³⁾			± 2.4	
			LM4051CIM3 ⁽³⁾			± 6	
		Industrial Temp. Range $T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$	LM4051AIM3 ⁽³⁾			± 5.2	
			LM4051BIM3 ⁽³⁾			± 6.4	
			LM4051CIM3 ⁽³⁾			± 10.1	

(1) This overtemperature limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance $\pm [(\Delta V_R/\Delta T)(\text{max}\Delta T)(V_R)]$. Where, $\Delta V_R/\Delta T$ is the V_R temperature coefficient, $\text{max}\Delta T$ is the maximum difference in temperature from the reference point of 25°C to T_{MAX} or T_{MIN} , and V_R is the reverse breakdown voltage. The total overtemperature tolerance for the different grades in the industrial temperature range where $\text{max}\Delta T = 65^\circ\text{C}$ is shown below:

(a) A-grade: $\pm 0.425\% \pm 0.1\% \pm 50 \text{ ppm}/^\circ\text{C} \times 65^\circ\text{C}$

(b) B-grade: $\pm 0.525\% \pm 0.2\% \pm 50 \text{ ppm}/^\circ\text{C} \times 65^\circ\text{C}$

(c) C-grade: $\pm 0.825\% \pm 0.5\% \pm 50 \text{ ppm}/^\circ\text{C} \times 65^\circ\text{C}$

Therefore, as an example, the A-grade LM4051-1.2 has an overtemperature Reverse Breakdown Voltage tolerance of $\pm 1.2 \text{ V} \times 0.425\% \pm 5.2 \text{ mV}$.

(2) Reference voltage and temperature coefficient will change with output voltage. See [Typical Characteristics](#) curves.

(3) Limits are 100% production tested at 25°C . Limits over temperature are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

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LM4051-ADJ Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{RMIN} Minimum Operating Current	LM4051AIM3 ⁽⁴⁾			36		μA
	LM4051BIM3 ⁽⁴⁾			36		
	LM4051CIM3 ⁽⁴⁾			36		
	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}	LM4051AIM3 ⁽³⁾		60		
		LM4051BIM3 ⁽³⁾		60		
		LM4051CIM3 ⁽³⁾		65		
$\Delta V_{REF}/\Delta I_R$ Reference Voltage Change with Operating Current Change	$I_{RMIN} \leq I_R \leq 1$ mA $V_{OUT} \geq 1.6$ V ⁽⁵⁾	$T_J = 25^\circ C$		0.3		mV
		Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		1.1 ⁽¹⁾		
	1 mA $\leq I_R \leq 12$ mA $V_{OUT} \geq 1.6$ V ⁽⁵⁾	$T_J = 25^\circ C$		0.6		
		Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		6 ⁽¹⁾		
$\Delta V_{REF}/\Delta V_O$ Reference Voltage Change with Output Voltage Change	$I_R = 0.1$ mA	$T_J = 25^\circ C$		-1.69		mV
		Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		-2.8 ⁽¹⁾		
I_{FB} Feedback Current				70	130	nA
$\Delta V_{REF}/\Delta T$ Average Reference Voltage Temperature Coefficient (Note 8)	$V_{OUT} = 2.5$ V $\Delta T = -40^\circ C$ to $+125^\circ C$	$I_R = 10$ mA	$T_J = 25^\circ C$	20		ppm/ $^\circ C$
			Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}	± 50 ⁽¹⁾		
		$I_R = 1$ mA	$T_J = 25^\circ C$	15		
			Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}	± 50 ⁽¹⁾		
		$I_R = 100$ μA	$T_J = 25^\circ C$	15		
			Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}	± 50 ⁽¹⁾		
Z_{OUT} Dynamic Output Impedance	$I_R = 1$ mA, $f = 120$ Hz, $I_{AC} = 0.1$ I_R	$V_{OUT} = V_{REF}$		0.3		Ω
		$V_{OUT} = 10$ V		2		
e_N Wideband Noise	$I_R = 100$ μA , $V_{OUT} = V_{REF}$, 10 Hz $\leq f \leq 10$ kHz			20		μV_{rms}
ΔV_{REF} Reference Voltage Long Term Stability ⁽⁶⁾	$t = 1000$ hrs, $I_R = 100$ μA , $T = 25^\circ C \pm 0.1^\circ C$			120		ppm
V_{HYST} Thermal Hysteresis ⁽⁷⁾	$\Delta T = -40^\circ C$ to $+125^\circ C$			0.3		mV/V

(4) Limits are 100% production tested at $25^\circ C$. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

(5) When $V_{OUT} \leq 1.6$ V, the LM4051-ADJ in the SOT-23 package must operate at reduced I_R . This is caused by the series resistance of the die attach between the die (–) output and the package (–) output pin. See the Output Saturation curve in the [Typical Characteristics](#) section.

(6) Long-term stability is V_R at $25^\circ C$ measured during 1000 hrs.

(7) Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ C$ after cycling to temperature $-40^\circ C$ and the $25^\circ C$ measurement after cycling to temperature $+125^\circ C$.

6.7 Typical Characteristics

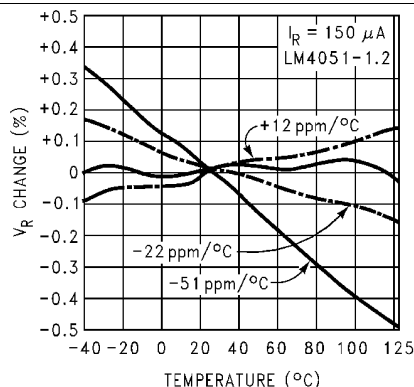


Figure 1. Temperature Drift for Different Average Temperature Coefficient

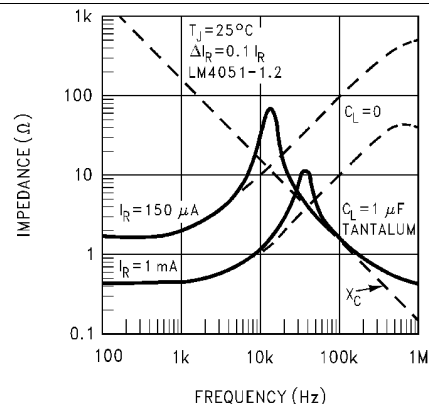


Figure 2. Output Impedance vs Frequency

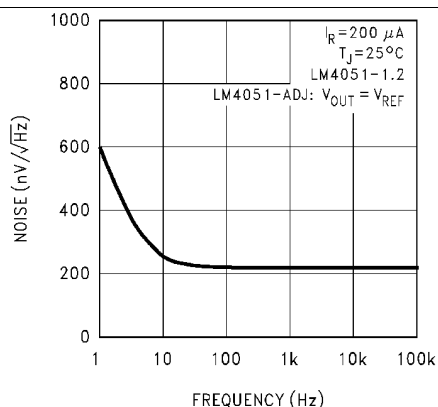


Figure 3. Noise Voltage

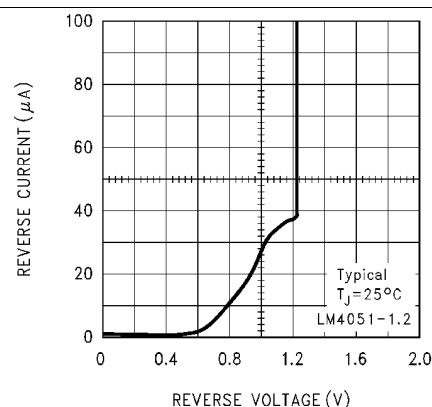


Figure 4. Reverse Characteristics and Minimum Operating Current

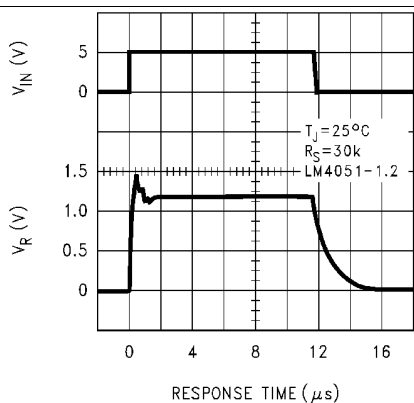


Figure 5. Start-Up Characteristics

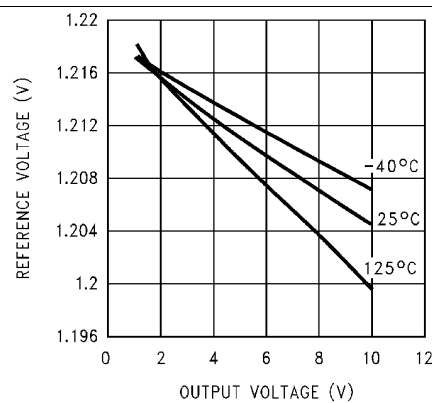


Figure 6. Reference Voltage vs Output Voltage and Temperature

Typical Characteristics (continued)

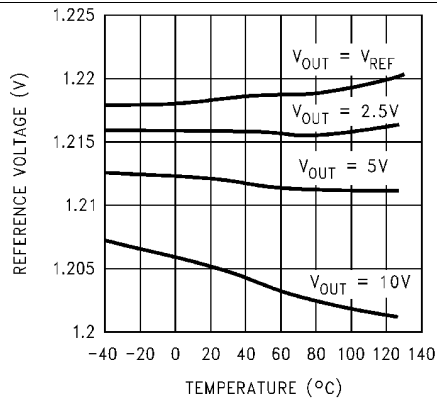


Figure 7. Reference Voltage vs Temperature and Output Voltage

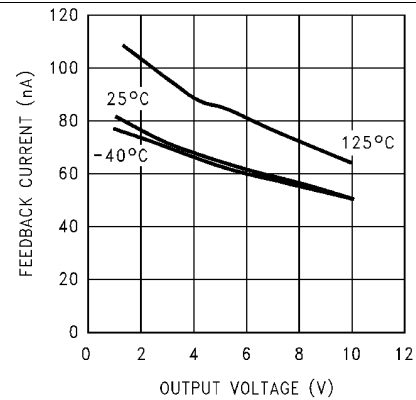


Figure 8. Feedback Current vs Output Voltage and Temperature

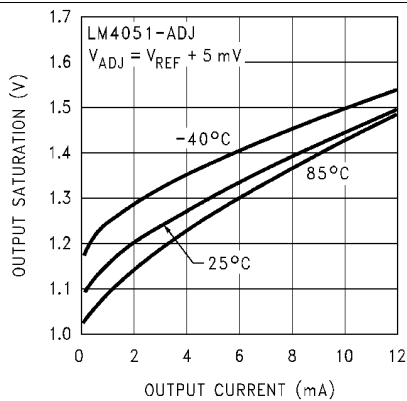


Figure 9. Output Saturation (SOT-23 Only)

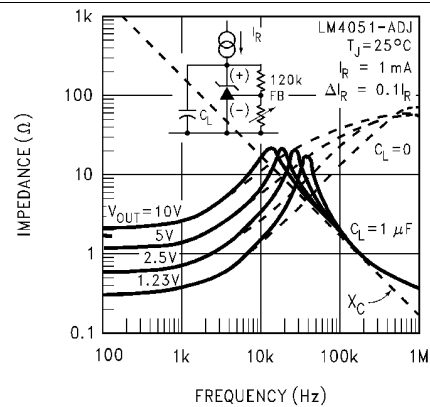


Figure 10. Output Impedance vs Frequency

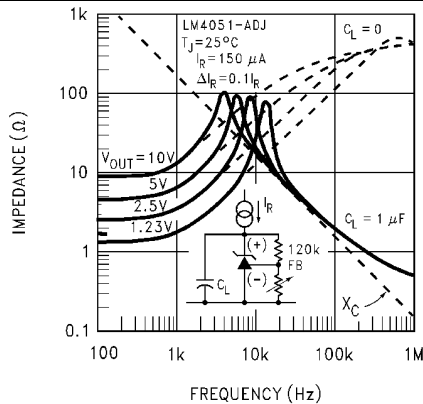


Figure 11. Output Impedance vs Frequency

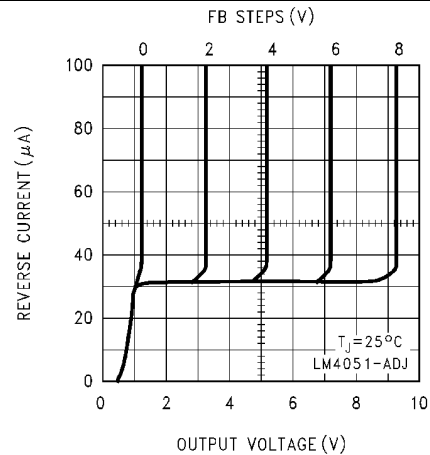


Figure 12. Reverse Characteristics

Typical Characteristics (continued)

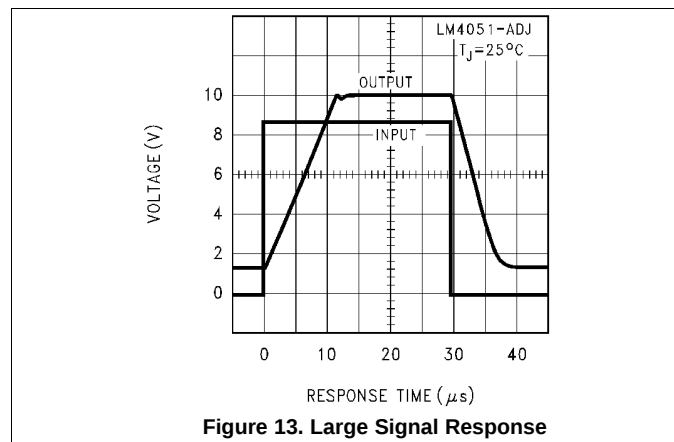


Figure 13. Large Signal Response

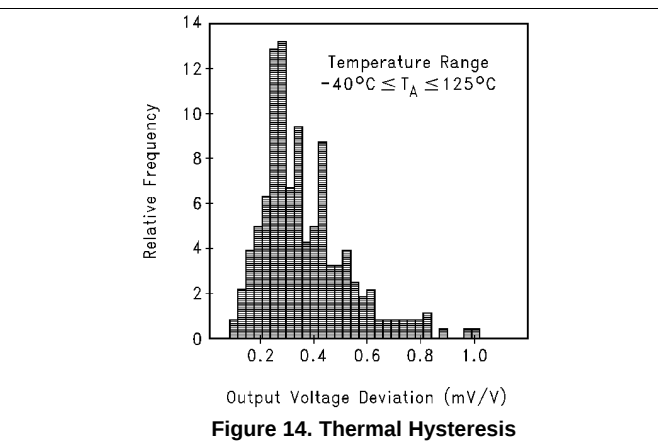


Figure 14. Thermal Hysteresis

7 Parameter Measurement Information

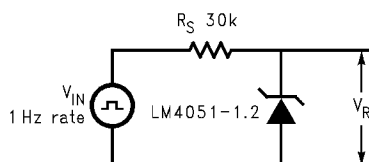


Figure 15. Test Circuit for Start-Up Characteristics

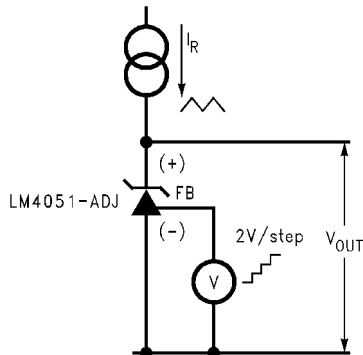


Figure 16. Test Circuit for Reverse Characteristics

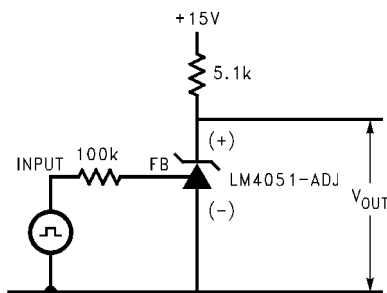


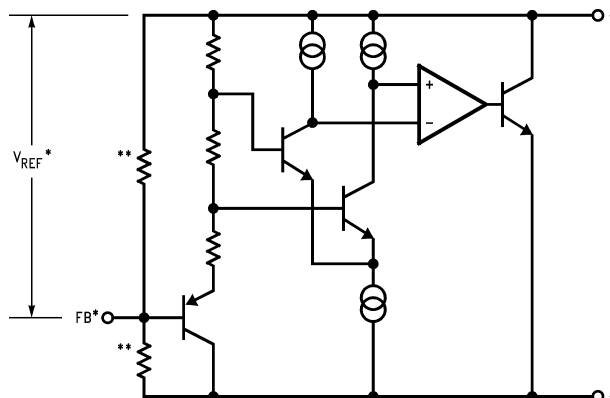
Figure 17. Test Circuit for Large Signal Response

8 Detailed Description

8.1 Overview

The LM4051-N is a precision voltage reference available in SOT-23 surface mount package. The LM4051-N is available in a 1.225 V fixed-option as well as an adjustable voltage option. The LM4051-N comes in three different tolerance grades (A, B, and C). The best grade devices (A) have an initial accuracy of 0.1%, while the B-grade have 0.2% and the C-grade 0.5%, all with a temperature coefficient of 50 ppm/°C guaranteed from -40°C to 125°C.

8.2 Functional Block Diagram



*LM4051-ADJ only

**LM4051-1.2 only

8.3 Feature Description

The LM4051-N device is effectively a precision Zener diode. The part requires a small quiescent current for regulation, and regulates the output voltage by shunting more or less current to ground, depending on input voltage and load. The only external component requirement is a resistor between the cathode and the input voltage to set the input current. An external capacitor can be used on the input or output, but is not required.

For the adjustable version, feedback is applied from the Cathode and Reference pins, the LM4051-N behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations in order for it to be in the proper linear region giving the LM4051-N enough gain.

8.4 Device Functional Modes

8.4.1 LM4051-N - 1.2 V

The LM4051-N - 1.2V device is a fixed output voltage part, where the feedback is internal. Therefore, the part can only operate in a closed loop mode and the output voltage cannot be adjusted. The output voltage will remain in regulation as long as I_R is between I_{RMIN} . Proper selection of the external resistor for input voltage range and load current range will ensure these conditions are met.

8.4.2 LM4051-N - ADJ

The majority of applications involving LM4051-N uses closed loop operation to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM4051-N is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4051-N is available in the sub-miniature SOT-23 surface-mount package. The LM4051-N has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "-" pin. If, however, a bypass capacitor is used, the LM4051-N remains stable. Design effort is further reduced with the choice of either a fixed 1.2-V or an adjustable reverse breakdown voltage. The minimum operating current is 60 μ A for the LM4051-1.2 and the LM4051-ADJ. Both versions have a maximum operating current of 12 mA.

LM4051-N's using the SOT-23 package have pin 3 connected as the (–) output through the package's die attach interface. Therefore, the LM4051-1.2's pin 3 must be left floating or connected to pin 2 and the LM4051-ADJ's pin 3 is the (–) output.

The typical thermal hysteresis specification is defined as the change in +25 °C voltage measured after thermal cycling. The device is thermal cycled to temperature –40 °C and then measured at 25 °C. Next the device is thermal cycled to temperature +125 °C and again measured at 25 °C. The resulting V_{OUT} delta shift between the 25 °C measurements is thermal hysteresis. Thermal hysteresis is common in precision references and is induced by thermal-mechanical package stress. Changes in environmental storage temperature, operating temperature and board mounting temperature are all factors that can contribute to thermal hysteresis.

In a conventional shunt regulator application ([Figure 18](#)), an external series resistor (R_S) is connected between the supply voltage and the LM4051-N. R_S determines the current that flows through the load (I_L) and the LM4051-N (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4051-N even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4051-N is less than 12 mA.

R_S should be selected based on the supply voltage, (V_S), the desired load and operating current, (I_L and I_Q), and the LM4051-N's reverse breakdown voltage, V_R .

$$R_S = \frac{V_S - V_R}{I_L + I_Q} \quad (1)$$

The LM4051-ADJ's output voltage can be adjusted to any value in the range of 1.24 V through 10 V. It is a function of the internal reference voltage (V_{REF}) and the ratio of the external feedback resistors as shown in [Figure 20](#). The output voltage is found using [Equation 2](#):

$$V_O = V_{REF} \left[\left(R_2 / R_1 \right) + 1 \right]$$

where

- V_O is the output voltage (2)

$$R_S = \frac{V_S - V_R}{I_L + I_Q + I_F} \quad (3)$$

The actual value of the internal V_{REF} is a function of V_O . The *corrected* V_{REF} is determined by [Equation 4](#):

$$V_{REF} = V_O (\Delta V_{REF} / \Delta V_O) + V_Y$$

where

- $V_Y = 1.22$ V (4)

Application Information (continued)

$\Delta V_{REF}/\Delta V_O$ is found in the [LM4051-ADJ Electrical Characteristics](#) and is typically -1.55 mV/V . You can get a more accurate indication of the output voltage by replacing the value of V_{REF} in [Equation 2](#) with the value found using [Equation 4](#).

9.2 Typical Applications

9.2.1 Shunt Regulator

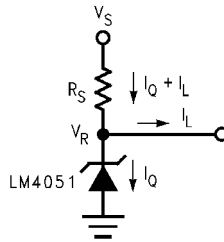


Figure 18. Shunt Regulator

9.2.1.1 Design Requirements

$$V_{IN} > V_{OUT}$$

Select R_S such that:

$$I_{R_{MIN}} < I_R < I_{R_{MAX}} \text{ where } I_{R_{MAX}} = 12 \text{ mA}$$

See [LM4051-1.2 Electrical Characteristics](#) for minimum operating current for each voltage option and grade.

9.2.1.2 Detailed Design Procedure

The resistor R_S must be selected such that current, I_R , will remain in the operational region of the part for the entire V_{IN} range and load current range. The two extremes to consider are V_{IN} at its maximum, and the load at its minimum, where R_S must be large enough to main $I_R < I_{R_{MAX}}$. For most designs, $0.1 \text{ mA} \leq I_R \leq 1 \text{ mA}$ is a good starting point.

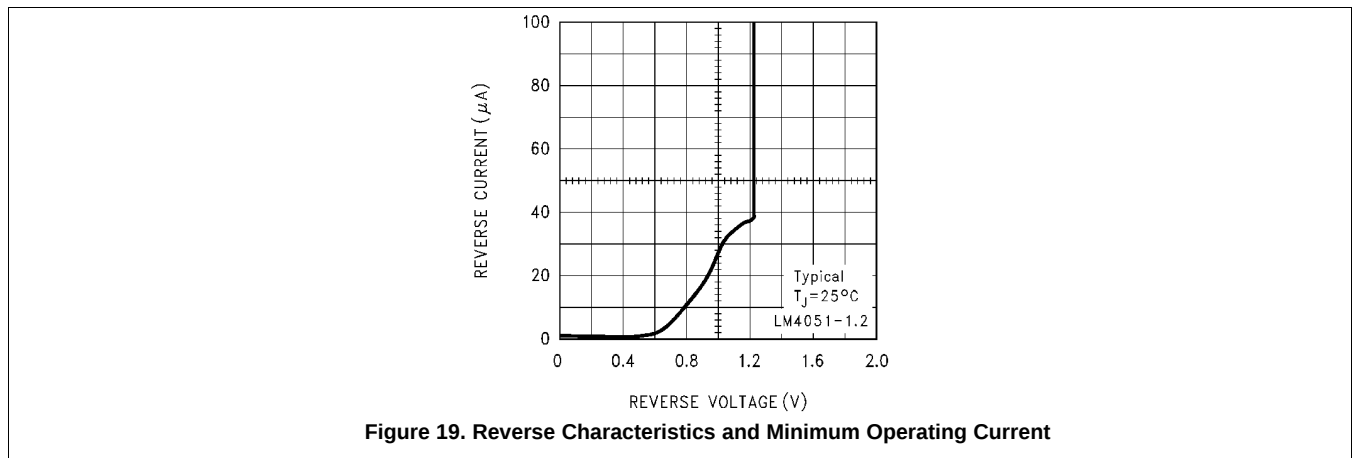
Use cross and cross to set R_S between R_{S_MIN} and R_{S_MAX} .

$$R_{S_MIN} = \frac{V_{IN_MAX} - V_{OUT}}{I_{LOAD_MIN} + I_{R_MAX}} \quad (5)$$

$$R_{S_MAX} = \frac{V_{IN_MIN} - V_{OUT}}{I_{LOAD_MAX} + I_{R_MIN}} \quad (6)$$

Typical Applications (continued)

9.2.1.3 Application Curves



9.2.2 Adjustable Shunt Regulator

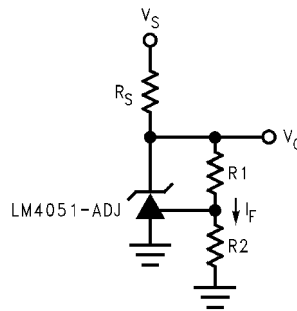


Figure 20. Adjustable Shunt Regulator

9.2.2.1 Design Requirements

$$V_{IN} > V_{OUT}$$

Select R_S such that:

$$I_{RMIN} < I_R < I_{RMAX} \text{ where } I_{RMAX} = 12 \text{ mA}$$

See [LM4051-ADJ Electrical Characteristics](#) for minimum operating current for each voltage option and grade.

9.2.2.2 Detailed Design Procedure

In order to program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in [Figure 20](#), with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in [Equation 7](#). The cathode voltage can be more accurately determined by taking in to account the cathode current shown in equation [Equation 8](#).

$$V_O = \left(1 + \frac{R1}{R2}\right) \times V_{REF} \quad (7)$$

$$V_O = \left(1 + \frac{R1}{R2}\right) \times (V_{REF} - I_{REF} \times R_1) \quad (8)$$

Typical Applications (continued)

In order for this equation to be valid, LM4051-ADJ must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the I_{RMIN} denoted in [LM4051-ADJ Electrical Characteristics](#).

9.3 System Examples

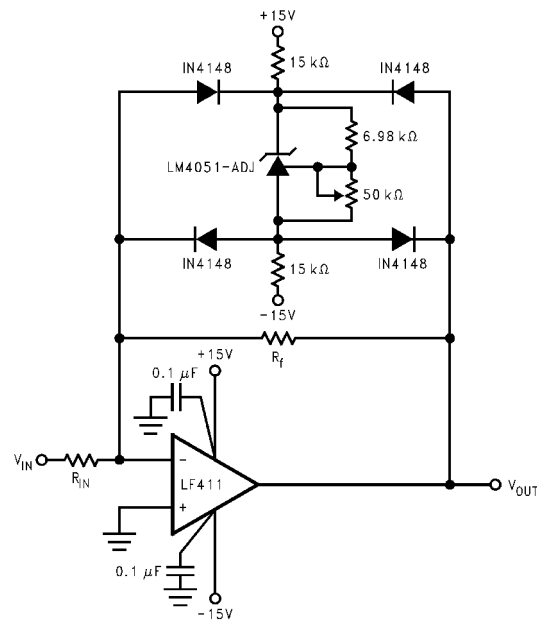


Figure 21. Bounded Amplifier Reduces Saturation-induced Delays and Can Prevent Succeeding Stage Damage. Nominal Clamping Voltage is $\pm V_O$ (LM4051-N's Reverse Breakdown Voltage) +2 Diode V_F .

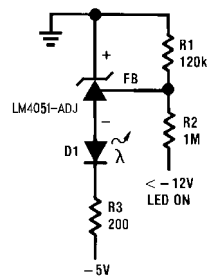


Figure 22. Voltage Level Detector

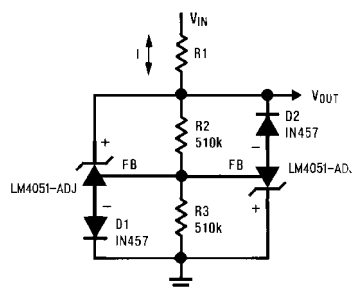


Figure 23. Voltage Level Detector

System Examples (continued)

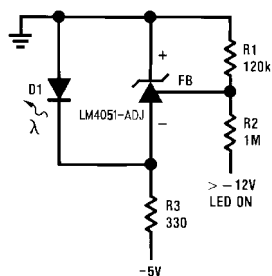


Figure 24. Fast Positive Clamp $2.4V + V_{D1}$

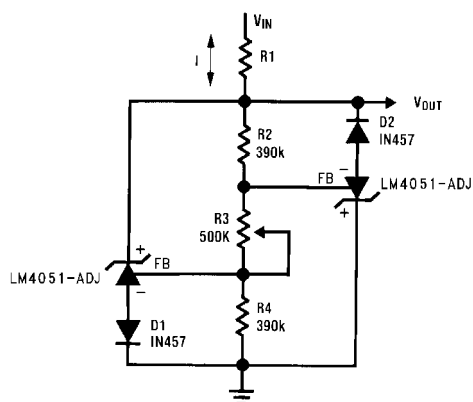


Figure 25. Bidirectional Clamp $\pm 2.4V$

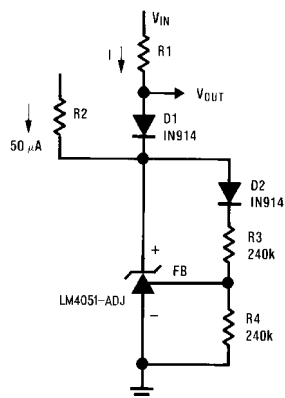


Figure 26. Bidirectional Adjustable Clamp $\pm 18V$ to $\pm 2.4V$

System Examples (continued)

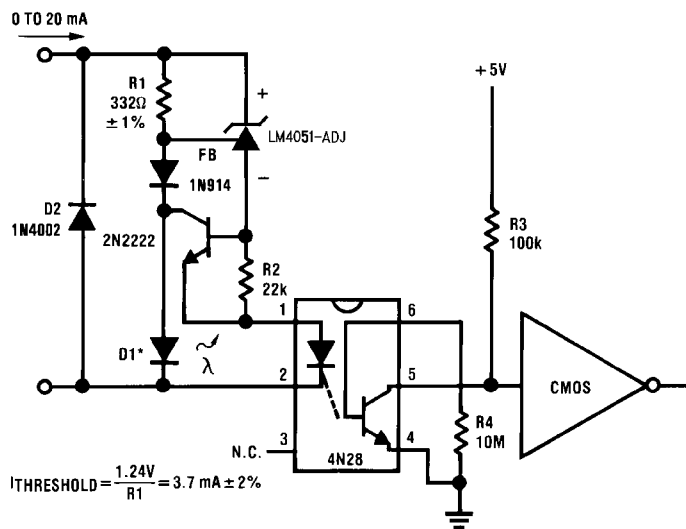


Figure 30. Precision Floating Current Detector

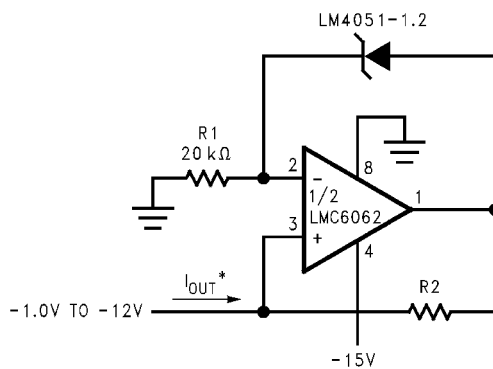


Figure 31. Precision 1 μA to 1 mA Current Source

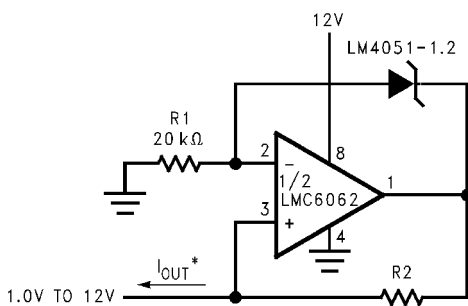


Figure 32. Precision 1 μA to 1 mA Current Source

10 Power Supply Recommendations

While a bypass capacitor is not required on the input voltage line, TI recommends reducing noise on the input which could affect the output. A 0.1- μF ceramic capacitor or larger is recommended.

In order to not exceed the maximum cathode current, be sure that the supply current is limited. For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have proper current density.

11 Layout

11.1 Layout Guidelines

Bypass capacitors should be placed as close to the device as possible. Current-carrying traces need to have widths appropriate for the amount of current they are carrying. Place R_S as close as possible to the cathode. Although not as critical, keep feedback resistor close to the device whenever possible.

11.2 Layout Example

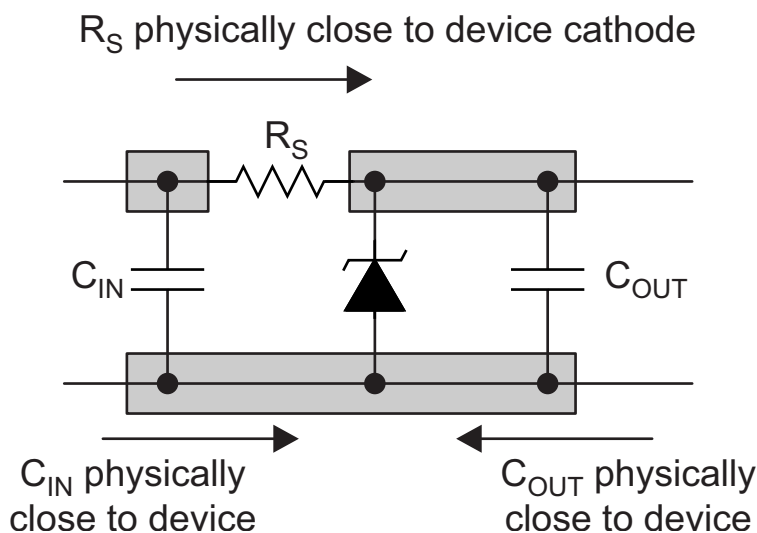


Figure 33. Layout Diagram

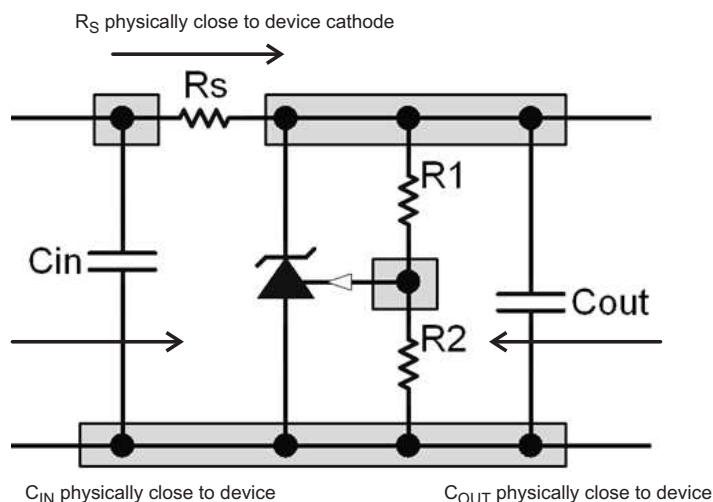


Figure 34. Feedback Resistors Layout Diagram

12 器件和文档支持

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

[SLYZ022](#) — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

表 1. SOT-23 封装标记信息

器件标记	标记位定义		
RHA RIA	第一位: R = 基准	第二位: H = 1.225V 电压选项 I = 可调节	第三位: A-C = 初始反向击穿 电压或基准电压容差 A = ±0.1%, B = ±0.2%, C = ±0.5%
RHB RIB			
RHC RIC			

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